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A LOW POWER SERIAL OUTPUT FLASH ADC IN 0,18 μm CMOS PROCESS

Al Al, Mamun Bin Ibne Reaz, Md. Syedul Amin, Mohd. Alauddin Mohd. Ali, Jae Sung Yu, Tae Gyu Chang

Original scientific paper
This paper proposes a simple design of a flash analog-to-digital converter (ADC) in 0,18 μm CMOS technology. This ADC is expected to be used within a temperature sensor, which provides analog data output having a range of 360 mV to 560 mV. This system consists of three main blocks: the threshold inverter quantization (TIQ)-comparator, encoder and parallel input serial output (PISO) register. The design goal is to get a flash ADC with low power dissipation, small size and compatible with the temperature sensors. The method is proposed to set each of the transistor channel length, for finding out the threshold voltage difference of the inverter each on the TIQ comparator. The design has an input range of 285 to 600 mV and 6-bit resolution output. The chip area of the designed ADC is 844,48 × 764,77 μm^2 and the power dissipation is 0,162 μW with 1,6 V supply voltage.

Keywords: *CMOS, Comparator, Flash ADC, Temperature Sensor*

Serijski izlazni impulsni ADC male snage u 0,18 μm CMOS postupku

Izvorni znanstveni članak
U radu se predlaže jednostavan projekt impulsno analogno-digitalnog pretvarača (ADC) u 0,18 μm CMOS tehnologiji. Taj bi se pretvarač trebao koristiti u senzoru temperature, koji daje izlaz analognih podataka u rasponu od 360 mV do 560 mV. Sustav se sastoji od tri glavna bloka: threshold inverter quantization (TIQ) - komparatora, kodnog uređaja (kodera) i parallel input serial output (PISO) registra. Svrha je projekta dobiti impulsni ADC s malim gubitkom energije, malih dimenzija i kompatibilnim sa senzorima temperature. Ovom bi se metodom trebala podesiti dužina svakog kanala tranzistora u svrhu pronalaženja razlike u ulaznom naponu pretvarača na TIQ komparatoru. Projektom se predviđa ulazni raspon od 285 do 600 mV i izlaz rezolucije 6-bita. Površina čipa projektiranog ADC je 844,48 × 764,77 μm^2 a gubitak energije iznosi 0,162 μW uz napajanje od 1,6 V.

Ključne riječi: *CMOS, komparator, impulsni ADC, senzor temperature*

1 Introduction

Technological developments and use of wireless-system applications with low power consumption have become one of the main attractions in the circuit design [1, 2]. Explosive growth of embedded sensors into radio frequency identification (RFID) tags are extensively used nowadays. In an RFID system, to read the data from sensors, a fully integrated and high performance ADC circuit is essential. This ADC is used to convert analog data into digital data format to facilitate the processing and transfer of data to the sensor implanted on RFID-Tag chip, which is integrated into the RFID system or wireless system.

The design is expected to have the lower power dissipation and operating voltage, small area size subsequent circuit. The ADC design presented in this paper is a converter suitable for a temperature sensor and easy to integrate with the other circuits. The ADC is proposed for the intention, it is Flash-ADC with TIQ-comparator applies, due the Flash-ADC has many advantages are high speed, high linearity, low voltage and reduce power dissipation [3, 4]. The previous researches have done a variety of methods to get the best performance of ADC.

There are several flash ADC designs proposed by different researchers with very low power dissipation. An inverter based design of ADC proposed by [5], shows the lowest power dissipation of only 1,66 μW. Besides, [6] proposed SAR ADC design method with a power dissipation of 1200 μW and [7] proposed a pipelined ADC with 348 mW power dissipation. But they did not get a lower power consumption compared to Flash ADC. This paper proposes a flash ADC designed with TIQ-comparator, encoder and PISO register, to obtain the best performance suitable for use in the wireless temperature sensor system. The aim of research is how to design a low power Flash ADC compatible with this system.

2 Material and methods

The complete system of flash ADC consists of three main blocks: TIQ comparator, encoder and PISO registers, as shown in Fig. 1.

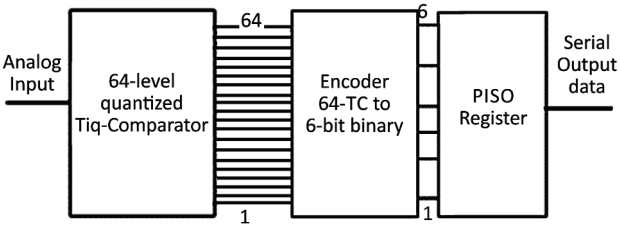

Figure 1 Block diagram of the flash ADC

The TIQ-Comparator is functioning as data quantization of the analog data to thermometer code (TC). This part is very important for ensuring linearity and the accuracy of the data transfer. The encoder makes sharper thresholding of comparator output and provides full digital output voltage swing converting to 6-bit binary code. So, if the comparator is less efficient the output data will be less accurate. The PISO register works to process 6-bit of parallel to serial data.

The temperature sensor will use this design in the range between −100° C to 200° C because the sensor shows excellent linear response in this temperature range. The sensor has a range analog output from 285 to 560 mV with the supply voltage 1,6 V and 31,14 μW power consumption. This sensor was founded on our previous research [8] and match to input of Flash ADC proposed.

2.1 TIQ comparator

A TIQ Comparator basic circuit consists of two cascaded CMOS inverters as shown in Fig. 2 [3]. The first inverter functions as voltage reference to the ADC system. The second inverter serves as the gain booster to keep the linearity in balance from the voltage rising and falling intervals.

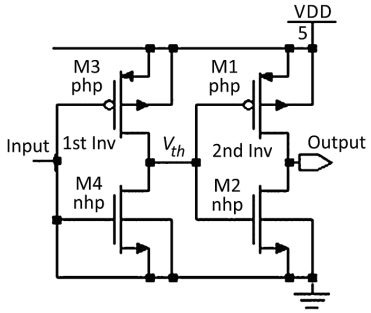

Figure 2 TIQ-comparator basic circuits

In the previous researches there are many methods for design of TIQ-comparator, such as: the analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) by means of transistor sizing [9, 10], the size of both transistor channel.

This research applies another method, by adjusting L and keeping W fixed. The advantages are reduced power consumption and area of the layout. Increasing L reduces the transistor drain current, I_D according to [11], for a transistor in saturated condition as Eq. (1).

$$I_D = \frac{1}{1}\left(\frac{\mu_n \varepsilon_{ox}}{t_{ox}} \cdot \frac{W}{L}\right) \cdot \left[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2\right], \quad (1)$$

where I_D is transistor drain current, μ_n is electron mobility, ε_{ox} is permittivity of the silicon dioxide, t_{ox} is the transistor channel width layer, W is transistor channel width, L is transistor channel length, V_{GS} is voltage gate–source, V_{tn} is the voltage drain-source voltages, V_{DS} is voltage drain-source.

The main design of TIQ comparator is converting analog data to 64-level thermometer data code as a block diagram in Fig. 3. This design is referred to that to obtain n-bit flash ADC is $(2^n - 1)$ comparator [12]. Therefore it is necessary to design a 6-bit Flash ADC is needed as much as $2^6 - 1 = 63$ TIQ comparators. Meanwhile, to get the CMOS transistor channel L of each first inverter refers to the mathematical expression of the threshold voltage (V_{th}) of any quantized sub-unit can be derived approximately as Eq. (2) [13, 14].

$$V_{th} = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{K_n}{K_p}}}{1 + \sqrt{\frac{K_n}{K_p}}}. \quad (2)$$

Here V_{tn} and V_{tp} are the threshold voltages for NMOS and PMOS devices, respectively and $K_n = (W/L)_n \mu_n C_{ox}$, $K_p = (W/L)_p \mu_p C_{ox}$, and μ_n and μ_p are the hole and electron mobility of NMOS and PMOS respectively.

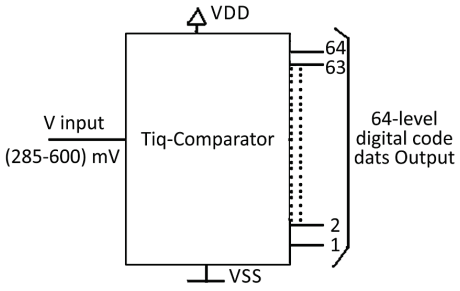

Figure 3 Block diagram of the TIQ-Comparator

Development of the comparator was based on the basic circuit given in Fig. 2 and Eq. (2). The Eq. (2) was used to calculate the PMOS transistor channel L of the first inverter, according to the desired value of threshold voltage and this result is shown in Tab. 1. The range of the threshold voltage this calculation is match necessary to the output voltage of the sensor, which is at list from 360 to 560 mV.

Table1 Calculation result of the transistor channel length and width

The first Inverter of PMOS transistor channel	The number of TIQ-comparator																				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Channel length (µm)	0,51	0,54	0,58	0,62	0,66	0,71	0,78	0,84	0,92	1,08	1,11	1,2	1,32	1,45	1,60	1,75	1,95	2,16	2,38	2,62	2,91
Channel width (µm)	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4

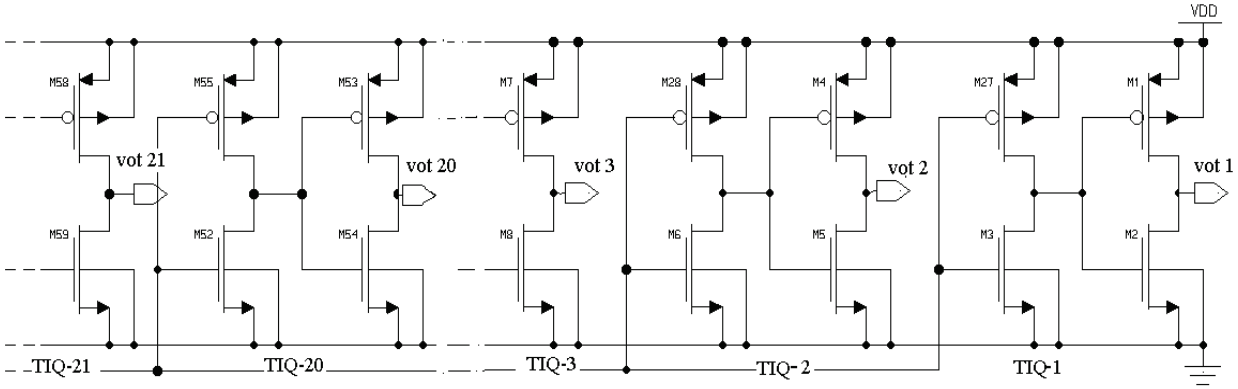

Figure 4 TIQ comparator schematic with the L channel varying

Further implementation of the design is done as follows: the design size of the *L* and channel *W* of the second inverter are fixed, according to the design standard of the 0,18 µm CMOS Technology. The standard design is 0,18 µm of *L* and 1,4 µm of *W* for PMOS and NMOS transistors respectively. Here, PMOS transistor's *W* on the first inverter is made on 1.4 µm fixed, whereas the channel length is different and these techniques are followed to next inverters, according to Fig. 4. However, NMOS of all inverters remain same ratio of *W* and channel *L*. The calculation is made starting with the most significant bit (MSB) of quantized to the least significant bit (LSB) with the value of Vth, 600 to 285 mV. In this calculation, it is obtained the size of the channel *L* for the comparator no. 1 to no. 21 only, with the channel *L* from 0,51 µm to 2,91 µm as shown in Fig. 4.

For the next comparator no. 22 to no. 63 are inserted one or two PMOS transistor as compensation in diode connection, to complement the achievement of the expected voltage input range to the lower side. The compensation transistor inserted between VDD to the first inverter PMOS transistors as shown in Fig. 5.

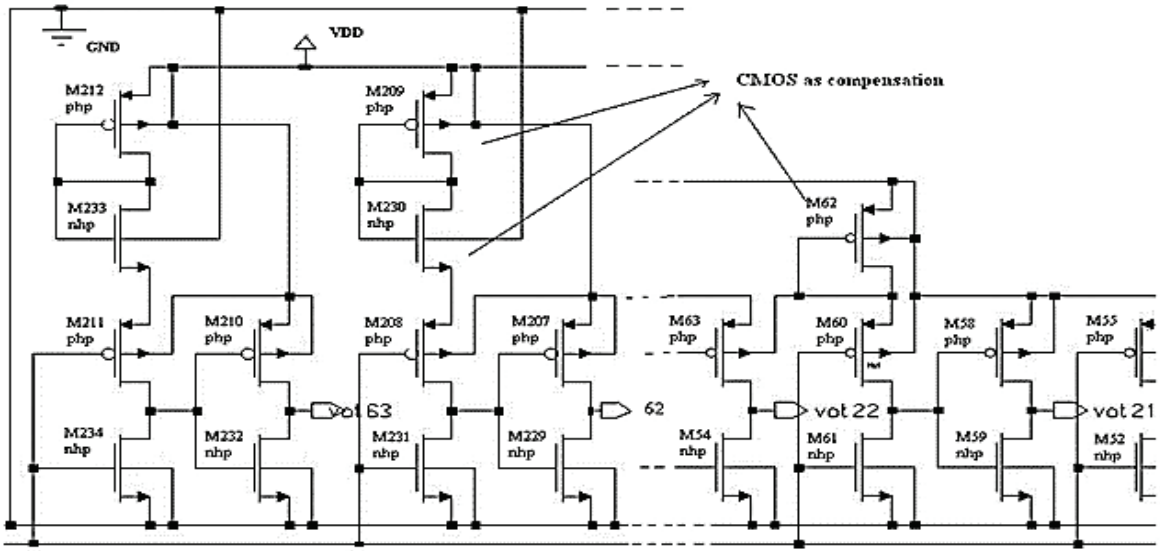

Figure 5 TIQ Comparator with CMOS compensation

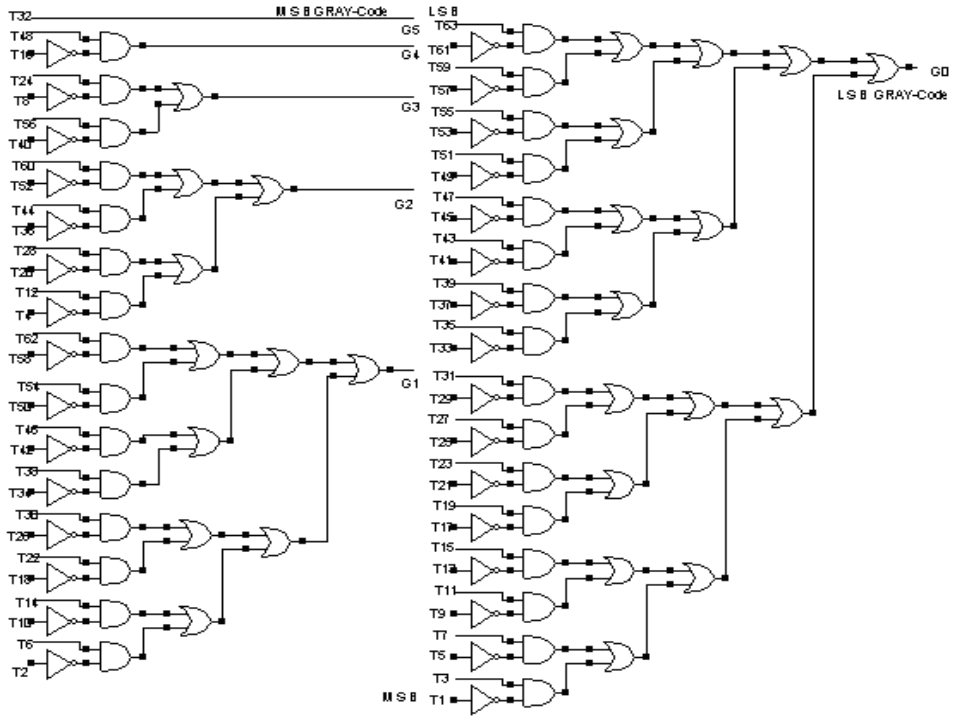

Figure 6 Grey code circuits

2.2 Grey code circuits

In the previous research works, many methods have been utilized for the design of the encoder circuit. There are: Fat-tree encoder [15]; MUX-based encoder [16, 17]; bubble error correction (BEC) circuit [18]; ROM based encoder [19]; logic-based encoder [20]. All the methods are proposing the same advantages such as high speed, high resolution, low power etc. Logic-based encoder is the best performance [21] and match to propose design. Due in this design is two the important points are low power and simple circuit. For these

benefits of low power and simple circuit, the encoder is redesigned, implementing the circuits by using CMOS logic gates in CEDEC standard library. In this process, the encoder has two functions: to eliminate the bubble-error and convert 64-level thermometer code to 6-bit binary. The bubble error is the result of many sources, for instance, clock jitter, device mismatch, offset voltage. The input thermometer code of a circuit is invalid code and there is no correction circuit, consequently output of the ADC in this case is incorrect [18].

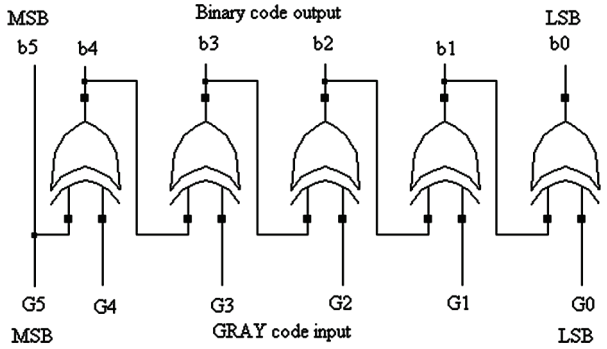

Figure 7 Decoder circuits

Circuits of the proposed encoder consist of gray circuits and decoder circuits. The grey circuit contains NOT, AND and OR gate configuration as in Fig. 6.

Output of the grey circuits follows to the decoder circuits convert to 6-bit binary code. The decoder circuits contain EXOR-gate configuration as in Fig. 7 where, T is a thermometer code with T63 is LSB and T1 is MSB. G is a grey code with G0 is LSB and G5 MSB. Follow expression, b is binary code with b0 is LSB and b5 is MSB and b5 = G5, b4 = G5 (+) G4, b3 = b4 (+) G3b2 = b3 (+) G2.

Converting 64-level TC to BCs is shown in Tab. 3. The Booleans algebra can be expressed as:

G5 = T32, G4 = T48.T16, G3 = T56.T40 + T24.T8 ,
G2 = T60.T52 + T44.T36 + T28.T20 + T12.T4 ,
G1 = T62.T58 + T54.T50 + T46.T42 + T38.T34 + T30.T26 + T22.T18 + T14.T10 +T6.T2 , G0 = T63.T61 + T59.T57 + T55.T53 + T51.T49 + T47.T45 + T43.T41 + T39.T37 + T35.T33 + T31.T29 + T27.T25 + T23.T21 + T19.T17 + T15.T13 + T11.T9 + T7.T5 + T3.T1
b1 = b2 (+) G1, b0 = b1 (+) G0

The thermometer code convert to gray code and convert to 6-bit binary are shown in the Tab. 2.

Table 2 Thermometer code to gray code and to 6-bit biner

No	Thermometer Code										Gray Code						6-bit binary					
	T63	T62	T61	-	T32	-	T4	T3	T2	T1	G5	G4	G3	G2	G1	G0	b0	b1	b2	b3	b4	b5
0	0	0	0	-	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	-	0	-	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1
2	0	0	0	-	0	-	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	0
3	0	0	0	-	0	-	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1
4	0	0	0	-	0	-	1	1	1	1	0	0	0	1	1	0	0	0	0	1	0	0
-	-	-	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
32	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0
-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
61	0	0	1	-	1	-	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1
62	0	1	1	-	1	-	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0
63	1	1	1	-	1	-	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1

2.3 PISO register

Parallel input serial output (PISO) register is functioning as converting parallel 6-bit binary to serial output as in Tab. 4. The low power of shift register design was proposed by [22], using D flip-flop in weak inversion region. For the efficient design of the register was used D flip-flop by [23]. In this design, the PISO register circuit is configured of D-FF with load and clock control as in Fig. 8. Both their controls are arranging data shifting in the shift-register system. Parallel 6-bit binary data convert to serial output data are shown in Tab. 3.

Table 3 Parallel 6-bit binary to serial on 1 byte data

CLK	Parallel Data Input						Serial Output
	B5 MSB	B4	B3	B2	B1	B0 LSB	
0	1	0	1	0	1	0	X
1	X	1	0	1	0	1	0 LSB
2	X	X	1	0	1	0	1
3	X	X	X	1	0	1	0
4	X	X	X	X	1	0	1
5	X	X	X	X	X	1	0
6	X	x	X	X	X	X	1 MSB

3 Results and discussion

The circuit design is designed and simulated by using the tools of the Mentor Graphics Design Architect (DA) CEDEC_KIT. The design and simulations are carried out to achieve a linear quantization value repeatedly. To obtain a linear quantization value in the simulation of 0.0 V to 0.61 V is given by the DC input signal as Fig. 9, while to obtain a frequency response of quantization from 1 to 10 KHz is given by the AC signal input as in Fig. 10.

In Fig. 9, it is shown that the conversion of analog input to quantization output responding range from 0,285 V to 0,6 V. During the increment of 5 mV in the DC input, the quantization output increases 1 level.

Fig. 10 illustrates the simulated result of the TIQ Comparator designed on 64 levels of quantization with the sinusoidal input voltage of 0 V to 0,6 V - peak at the frequency 10 kHz and half wave positive transition. This graphical response exhibits a good linearity and sensitivity with linear rise and fall of the input signal.

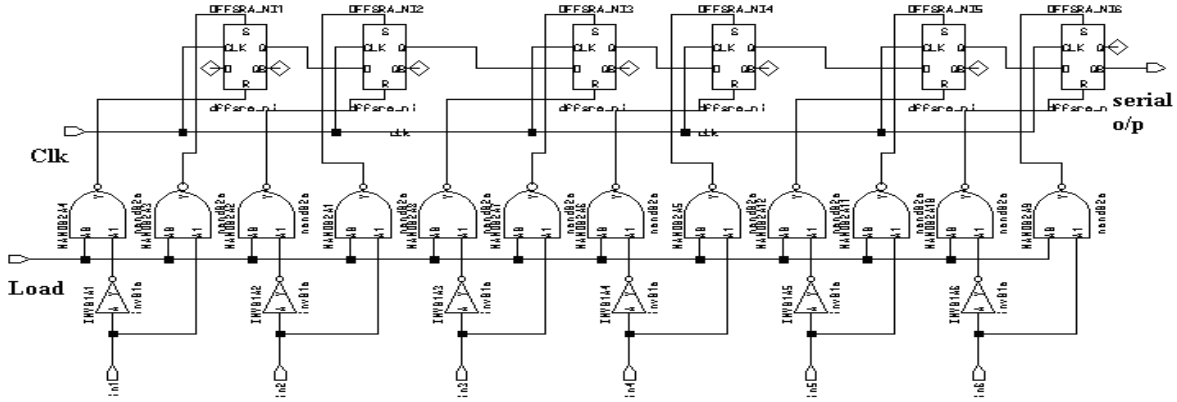

Figure 8 6-bit PISO Register circuits

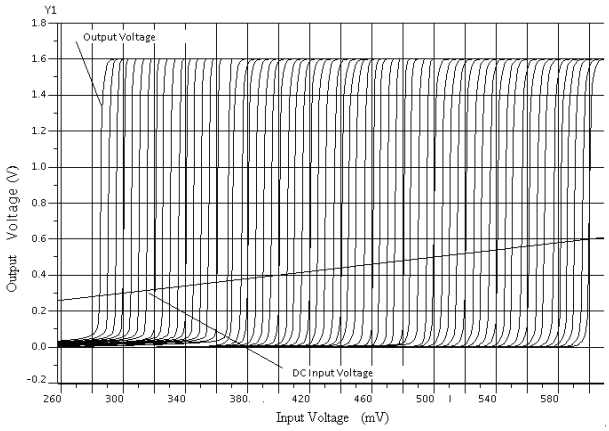

Figure 9 Quantized output for the DC input voltages 0 to 0,61 V

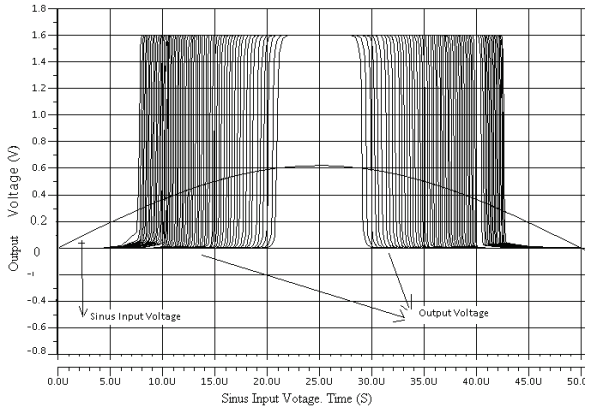

Figure 10 Quantized output for the sine input voltage of 0,61 V and frequency of 10 KHz

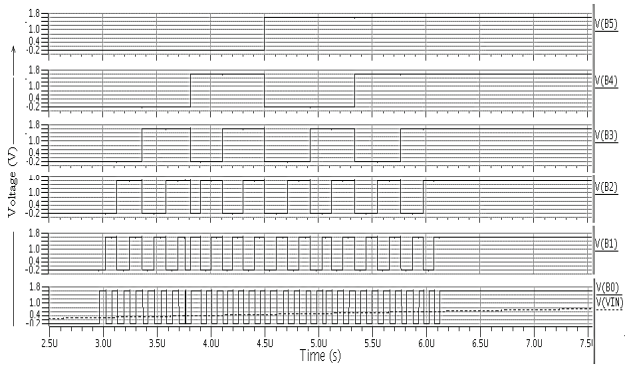

Figure 11 The encoder output graph with the signal input rising

The Encoder output graph is shown in Fig. 11. This output is the result of simulation synchrony to Fig. 8 and matches Tab. 3 of design principle. Fig. 12 is showing the simulation results of PISO registers with 6 bit binary parallel input and serial output. Pulse clock (V clock) function as shift control on register and pulse load (V load) for reset of the register every one byte data transfer.

The final layout design of the chip is shown in Fig. 13. The chip design consists of three main blocks: TIQ-comparator, encoder and PISO register. Around the circuit is added pad terminal to connect the circuits with the power supply as well as input and output pin. All of the blocks of the flash ADC integrated in this chip, with the layout size 844,48 × 764,77 μm^2.

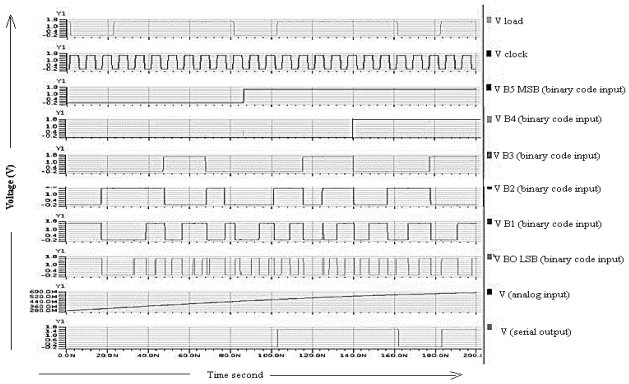

Figure 12 The simulation results of PISO register

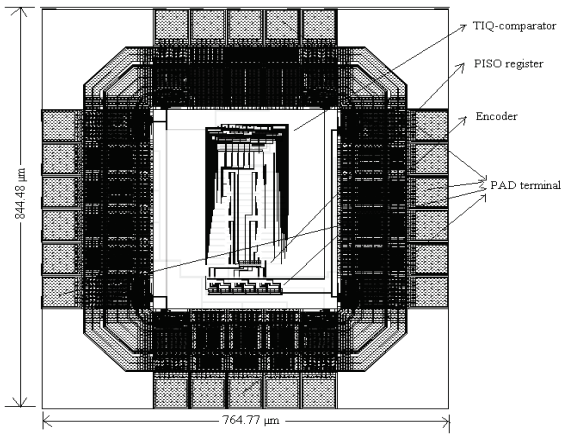

Figure 13 The Layout design

Tab. 5 shows the comparison result of the proposed ADC with other Flash ADC architectures. It can be seen that the proposed design shows the lowest power dissipation because of judicious choice of *W*/*L* of the CMOSs. The layout area of the design is shown in Fig. 13

with the pad terminal included, whereas the other designs are featured by excluding pad terminal. The total area of the circuit including pads is (844,48 × 764,77) µm^2. However this layout size of the pad depends on the library CEDEC standard design. Hence, the proposed design did not appear the smallest layout size in Tab. 4.

Table 4 The comparison of the proposed design to the other flash ADCs

References	Design				
	Architecture/Method	CMOS technology (µm)	Supply voltage (V)	Power dissipation (µW)	Layout area (µm)
[3]	Flash/TIQ technique	0,25	2,375 to 2,65	35 250	228
[5]	Flash/comparator redundancy	0,18	0,2 to 0,9	1.66	1 960 000
[19]	Flash/ extend the TIQ	0,18	1,8	36 980	-
[24]	Flash/data trees	0,35	5	500 000	-
[25]	Flash/TIQ technique	0,18	1,8	20 000	8 000 000
[26]	Flash/TIQ technique and sh circuit	0,35	2,5	5000	-
[27]	Flash/sh circuit	0,18	1,8	5300	-
[28]	Flash/reference voltage and common mode calibration	0,065	1,2	4000	130 000
[29]	Flash	0.090	1,2	1919	-
[30]	Flash/Sub Flash	0,065	1,0	15 000	1 000 000
[31]	Flash/Time domain comparator	0,18	1,8	8000	13 200
Proposed design	Flash/TIQ Comparator	0,18	1,6	0,162	645 832

4 Conclusion

The flash ADC is designed and verified by using the Mentor Graphics VLSI Design Software. The final chip is designed by CEDEC industry standard I/O cell library for fabrication lab Silterra Malaysia. It consists of 63 pairs of CMOS inverters in the-TIQ comparator part, the logic based is used for the encoder part, and D FF for the PISO register development. The design has an input range of 285 to 600 mV and 6-bit resolution output. The chip area of the designed ADC including pads is 844,48 × 764,77 µm^2.The power dissipation is only 0,162 µW in 1,6 V supply voltage and the sinusoidal input voltage of 0V to 0,6 V peak at the 10 kHz frequency and positive half wave transition condition. This design is suitable for use in the wireless temperature sensor system.

Acknowledgments

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Authors' addresses

Al Al, PhD Student
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 UKM, Bangi, Selangor, Malaysia
E-mail: al_mt62@yahoo.com

Mamun Bin Ibne Reaz, PhD, Professor
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 UKM, Bangi, Selangor, Malaysia
E-mail: mamun.reaz@gmail.com

Md. Syedul Amin, PhD Student
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 UKM, Bangi, Selangor, Malaysia
E-mail: syedul8585@yahoo.com;

Mohd. Alauddin Mohd. Ali, PhD, Professor
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 UKM, Bangi, Selangor, Malaysia
E-mail: mama@eng.ukm.my

Jae Sung Yu, Masters Student
School of Electrical and Electronics Engineering
Chung-Ang University
221, Heuksuk-dong, Dongjak-ku
Seoul 156-756, South Korea

Tae Gyu Chang, PhD, Professor
School of Electrical and Electronics Engineering
Chung-Ang University
221, Heuksuk-dong, Dongjak-ku
Seoul 156-756, South Korea
E-mail: tgchang@cau.ac.kr