

An IC architecture for RF Energy Harvesting systems

Leonardo Pantoli, Alfiero Leoni, Vincenzo Stornelli, and Giuseppe Ferri

Original scientific paper

Abstract— In this work we present an IC architecture for RF energy harvesting. The system has been designed with a 0.18 μm CMOS SMIC technology and optimized at 900MHz. Simulation results have confirmed that the integrated system handles an incoming power typically ranging from -25 dBm to 20 dBm by rectifying the variable input signals into a DC voltage source with an overall efficiency up to 50%. The chip area estimation for the proposed system is as low as 3x3mm².

Keywords—Energy harvesting; integrated circuits; autonomous devices; RF signals; low-power.

I. INTRODUCTION

In the last years, the number of RF sources that are available within urban environments is rapidly increasing thanks to the development of wireless communication systems that have replaced the massive cable interconnections. Beyond reducing the complexity of the systems, this tendency leads to the availability of many ambient energy still not used. Relying the electromagnetic (EM) energy, typically, a spectral survey reveals a wide range of energy contributions in the environment that are difficult to collect and store [1-4]. Till now, many RF energy harvesters have been presented in the literature, but only a few have been able to catch energy with good efficiency [5-10] being, especially at very low RF available energy, difficult to achieve good rectifiers. There are many problems that limit the collection of these resources, as for instance the not constant presence of the EM signals in the environment during the day and their spectral characteristics, due to modern communication codes, that spread the transmitted energy. From an electronic point of view, there are physical limitations that do not facilitate the realization of EM energy harvesters [5-12]. In particular, for what concerns the antenna and rectification section, its pattern and characteristics are strictly related to the target incoming frequency; another critical part is the regulation and storage section, because being not constant in time, the caught energy cannot be furnished to any devices but must be stored and provided on request, if available. Finally, any harvester systems may guaranty a conversion efficiency in order to provide more energy with respect to that it requires to properly work and be reasonably used. All these critical aspects are, in some way, mitigated by the recent advances and expansion that have involved the integrated technology.

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The enhancements can be appreciated, at least, by two different points of view. Concerning the usefulness, in the last years both the size and power supply have been drastically decreased for many devices [13-15]. As a consequence, the idea to produce enough power to recharge the battery or directly supply the electronics is becoming even more consistent. About the reliability, the integrated circuit (IC) solutions will give more emphasis in the development of miniaturized energy harvesters with reduced power consumption and improved capability to track the energy variations of the incoming EM beam. These aspects will lead to energy harvesting systems with improved efficiency and advanced real-time operation capability. Also the receiving section may achieve further benefits from the IC technology with the possibility to realize integrated antenna of different topologies with compact dimensions and a wider operational bandwidth. The same authors have already developed and presented a discrete version of an energy harvester system capable to catch and manage RF radiation at 936 MHz (used for mobile GSM transmissions) and 2.4 GHz (frequency adopted for Wi-Fi internet connections) [16-18]. The aim of this work is to reproduce the promising results obtained with the discrete element board by means of an integrated technology: novel and completely integrable circuits and architectures are here presented for the first time. Each building block may be analyzed and reconsidered at technology level with important advantages in term of performance and miniaturization. Preliminary results are shown in this paper and have been obtained at simulation level using a 0.18 μm CMOS SMIC technology with the aim to evaluate the expected additional benefits that can be achieved with future integration.

II. PROPOSED DISCRETE ARCHITECTURE

A basic architecture for the realization of an energy harvester is shown in Fig. 1. Below the discrete, external, antenna, typically a matching network is used to transfer the incoming power towards the following signal managing circuits. In some cases, also a pass-band or a low-pass filter is used to eliminate unwanted frequency components that cannot be handled by the designed circuit. An important structure that must be carefully designed is the passive rectifier which must be able to perform the AC/DC transformation and it is usually designed with diode architectures. Finally, we usually have a storage section that implements the important function of energy storage or supply to external devices.

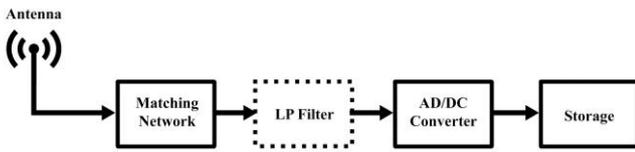


Fig. 1. Energy harvester simple architecture.

The harvester architecture that has been designed is illustrated in Fig. 2, while the detailed block scheme is shown in Fig. 3. It is conceived for operating in two separate bandwidth (the GSM sub-band of 936 MHz and the *WiFi* channel at 2.4GHz) and organized to handle different power levels on different channels in order to improve the conversion efficiency. There are two energy conversion channels (“Low Power” and “Medium Power” in Fig. 3), each of which optimized to work with a different range of incoming power levels at both the considered frequencies, being after the antenna considered a 1:100 transformer. The recovered energy is then manipulated by a common regulation and storage section. A feedback control network realized with a voltage comparator is responsible of switching the incoming power in the appropriate channel. It is an ultra-low power component that compares the rectified voltage with an internal voltage threshold and conveys the EM radiation towards the dedicated receiver. The “Low Power” way is conceived to manage an input power in the range (-25 : 5) dBm, while the “Medium Power” channel is optimized to work with input power levels going from 5 dBm to 20 dBm. Both the channels foresee the AC/DC converter and different matching network, realized with passive components. In the discrete prototype, the following regulation and storage section have been realized with commercial components and makes use of an ultra-low voltage Step-Up Converter, the LT3108 from Linear Technology, that decouples the system from the generic load or device and boosts the incoming signal to the regulation section. Finally, a common load as a “storing section” is used for simulation and performance evaluation. In Fig. 3 for instance, a gas sensor has been used.

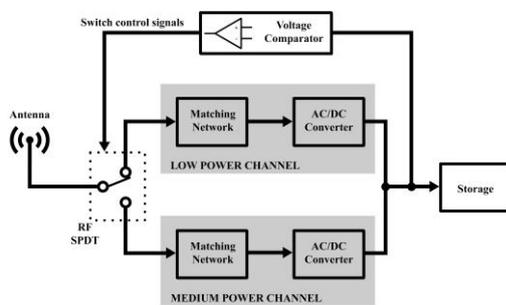


Fig. 2. Simplified scheme of the conceived architecture.

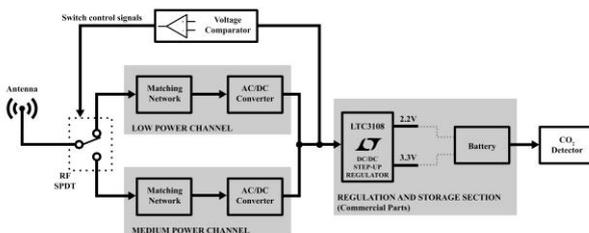


Fig. 3. Detailed block scheme of the designed, discrete, energy harvester architecture.

III. INTEGRATED SOLUTION EVALUATION

Concerning the novel IC solution, a feasibility study has been performed in order to obtain a reliable, miniaturized solution with improved performance both in term of conversion efficiency and harvested energy. The evaluation is performed at simulation level using a 0.18 μ m CMOS SMIC technology and considering a reference frequency of 900 MHz that is used for both mobile phone service and digital television. In particular, the attention has been focused on the simplified architecture of Fig. 2, paying attention on the rectifiers, the voltage comparator and the DC/DC boost converter that are the most critical parts to catch and manage the incoming radiation (Fig. 4).

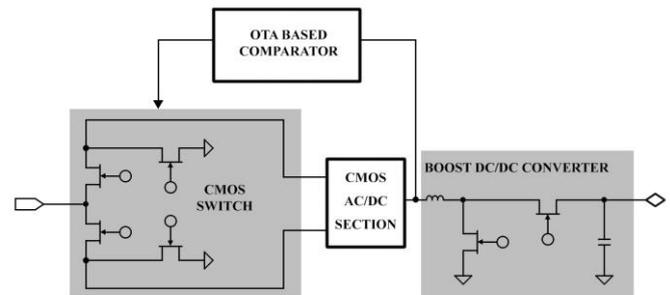


Fig. 4. Block scheme of the integrated version of the harvester.

About the antenna, a dipole antenna has been taken into account since it shows good performance on a wider bandwidth and can be successfully miniaturized adopting more complex geometry, as for instance in [19, 20]. In particular, a geometry folded dipole antenna similar to that proposed in [19] has been considered and is shown in Fig. 5. For system simulation purposes, the antenna has been simulated with Momentum software also considering a 1:100 RF transformer and represented by a Thevenin equivalent source considering its impedance.

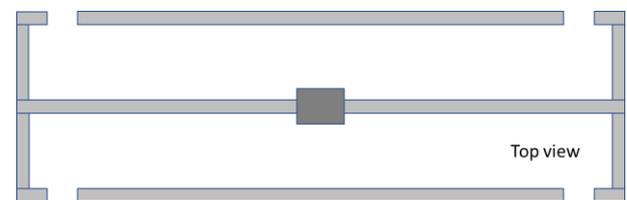


Fig. 5. Simplified representation of the considered folded dipole antenna.

The RF Switch can be easily realized with parallel MOS transistors controlled by means of gate voltages, as shown in the miniature of Fig. 4. The comparator is a crucial element in the RF chain since even if it makes possible to double the power management chains, it requires a bias voltage and a reference voltage to set a suitable voltage threshold. The proposed solution concerns the realization of the comparator with a couple of low-voltage, low-power operational transconductance amplifiers (OTAs) [21,22] that allow to minimize the requested power to drive the switch. The circuit here adopted for the OTA is shown in Fig. 6 and it requires a very low biasing level (<1 μ W) that can be easily recovered

from the storage section itself. Obviously, we are supposing the system will be provided of a rechargeable battery pack, initially charged, so avoiding the use of an external supply voltage for a while, until the incoming RF radiation arises to a sufficient value to auto-sustain the circuit functionality. In detail, the OTA has two stages: an input symmetrical OTA ($M1-M9$) that decreases systematic and random offsets; a source degenerated output stage ($M10-M13$) that allows to obtain a full dynamic output range. Compensation is ensured by RC series network, while a high slew-rate value is obtained properly dimensioning a suitable V_{th} -dependent current generator through ($M14-M17$, $R1$). This current reference uses a “start-up” circuit.

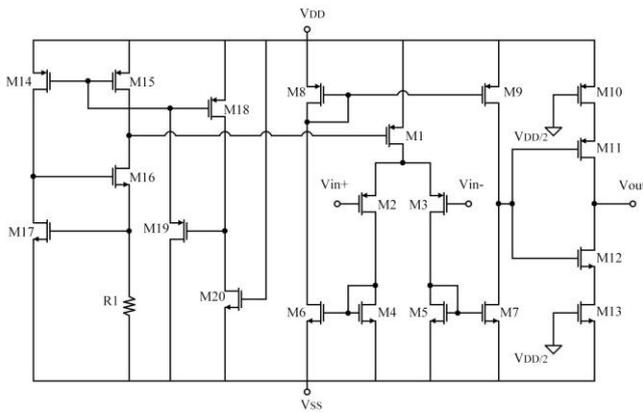


Fig. 6. Designed LV-LP OTA used for the comparator.

Concerning the voltage rectifier, being the two channels of the harvester dimensioned to handle quite different input power levels, it has been necessary to develop different solutions for this building block in order to have at the same time good sensitivity and the capability to manage large input power levels, so ensuring a wide dynamic range. The solution adopted for the medium-power channel is reported in Fig. 7 and derived by the architecture proposed in [22]. It is a full-wave gate cross-coupled rectifiers where the transistors in the two main branches are cross-coupled. This configuration limits the associated voltage drop due to the voltage threshold of the MOS transistor and allows to obtain a higher power efficiency towards classical diode-based solutions. The low-power channel has been conceived with a different scheme, keeping advantages of the solution always proposed in [23]. Since this channel is devoted to handle low-power levels, improved performance in term of efficiency and sensitivity are necessary. The adopted solution implements two MOS switches with very low effective threshold voltage to replace the classical diode-connected pMOS transistors usually employed. In addition, this architecture also take advantages from the cross coupled structures that are applied to the MOS transistors and this allows to drive the transistors with a larger voltage swing, increasing the output voltage and improving the power conversion efficiency. A dynamic bulk biasing circuit for diode-connected transistors $M5 - M6$ is also used for reducing the circuit dropout voltage and power dissipation at start up.

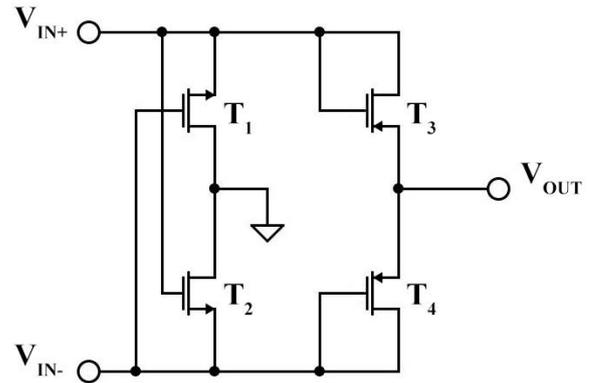


Fig. 7. Schematic of full-wave medium-power channel rectifier as proposed in [23].

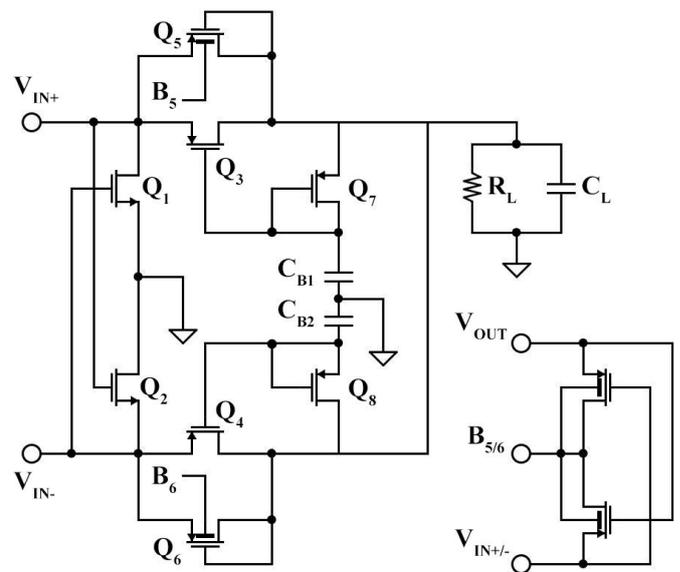


Fig. 8. Schematic of full-wave low-power channel rectifier as proposed in [23].

Finally, the solution illustrated in Fig. 9 has been adopted for the Boost DC/DC converter [24]. In this design, two instances of the low-power OTA (that is shown in Fig.6) are used in a charge pump configuration to multiply the input voltage. The first OTA acts as a relaxation oscillator, serving as the master charge-pump clock, while the second amplifier is configured as a comparator slaved to the timing cycle established by the first one. Considering the same definition of the Efficiency parameter as in [18], that is, the ratio between the incoming power and the rectified power, preliminary simulation results have confirmed that the integrated system handles an incoming power typically ranging from -25 dBm to 5 dBm by rectifying the variable input signals into a DC voltage source with an overall efficiency up to 50%. In Fig. 10 and Fig. 11, simulation results concerning the conversion efficiency on the two channels are shown confirming the suitability of the proposed circuits towards portable system applications. The chip area estimation for the proposed system is as low as $3 \times 3 \text{ mm}^2$.

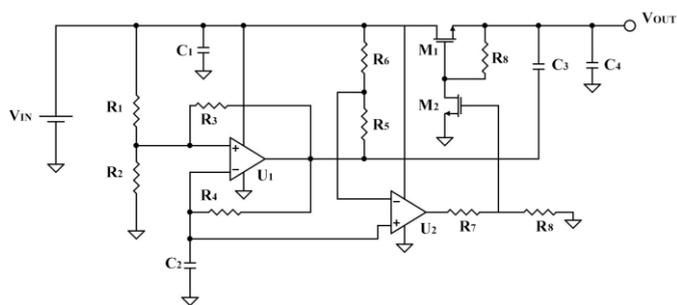


Fig. 9. Simplified schematic of the boost DC/DC converter.

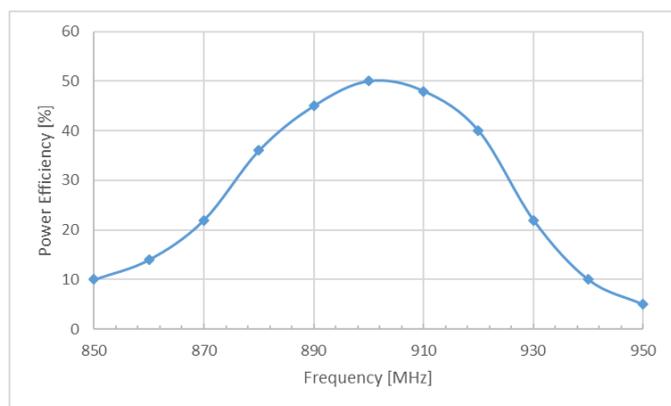


Fig. 10. Conversion efficiency for the low power channel at 0 dBm input power

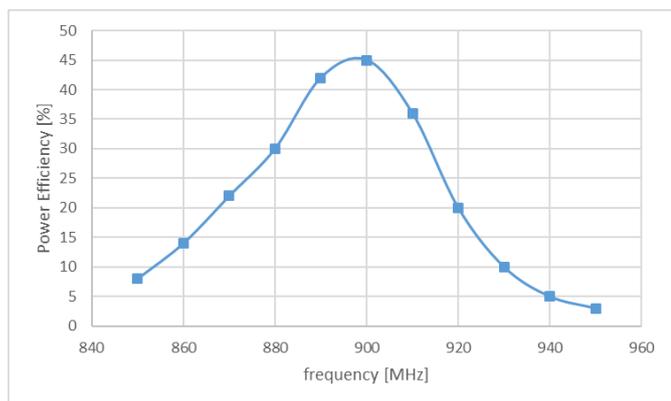


Fig. 11. Conversion efficiency for the medium power channel at 10 dBm input power

IV. CONCLUSION

We have presented preliminary simulation results about IC architecture for the realization of a dual band RF energy harvesting system. The solution here addressed takes advantages of the results already obtained by the same authors with a discrete prototype board operating at both GSM and Wifi frequencies. The integrated version has utilized models taken from a 0.18 μ m CMOS SMIC technology and the system has been dimensioned at 900MHz. Circuitry details of the main building block have been described and preliminary

results demonstrate the feasibility of the proposed solution and good reliability in terms of its performances.

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