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An Integrated Approach to Power Electronics Systems

Today's power electronics systems are typically manufactured using non-standard parts, resulting in labor-intensive manufacturing processes, increased cost and poor reliability. As a possible way to overcome these problems, this paper discusses an integrated approach to design and manufacture power electronics systems to improve performance, reliability and cost effectiveness. Addressed in the paper are the technologies being developed for integration of both power supplies and motor drives. These technologies include the planar metalization to eliminate bonding wires, the integration of power passives, the integration of current sensors, the development of power devices to facilitate integration as well as to improve performance, and the integration of necessary CAD tools to address the multidisciplinary aspects of integrated systems. The development of Integrated Power Electronics Modules (IPEMs) is demonstrated for two applications: (1) 1 kW asymmetrical half-bridge DC-DC converter and (2) 1–3 kW motor drive for heating, ventilation and air conditioning (HVAC). Electrical and thermal design tradeoffs of IPEMs and related enabling technologies are described in the paper.

Key words: packaging, power integrated circuits, power semiconductor devices, sensors, and integrated design methodology

1 INTRODUCTION

The fundamental approach to power conversion has steadily moved toward »high-frequency synthesis«, resulting in important reductions in converter performance, size, weight and cost. However, in some high frequency power conversion technologies, fundamental limits are being reached that will not be overcome without a radical change in the design and implementation of power electronics systems. It is well recognized within the industrial sector that the performance of power electronics systems were driven by improvements in semiconductor components over the last decades. Moving from bipolar to MOSFET technology [1, 2] has resulted in speed increases that, today, test the limits of packaging inductance and thermal handling. Thus, an order of magnitude increase in switching speed, which is possible with new device technologies, will require substantial reductions in structural capacitances and inductances associated with device and system-level packaging.

For a typical power electronics system, individual power devices are mounted on the heat sink, and the drivers, sensors, and protection circuits are implemented on a printed circuit board and mounted near the power devices. The manufacturing process for such equipment is labor and cost-intensive. However, some manufacturers have taken a more aggressive approach in recent years, developing a high level of integration where power semiconductors in the die form are mounted on a common substrate with wire bonding. Although the wire bonding technology has seen many improvements in reliability, this approach still limits the possibilities of three-dimensional integration, as well as having electromagnetic layout constraints. The thermal management in this type of packaging is essentially limited to one-dimensional heat flow, while the reduction of structural inductance associated with bonding wires have limitations.

It is perceived, however, that power electronics modules constitute one of the driving forces towards modularization and integration of power electronics systems. Recent innovations in power modules have been mostly pushed by semiconductor development with the help of improved layout and packaging technologies. The development trends are focused on increasing current and voltage levels, increasing temperature, enhancing reliability and functionality, as well as reducing size, weight and cost [4]. New ideas on power modules include the reduction of the number of interfaces to reduce the number of solder layers and the risk of solder imperfections and thermal fatigue. Another concept that has been around is the elimination of the base plate from the power module, first observed at low power and now migrating to higher power applications. In terms of reliability improvement, devices using low temperature joint (LTJ) technology do not change their thermal resistance after extensive

power cycles (>50 000), as opposed to devices using low temperature conventional solder techniques that achieve the end of useful life after 30 000 power cycles [4].

While semiconductor devices are still one of the dominant barriers for future power system development, devices do not currently pose the fundamental limitation to power conversion technology. It is rather packaging, control, thermal management, and system integration issues that are the dominant technology barriers currently limiting the rapid growth of power conversion applications [3]. To address some of these issues, this paper briefly discusses the technology advancements needed to improve the characteristics of power electronics systems, as well as the technologies being developed for integration of multi-kilowatt power electronic equipment. Among these technologies being developed are the planar metalization device interconnect, that allows three-dimensional integration of power devices, and the integration of power passives to increase the power density, mainly for power supply applications. The technologies being developed span a wide range of applications from distributed power systems to motor drives. The development of packaging techniques, integration of current sensors and the development of power semiconductor devices to either improve performance or to facilitate integration of power electronics systems are addressed hereafter. This paper also discusses results obtained from the various technologies being developed within the research scope of the Center for Power Electronics Systems (CPES), whose mission is to promote an integrated approach to power electronics systems in the form of highly Integrated Power Electronics Modules (IPEMs).

2 PACKAGING OF POWER ELECTRONICS SYSTEMS – THE DPS EXAMPLE

The use of distributed power systems (DPS) for computer and telecommunication applications has opened up the opportunity to develop a standardized modular approach to power processing, which will improve the design and manufacturing processes significantly, as well as enhance the electrical system performance. For this reason, a DPS has been chosen to demonstrate the advantages of integrating power electronics systems.

The structure of a typical DPS is shown in Figure 1 (a), while a building block of a front-end converter is illustrated in details in Figure 1(b). A typical three-dimensional solid-body model representation for this type of system is shown in Figure 2(a). As observed, the existing approach requires discrete components, which makes it difficult to optimize space usage and to increase power density of the
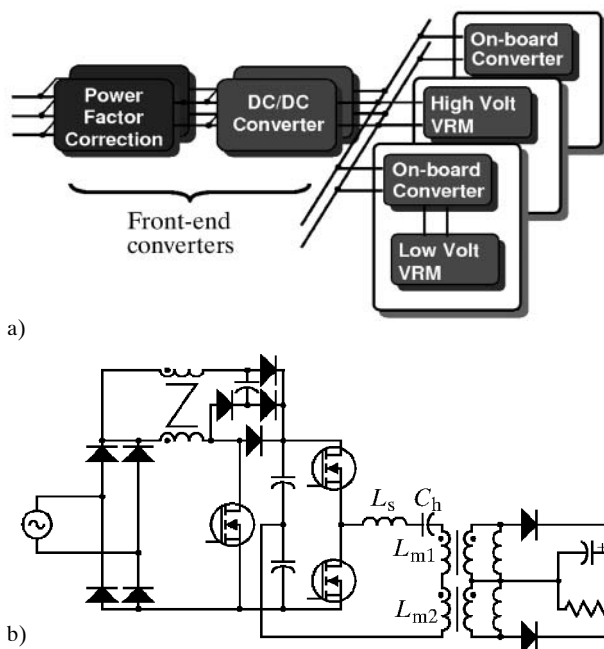

a)

b)

Fig. 1 (a) Distributed power system and (b) front-end PFC and DC-DC converters

entire system. The solid-body model shows that the components of the front-end converter are distributed on the printed circuit board, while Cu traces are routed to distribute power and control signals to all devices. This type of layout approach presents severe limitations from the electrical and thermal viewpoints. Figure 2(b) shows the top view of the 3-D solid-body model. The major components are identified in the same figure, as well as the critical paths defining which components must be placed next to each other in order to reduce parasitic inductance. The inductance formed by the critical loop will generate voltage overshoot across the PFC and DC-DC switches during turn-off.

Although bringing devices together helps reduce the structural inductances, there is a clear limitation to this packaging approach because the space optimization is limited by the form factor of the various components. Therefore, the structural inductance of the packaging approach shown in Figure 2(a) becomes a limiting factor to increasing switching frequency and power level. The only way to overcome this problem is to minimize the parasitic inductance of critical paths by seeking integrated approaches for power devices and components. The realization of an integrated power electronics system requires advances in technologies, which depend upon finding solutions to deal with the multi-disciplinary issues in materials, electromagnetic compatibility and thermal management.
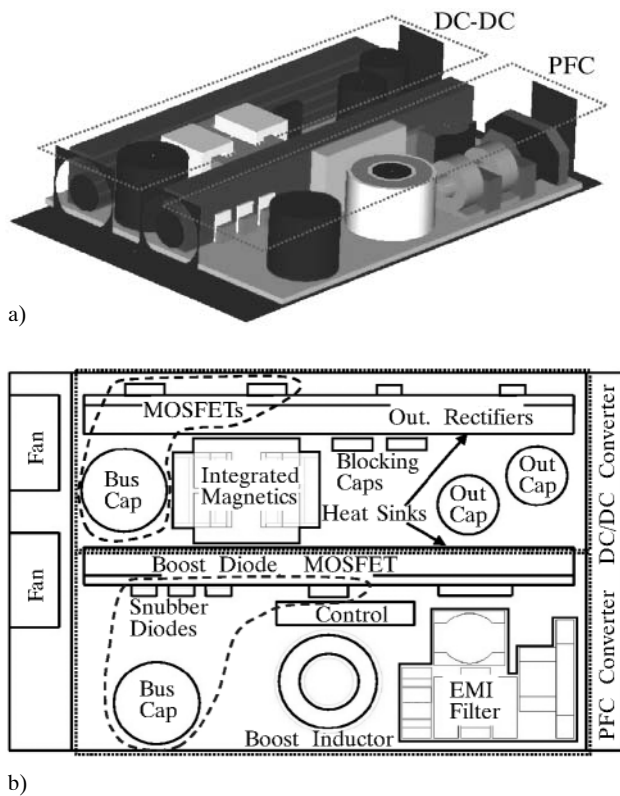
a)

b)

*Fig. 2 Typical component layout for DPS applications: (a) 3-D so-
lid-body model and (b) top view and critical paths of a typical DPS
front-end converter*

Although the end objective is to integrate functi-
ons and components for both the PFC and DC-DC
converters shown in Figure 1(b), the results repor-
ted hereafter are related to the integration of the
front-end asymmetric half-bridge DC-DC converter
(AHBC) illustrated in Figure 3. In the same figure,
two blocks are highlighted as active and passive
IPEMs. The active IPEM represents the integration
of power MOSFETs and gate drivers, while the
passive IPEM represents the electromagnetic inte-
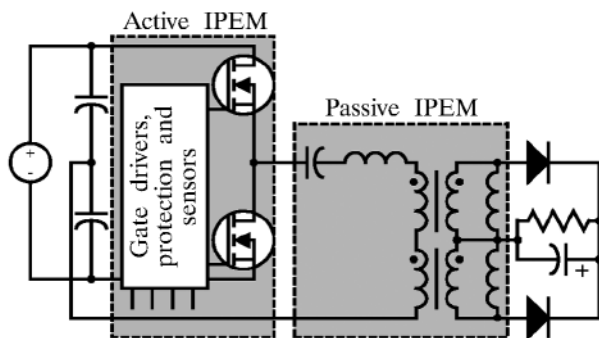gration of the DC blocking capacitor, transformer

*Fig. 3 Asymmetrical half-bridge DC-DC converter (AHBC) with ac-
tive and passive IPEMs*

and output inductors of the current doubler confi-
guration used in the AHBC. The main purposes of
integration are to reduce parts count, increase po-
wer density, develop a modular approach to power
electronics systems, and reduce the overall number
of interconnections at the system level.

2.1 DPS IPEM Design and Implementation Using the Embedded Power Technology

In designing an integrated system, several steps
must be taken towards defining specifications at the
system level, as well as at the module level. Table 1
shows specifications for the DC-DC converter at
200 kHz, while Table 2 and Table 3 describe the re-
quirements for the active and passive IPEMs.

Table 1 **System-level (DC-DC converter) specifications**

Parameter	Specification
Input voltage	300 V – 415 V
Output voltage	48 V ± 10 %
Output voltage ripple (pk-pk)	480 mV
Isolation (output to ground)	>10 kΩ
Output power	1 kW
Ambient temperature	50 C
Air flow at 5000 ft	20 CFM at 50 C amb 15 CFM at 35 C amb
Safety	UL 60950
EMI system-level	EN55022 Class B

Table 2 **Active IPEM requirements**

Parameter	Specification
DC bus voltage (500 device)	400 V
Surge of DC Bus voltage	415 V
Power terminal current	25 A
Junction temperature (max.)	150 C
Maximum operating junction temperature	125 C
Operating case temperature	–20 C – 100 C
Isolation voltage (case-to-terminal at 60 Hz)	>2500 V
Power terminal leakage current	<500 μA
Maximum switching frequency	500 kHz

Table 3 **Passive IPEM requirements**

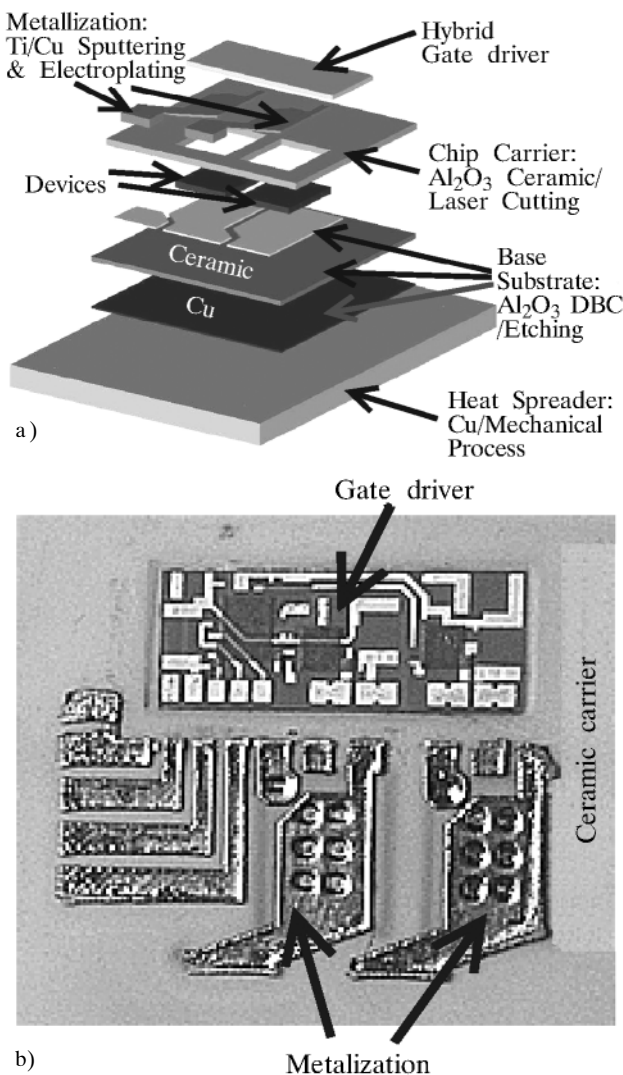| Parameter	Specification
DC blocking capacitance	>2 μF
Leakage inductance (ZVS range 50 % – 100 %)	2 μH
Magnetizing inductance	45 μH
Safety	UL 60950

a)

b)

Fig. 4 (a) Three-dimensional view of the active module using embedded power technology and (b) top view after metalization and assembly of gate driver

Several approaches have already been developed for integrated packaging of power modules. Previous work reported a MCM-D package for power applications [6], where a Si chip with one power transistor was used as a MCM-D substrate onto which the gate driver was mounted using flip-chip technology. A high level of integration was accom-

plished, but the power bus was still interconnected to the base substrate using bond wires. This also occurred in the IPM packaging technology, where power chips were mounted and interconnected with bond wires onto a high-density substrate [7], and the concepts of embedded chips and bump-less bonding were investigated for microelectronics packaging applications [8]. A planar device metalization technology was also developed in CPES, namely Embedded Power [9], which is a 3-D multilayer integrated packaging technology that sandwiches power bus structure and integrated circuitry. The principle of this technology is shown in Figure 4(a), while the metalization view of a power module is shown in Figure 4(b). Note that since one of the main structural elements of this planar technology is a ceramic chip carrier, the structure is suitable to mounting passive devices and advanced control functions in 3-D fashion directly on the carrier.

The DPS IPEM was designed to reduce the geometric footprint, while maintaining electrical and thermal performance [10]. A set of DPS IPEM models based on three-dimensional geometry was developed, including both electrical and thermal models. The electrical models were implemented in Maxwell Q3D for parameter extraction, while the thermal models were implemented in I-DEAS thermal.

Figure 5 and Table 4 summarize the results obtained from the design optimization. The first design was based on the wire bonding approach, while the other two were implemented with the embedded power technology. The proposed design achieved 35 % reduction of footprint area as compared to the wire bonding version, and approximately 9 % reduction in comparison to Generation II preliminary design shown in Figure 5(b). The planar interconnects reduced the structural inductance by a factor of 3 when compared to the wire bonding technology (Table 4 shows the largest structural packaging inductance only, but other paths also showed similar reduction ratio). However, the common-mode (CM) capacitance is increased by a factor of 5, as compared to the wire-bonding module. The parametric thermal study performed on the embedded power modules revealed that footprint reduction increases the temperature rise, ceramic thickness does

Table 4 **Design summary for DPS IPEM**

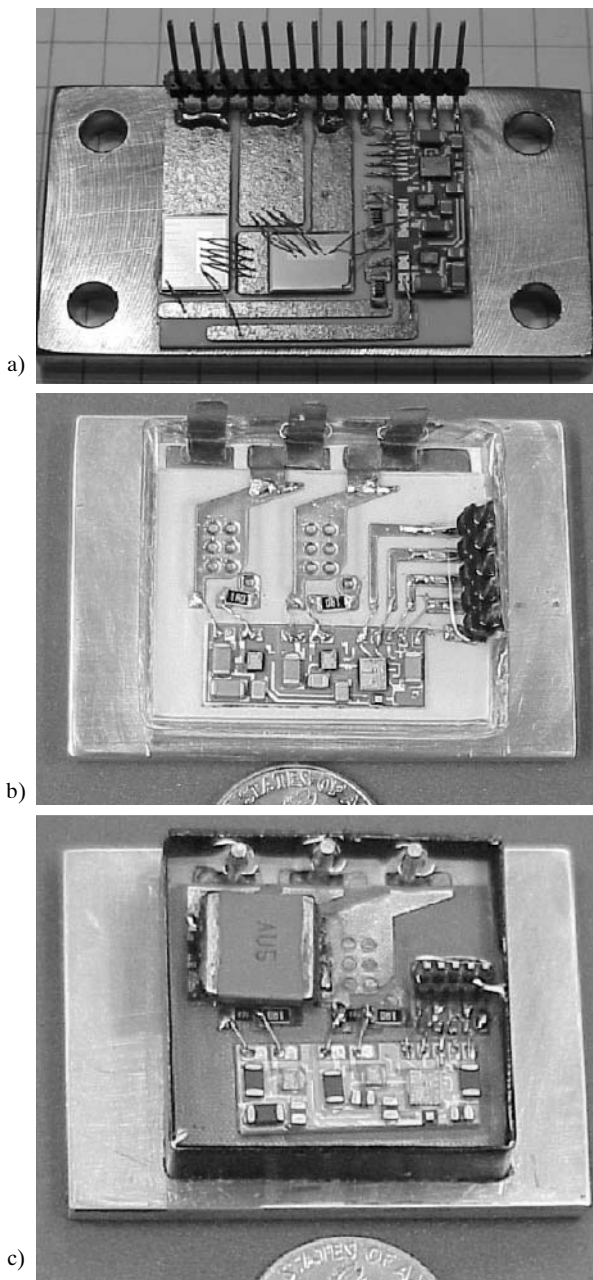| Property	Gen I	Gen II – Preliminary design	Gen II – Proposed design
Substrate Area (mm^2)	40×30	27×30	28.5×27.3
Inductance (nH)	10	3	3
Common-mode (CM) capacitance (pF)	4	60	20
Cm current at 200 kHz (A)	0.1	1.9	0.6
Temperature rise (C)	38	39	39

a)

b)

c)

Fig. 5 (a) Generation I IPEM using wire bonding, (b) generation II IPEM preliminary design using embedded power and (c) generation II IPEM proposed design also using embedded power

mendation. The proposed design recommendations based on cost and performance tradeoffs were 0.6 mm-thick Al_2O_3 ceramic substrate and 3 mm-thick heat spreader to improve thermal management and provide adequate mechanical stability. The next generation of the DPS IPEM will target at eliminating the heat spreader, while still maintaining electrical--thermo-mechanical performances similar to the proposed design shown in Figure 5(c).

2.2 Design and Implementation of Passive IPEMs Using Hybrid Winding Technology
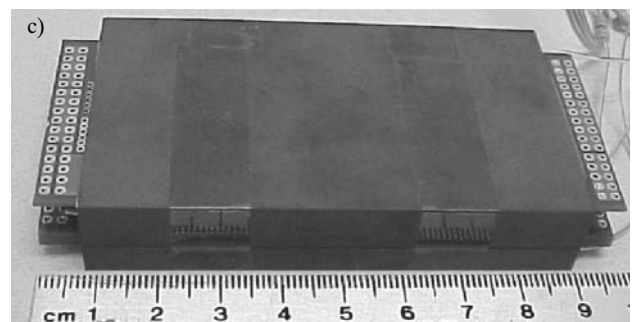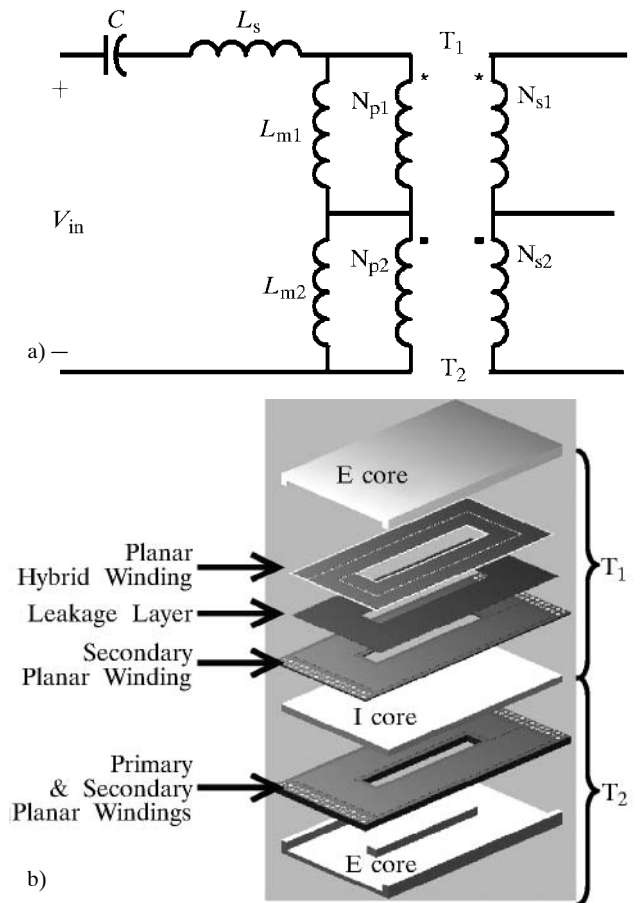

a)

b)

c)

Fig. 6 Components of the passive IPEM: (a) equivalent circuit, (b) exploded view of the passive IPEM, and (c) 1 kW prototype

not greatly affect the module thermal performance, and the heat spreader thickness improves thermal management [10]. An AlN substrate presented a slightly better thermal performance than Al_2O_3. Since ceramic thickness does not affect temperature rise largely, it should be chosen to minimize cost impacts as well as common-mode capacitance at the module level. Although the heat spreader improves thermal management, it has a detrimental effect if the thickness increases beyond the optimal recom-

For the design of the passive IPEM, constraints and parameters for all components were obtained from the system requirements and circuit analyses, as illustrated in Table 3. Because of the current doubler configuration, the structure of the passive IPEM has been realized by stacking two transformers, as illustrated in Figure 6(a). The transformers are built with two E-planar cores that share a common I core, as detailed in Figure 6(b). The DC blocking capacitor of the AHBC is implemented in transformer T_1 using the hybrid winding technology [11, 12]. This technology is implemented using Cu traces on both sides of the winding and a dielectric layer placed in the middle to enhance the capacitive component of that winding. The transformer T_2 is a conventional planar low-profile transformer. The inductances of the current doubler output filter are realized by the magnetizing inductances of both transformers. Figure 6(c) shows a picture of the passive IPEM implemented for the AHBC.

2.3 Experimental Results Using Active and Passive IPEMs

The AHBC configuration using the combined active and passive IPEMs is shown in Figure 7(a). The modular approach to system integration is clearly seen in this figure, where sub-assemblies are arranged and externally connected via a PCB placed on top. Figure 7(b) shows the waveforms measured at full load, in which V_{ds1} and V_{g1} are the waveforms related to the upper switch of the AHBC, while an efficiency comparison between the IPEM-based and discrete approaches are shown in Figure 7(c).

There are several advantages to integrated power electronics systems using the IPEM concept. Firstly, the modular approach can reduce the design and implementation time cycles, as well as simplify the assembling process. Secondly, the integration of functions in the form of IPEMs leads to improved usage of space, which increases power density and reduces profile of power electronics systems. For the example under consideration, the power density
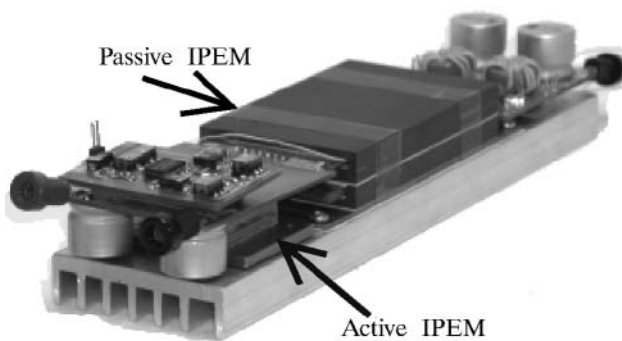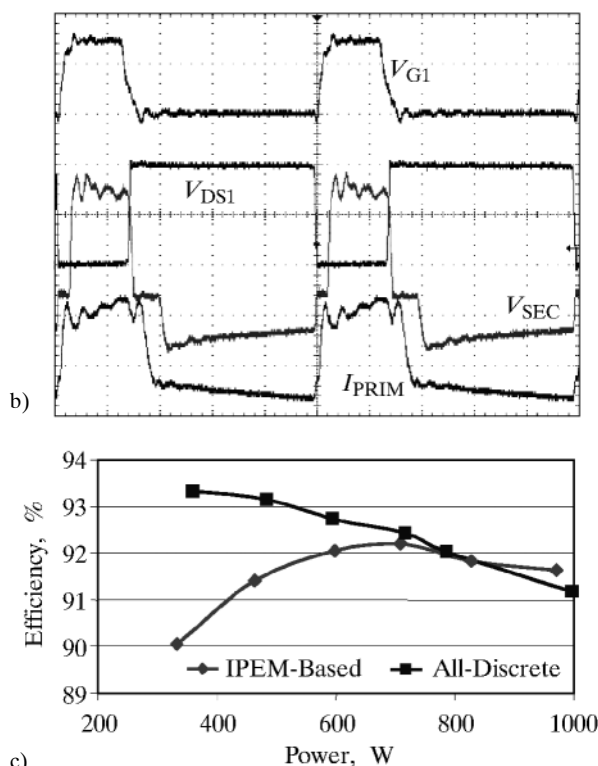

b)

c)

Fig. 7 (b) waveforms under test at 1 kW (V_{G1}: 10 V/div, V_{DS1}: 200 V/div, V_{SEC}: 100 V/div, I_{PRIM}: 20 A/div, time scale: 1 μs/div), and (c) efficiency

is increased by 2.8 times with respect to the discrete approach previously presented [13]. Thirdly, the reduction of interconnects at the system level due to integration certainly improves the system reliability, but this improvement has yet to be quantified. Fourthly, the reduction of structural packaging inductances leads to improved electrical performance. Reducing voltage ringing across the power switches allows increasing the switching frequency to further improve power density, as long as thermal de-rating is not implied.

3 TECHNOLOGY DEVELOPMENT FOR MOTOR DRIVES (MD)

Fans, pumps and compressors used in many industrial, commercial and residential applications, offer significant opportunities for energy savings, since they are generally powered by constant-speed drives rather than by more energy-efficient adjustable-speed drives. For example, heating, ventilation, and air conditioning (HVAC) systems consume more than 20 % of the total energy in the world, according to an EPRI report [14]. Projections indicate that replacing constant-speed drives in current HVAC systems with adjustable-speed drives could


Fig. 7 (a) View of the IPEM-based prototype

save 35 % of this energy. Although the benefits of adjustable speed control for many industrial, commercial and residential applications have been well documented, their success in large-scale production has been limited due to their higher purchase cost and perceived reliability limitations. However, effective means of integrating motor drives via the IPEM concept can achieve major improvements in cost, reliability, and performance. The major technology developments for motor drives are focused on active gate drivers [15] to control dv/dt and di/dt, motor drive IPEM implementation to help reduce cost [16], and the use of double-sided cooling to improve thermal management of the motor drive IPEM [5].

3.1 Active Gate Driver Control of dv/dt and di/dt

Figure 8 shows the equivalent model for the flexible dv/dt control topology applied to the gating circuit for an IGBT. A small external capacitor C_M is used to sense the switch's collector (C) terminal voltage derivative dv/dt and to generate current feedback to the gate (G) terminal for dv/dt control. The impact of the gate-collector capacitance on reducing the dv/dt of three-terminal switching devices is a well-understood phenomenon known as the Miller effect. This new approach introduces a dependent current source at the gate node whose current is proportional to the value of the capacitor current I_m achieving the same effect as changing the value of the external Miller capacitor C_M. In fact, the net effect of the control circuit can be interpreted as providing an electronically controlled Miller capacitance. The net current at the gate node contributed by the external Miller capacitor combined with the dependent source is $+I_m(1–A)$. Adjusting the value of A over a range, including positive and negative polarities, makes it possible to electronically increase or decrease the effective value of the total Miller capacitance [15].

Flexible control of the transistor di/dt during hard switching can be achieved by applying a dual
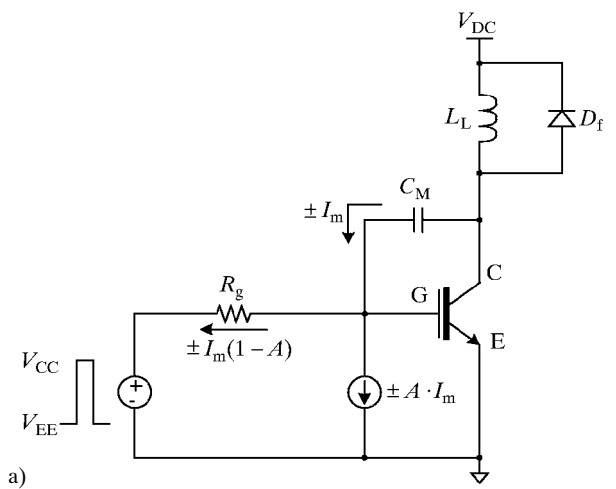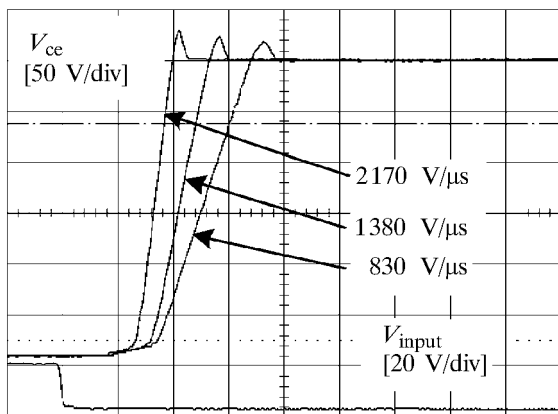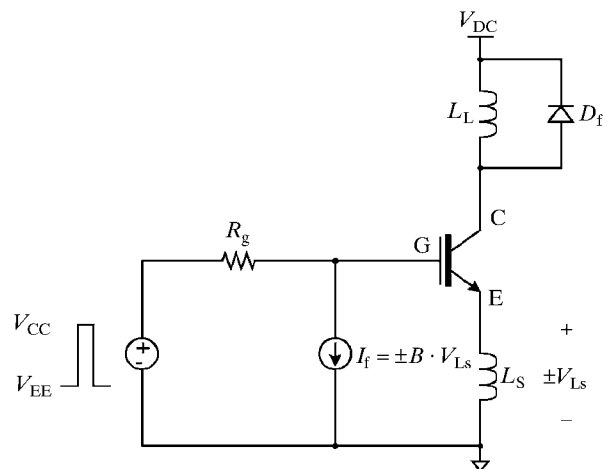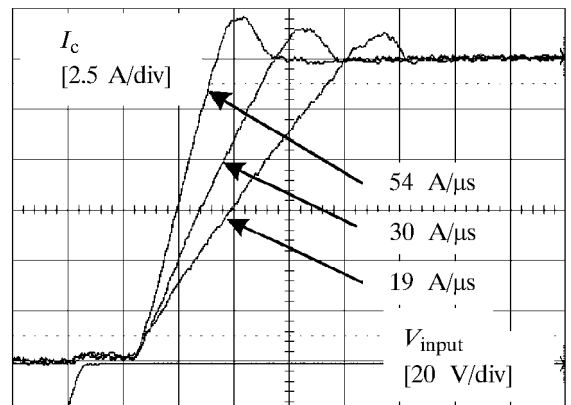

Fig. 8 (a) Equivalent circuit for flexible dv/dt control and (b) experimental test results for turn-off dv/dt control of a 1200 V/70 A IGBT operated at 300 V/15 A at three different dv/dt settings

Fig. 9 (a) Equivalent circuit for flexible di/dt control and (b) experimental test results for turn-on di/dt control of a 1200 V/70 A IGBT operated at 300 V/15 A at three different di/dt levels

version of the Miller capacitance used to control dv/dt. Figure 9(a) shows the equivalent model for the flexible di/dt control topology. The small external inductance L_s connected in series with the switch emitter is used to sense the di/dt value and generate feedback voltage for the control circuit. The value of this inductance can be chosen to be sufficiently small that it has negligible effect on the dominant time constant of the gate drive circuit. Using the same conceptual approach as in the dv/dt equivalent circuit shown in Figure 8(a), the measured di/dt is used to control a dependent current source that extracts current I_f from the switch's gate node. The value of this current is $+B \cdot V_{Ls}$, where $V_{Ls} = L_s \cdot$ di/dt and B is an adjustable gain analogous to A in the dv/dt control circuit. Changing B makes it possible to electronically adjust the value of di/dt, providing the same effect as changing the value of the external inductance L_s [15].

3.2 Flip-chip-on-Flex Packaging of Motor Drive IPEM

The flip-chip on flex motor drive IPEM is an extension of the successfully implemented lower-voltage (42 V) lower-power (500 watts) prototype unit for automotive applications [16]. In this previous demonstration, a single leg half-bridge was implemented with Si MOSFETs and Si PIN diodes. These units were constructed using commercially available flex (polyimide) substrates that are well accepted in automotive signal electronics systems for low-power applications.

Based upon this demonstration of a half-bridge circuit and companion evaluation of flex high voltage capability, a higher power (1–5 kilowatt), higher-voltage (600–1200 V) power flex circuit has been designed and is being implemented for the motor drive IPEM using Si IGBTs and Si PIN diodes. The first prototype of this circuit is shown in Figure 10, which is implemented in non-commercial flex circuitry. Commercial IGBTs and PIN rectifiers with moderate switching speed have been used (IRG4PC50W and HFA15TB60S, respectively). The electrical performance of this prototype indicates that full voltage and current can be handled in a small footprint. The switching waveforms of this half-bridge IGBT/PIN rectifier module are shown in Figure 11. They were obtained with a load consisting of an inductor of 200 μH connected in series with a resistor of 1.60 Ω. A small (<10 %) voltage overshoot can be observed in the turn-off waveforms shown in Figure 11(a), while significant diode reverse recovery current is apparent in the turn-on waveforms illustrated in Figure 11(b).

A power flex test vehicle designed using commercial flex circuitry for testing several alternative phase-leg and bridge physical layouts is shown in
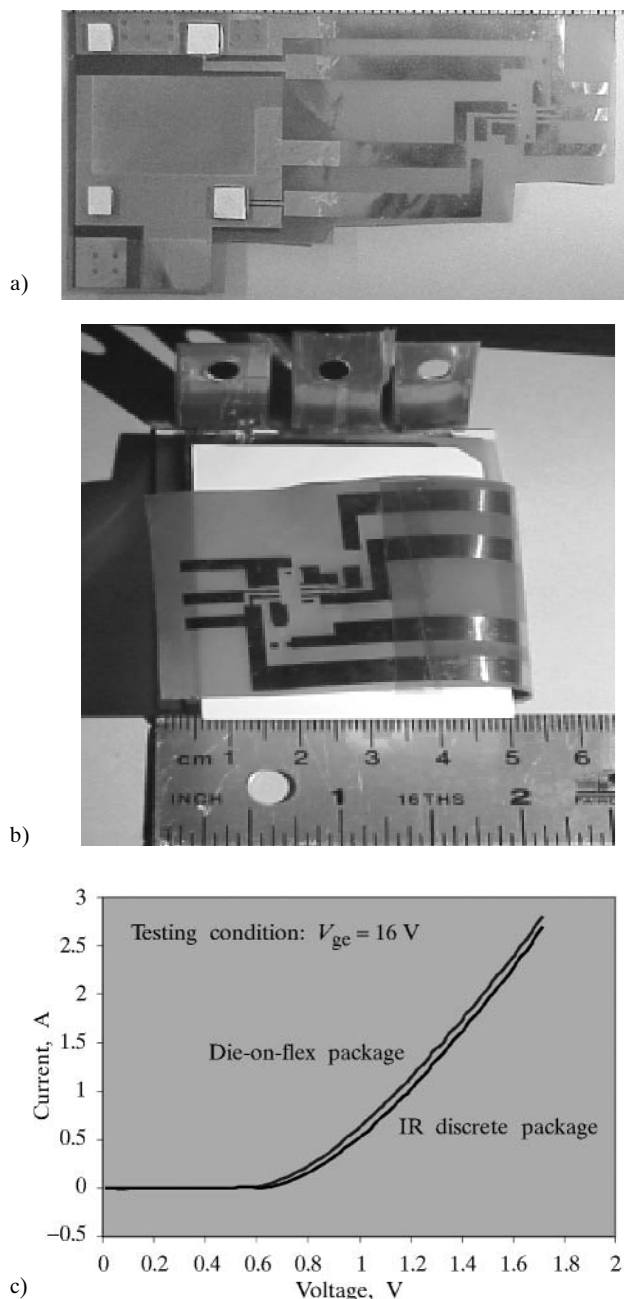

a)

b)

c)

Fig. 10 Flex-circuit motor drive IPEM generation 1 prototype: (a) flip-chip IGBT die on flex with under-fill, (b) assembled IGBT IPEM, and (c) IGBT device characteristics

Figure 12. A full complement of test structures is included and is presently under evaluation. However, based upon the flip-chip on flex results to date [16], the low-to-medium power electronics applications can be implemented with low parasitics and high power density. Thermal design considerations will be a factor in medium-to-high power applications.
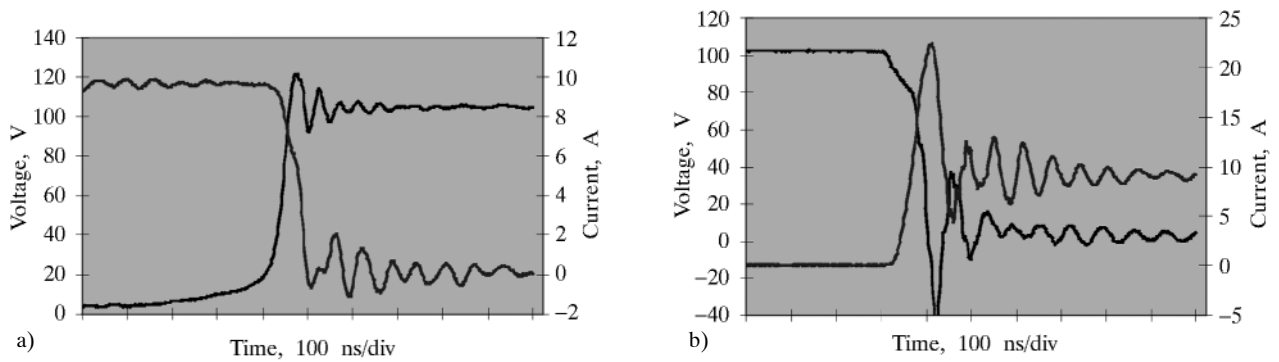
Fig. 11 Flex-circuit Generation 1 prototype electrical performance: (a) high side IGBT switch turn off waveform and (b) high side IGBT module switch turn on waveform
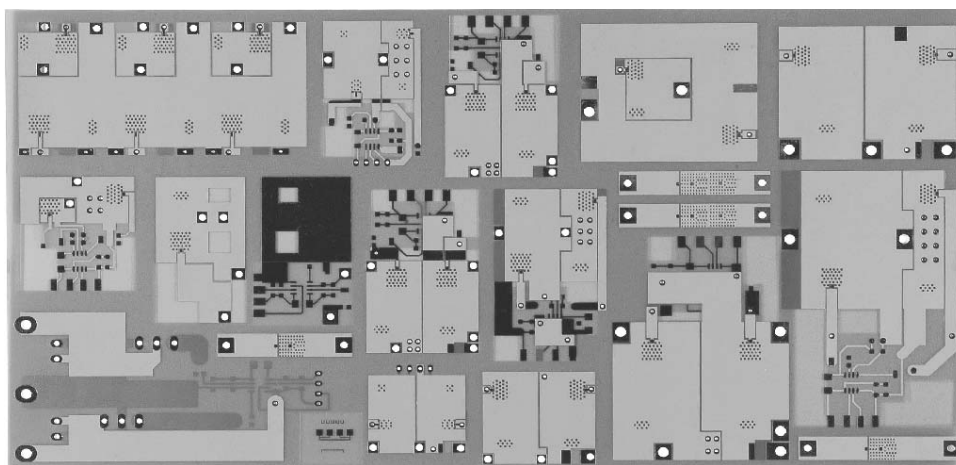

Fig. 12 Flex circuit Generation 2 test structures (Sheldahl standard Novaflex® technology, with either photo-imaged solder mask or film overlay solder mask. Double-sided 35 μm Cu and 50 μm dielectric substrate).

3.3 Double-Sided Cooling of MD IPEM Using Miniature Heat Pipes

IPEM planar interconnect technologies offer opportunities for improved thermal management by allowing thermal access to the upper side of the power devices [5], as illustrated in Figure 13(a).

Double-sided cooling of IPEMs has the potential to allow increased chip power dissipation and/or to improve IPEM reliability by lowering the junction operating temperature. To evaluate the effectiveness of
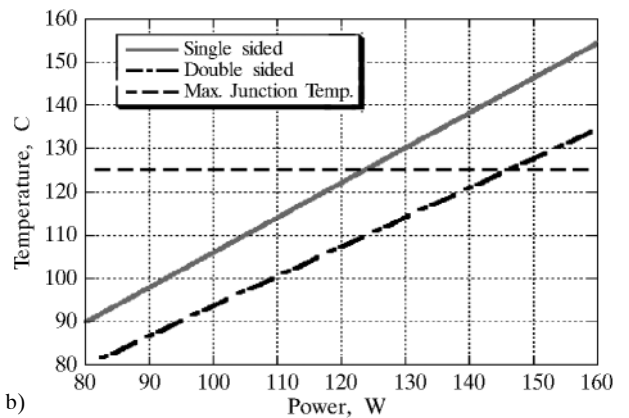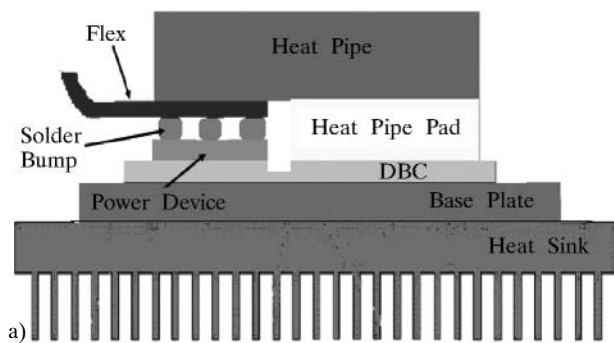

Fig. 13 (a) Double-sided cooling of flex packaging using heat pipe and (b) temperature reduction
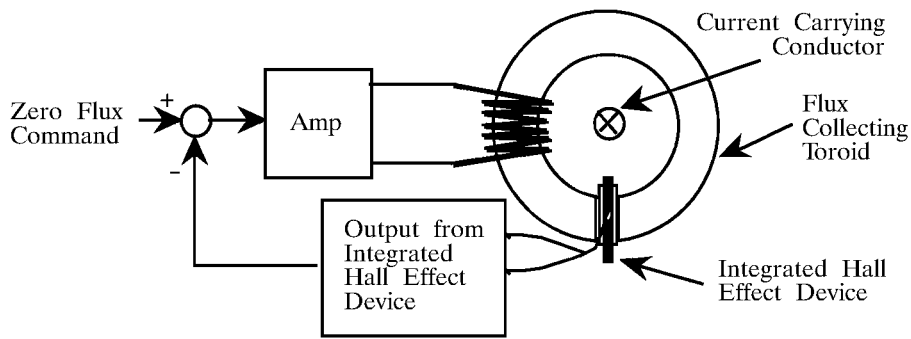
Fig. 14 The active null-regulated, Hall effect current sensor with flux concentrating toroid

heat pipes for removing heat from the top side of the power module, a nominal case was analyzed with ANSYS™ finite element software in both single-sided and double-sided configurations. The results are illustrated in Figure 13(b), which shows that 18 % more dissipation can be tolerated for double-sided cooling for the same maximum junction temperature. Alternatively, a 12 C reduction in the maximum temperature is observed with double-sided cooling compared to the single-sided case for the same power dissipation (100 W). This corresponds to a 15 % decrease in the maximum temperature rise relative to ambient temperature. For this test configuration, twenty-eight percent of the heat is removed from the upper side of the IPEM with double-sided cooling.

4 INTEGRATION OF CURRENT SENSORS IN IPEMS

Benchmarking studies focusing on reliability and cost of power electronic systems converged on the current sensor as a major opportunity for improvement via integration. The baseline technology is the Hall effect detector with a flux concentration toroidal core used in either the simple open loop form or in an active null regulated flux form as shown in Figure 14.

The current sensor integration objectives are to reduce the interconnections at both signal and power levels, reduce the parasitics in the power flow path, and reduce the number of components, while maintaining the accuracy, range, bandwidth and isolation properties of the baseline technology. To achieve
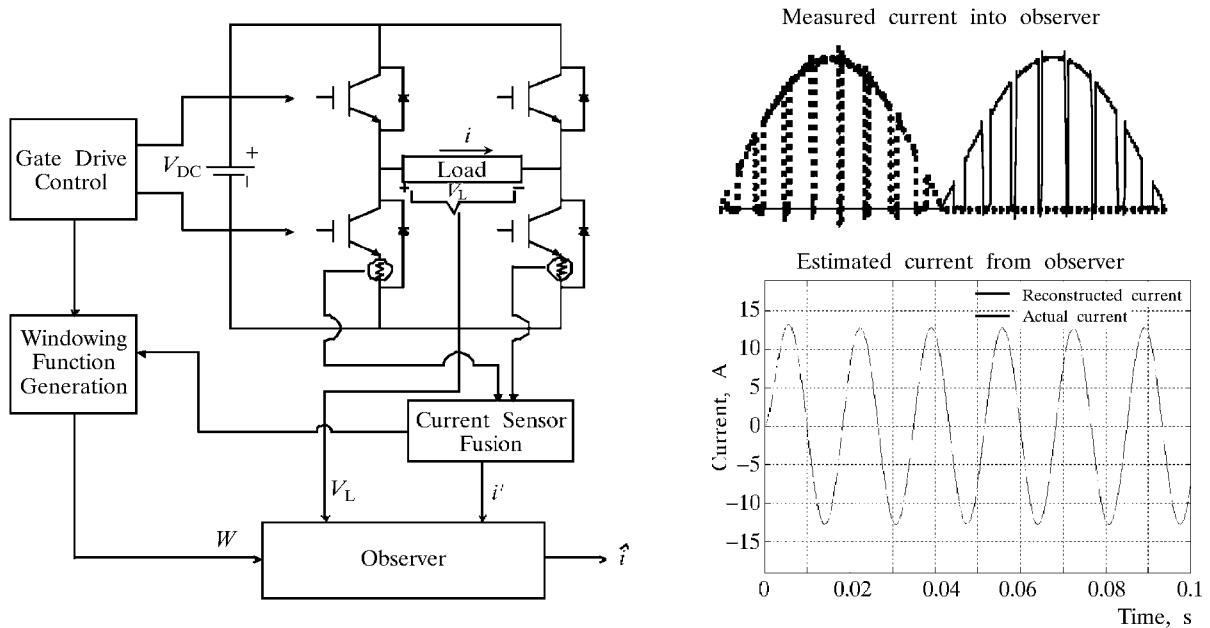

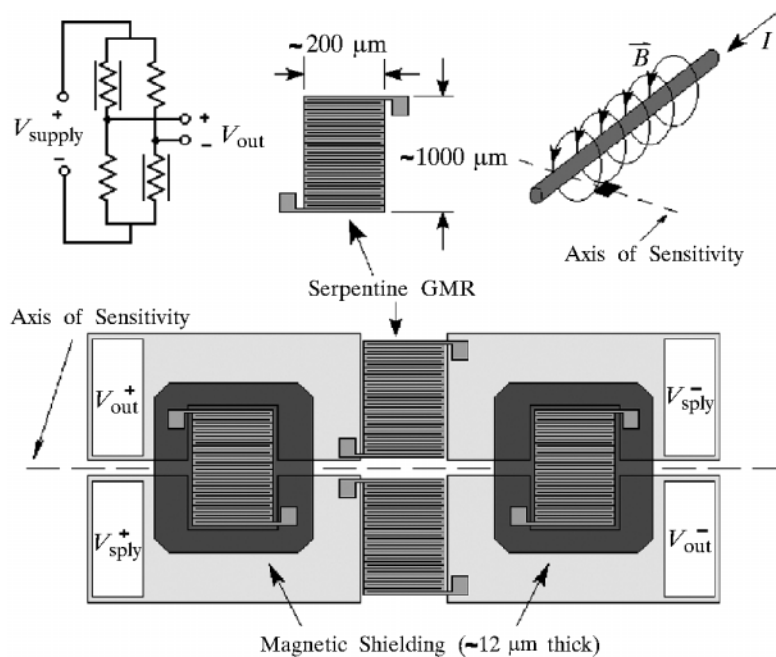Fig. 15 Direct sensing (shunt or pilot current) with integrated current observer

Fig. 16 GMR detectors in mean field-sensing configuration with bridge-based temperature decoupling

this objective, candidate technologies were evaluated, bench test beds were developed to evaluate alternative technologies and develop useful design approaches, as discussed in the following subsection.

4.1 Integrated current sensing alternatives

Current sensing can be broken down into two basic approaches: direct and magnetic field-based. The direct approach has two general forms: shunts and pilot current devices. Shunts generally use an in-line resistive substrate with Kelvin terminal voltage sensing. This approach lacks galvanic isolation but is very inexpensive and has the potential to be easily integrated into IPEM. The lack of galvanic isolation can be substantially mitigated by using only the lower bus location on each totem pole switch/antiparallel diode pair. Pilot current devices effectively channel the current from one of the active device cells to an active null-regulated (virtual ground) circuit. If the pilot device cell is well matched to the other cells, then this approach allows a highly integrated sensing method, albeit with compromises in galvanic isolation. In both direct sensing cases, a current observer is used to estimate the phase current. The observer bandwidth is a significant challenge. These approaches are shown conceptually in Figure 15 and are part of the ongoing CPES research effort on integrated current sensors.

The magnetic field-based approaches depend on placing materials, which have physical properties sensitive to magnetic fields, in magnetic fields produced by conductors. Such field detecting methods inherently offer some form of galvanic isolation. The classical Hall effect magnetic flux detector is one such device. However, its low sensitivity implies use of flux-concentrating cores, which yields bulky sensors not amenable to integrated packaging. By comparison, giant magnetoresistive (GMR) materials
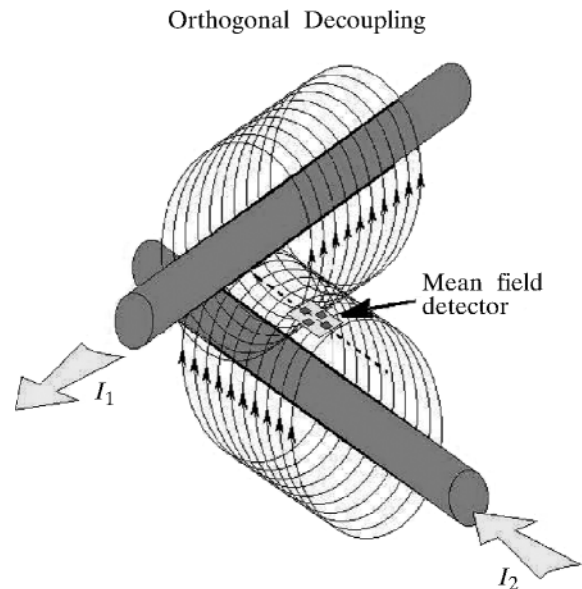

Fig. 17 Decoupling fields via geometric placement of GMR mean field detectors
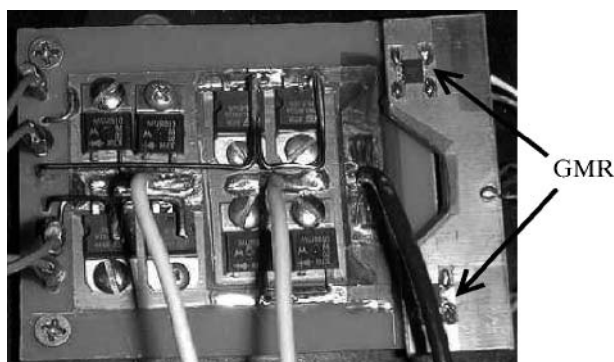
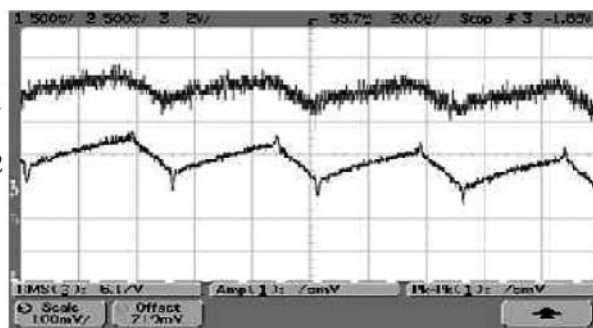*Fig. 18 IPEM totem pole with integrated GMR mean field detector bridges*

Fig. 19 Current measurement performance of IPEM integrated GMR detectors: (1) signal from scope current probe instrumentation, and (2) signal from GMR field detector summation

have very high sensitivity, which portends the potential for direct IPEM integration without core material [17]. Magneto-optical materials also offer such potential, but due to their more modest field sensitivity, the relative bulk volume required does not easily allow integration in IPEMs. Figure 16 shows a »sandwich« GMR detector in a bridge form [18].

The most challenging issue in use of such field detectors is the 3-D geometric design to decouple unwanted fields from the desired field without resorting to core materials [19]. Figure 17 shows the general problem and Figure 18 shows one approach used in CPES bench testing. The sensed load current result is shown in Figure 19. The major ongoing issues in the CPES IPEM current sensor integration effort are focusing on 3-D design of the IPEM with integrated GMR field detectors [20] and integrated shunt (or pilot current) sensors with hardware current observers. Both technologies are potential solutions to the interconnection and parasi-

tics objectives. Primary performance issues are signal-to-noise ratio (S/N), and resolution-to-range ratio (R/R), cross-coupled physical effects, and bandwidth.

5 DEVELOPMENT OF DEVICES FOR DPS AND MD APPLICATIONS

The scope of the device development within CPES is on the demonstration of novel discrete and integratable devices to facilitate IPEM implementation and to relief integrated packaging requirements, as well as to enhance performance for DPS and MD applications.

5.1 High-Voltage Si Trench Rectifiers

Poor reverse recovery characteristics of rectifiers limits switching frequency and stress the power switches in the power electronics circuits. To overcome this problem, a high-voltage trench sidewall oxide-merged pin/Schottky (TSOX-MPS) rectifier [21, 22], as shown in Figure 20(a), was proposed to
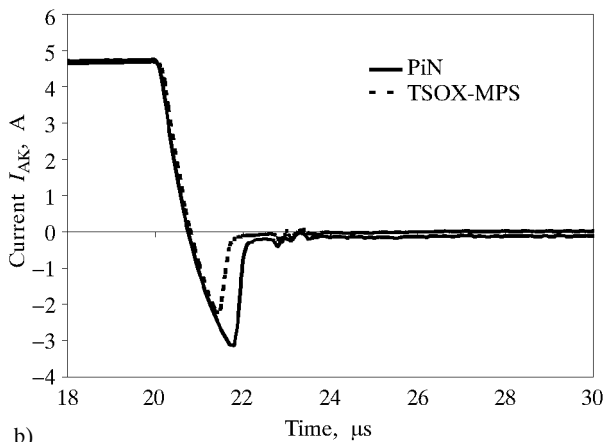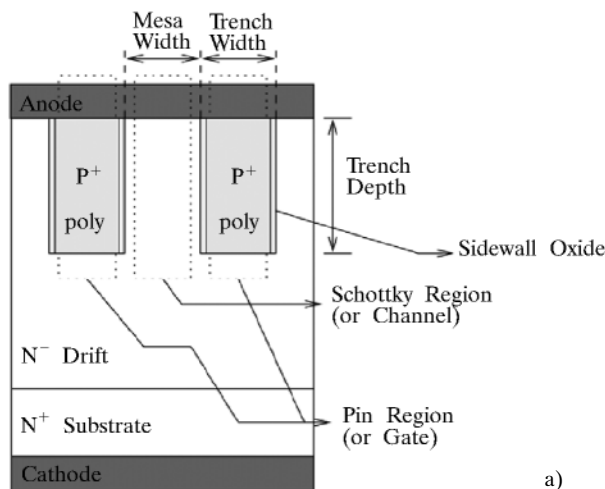

Fig. 20 (a) Schematic cross-section of high-voltage TSOX-MPS rectifier and (b) reverse recovery characteristics of 600 V TSOX-MPS rectifier and conventional pin junction rectifier

reduce both I_{RP} and Q_{rr}. This hybrid rectifier is actually a junction rectifier with adjacent Schottky regions separated with sidewall spacers. The oxide spacers not only suppress the reverse leakage current but also prevent lateral boron diffusion, thus allowing a more precise control of the Schottky region widths. Figure 20(b) shows the reverse recovery current waveform for this trench rectifier at room temperature. The reverse peak current and the reverse recovery charge are 30 % and 50 % smaller, respectively, than those from the conventional pin junction rectifier. The Si trench rectifier discussed in this section is suitable to improve efficiency for PFC applications.

5.2 Integrated Si DMOSFET/MPS Rectifier

The switching performance of the vertical DMOSFET is related to the reverse recovery characteristics of the anti-parallel diode. The anti-parallel diode of DMOSFETs has poor reverse recovery characteristics because of the high minority carrier lifetime in the drift region, which limits the switching capability of the power DMOSFET [23]. Smal-

ler reverse recovery charge and faster charge removal from the diode is necessary for faster switching and reduced power loss. To minimize the problems with the reverse recovery, a new device structure has been developed that integrates an anti-parallel merged PIN Schottky (MPS) rectifier within the conventional DMOSFET. The structure of the integrated DMOSFET/MPS rectifier is shown in Figure 21(a). The metal electrode from the n+-source region of the DMOSFET is extended to the surface n-drift region. The metal selected has the appropriate work function so that a Schottky contact is formed with the n-drift region while ohmic contacts are formed with the p-body and n+-source regions, thus resulting in a MPS structure [24]. The design and optimization of the 500 V DMOSFET/MPS was performed in MEDICI™. The new device exhibits about 30 % decrease in reverse peak current (I_{RP}) and minority carrier stored charge (Q_{rr}) [25, 26], as shown in Figure 21(b).

5.3 Integrated Si IGBT/MPS Rectifier

IGBTs are extensively used in power electronic circuits for motor drive applications. The absence of an integral diode in the IGBT structure requires the use of discrete power rectifiers, thus increasing the parts-count in the circuit and adding cost, as well as complexity. Furthermore, the interconnection of discrete devices aggravates the overall package parasitics. To overcome this drawback, research has been conducted to explore monolithic integration of the IGBT with the anti-parallel rectifier. Such integration is crucial to facilitate packaging of devices for motor drive applications.

Fig. 22 Die outlines of (a) conventional IGBT and (b) monolithic IGBT/MPS rectifier device

In the approach taken, the anti-parallel MPS rectifier is monolithically integrated into the IGBT die by the allocation of a portion of the total silicon area for the realization of the rectifier. The die-outlines of the conventional IGBT and the integrated IGBT/MPS device are illustrated in Figure 22. The size of the IGBT/MPS die has to be scaled up by about 30 %, while both the IGBT and the MPS devices have to be realized in an area ratio of 3:1.
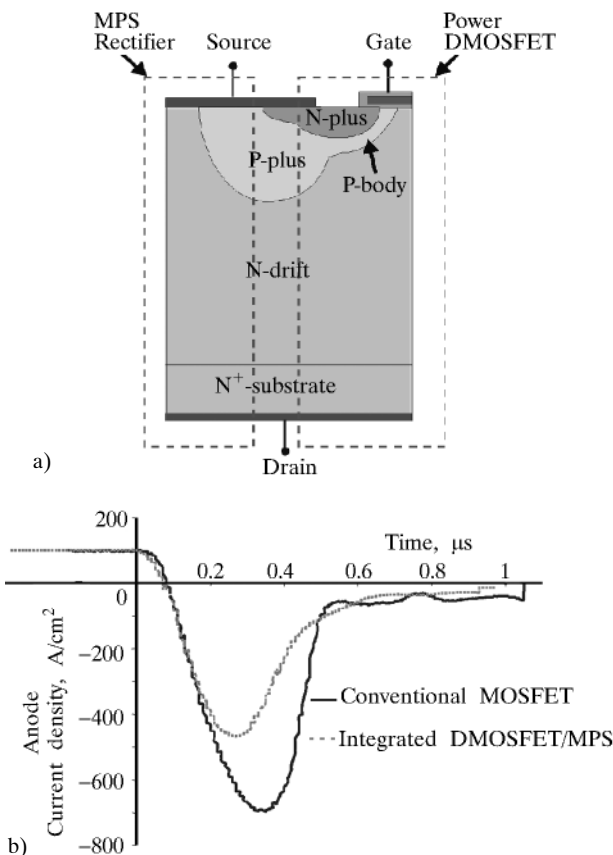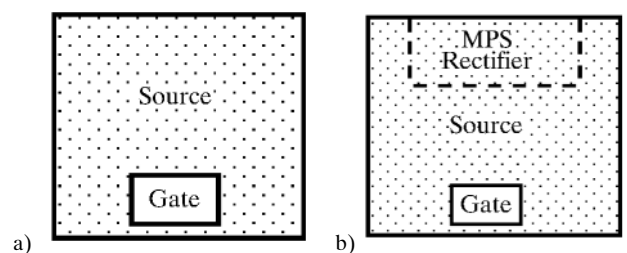

Fig. 21 (a) Cross section of the integrated DMOSFET/MPS power device and (b) Experimental reverse recovery of anti-parallel rectifiers in DMOSFET and DMOSFET/MPS at 100 C

5.4 Integratable, 80 V Si Lateral Trench MOSFETs

Lateral power MOSFETs have been the key components in power ICs used in portable power management products, such as PC peripheral and automotive applications. It has been shown that a trench quasi-vertical, RESURF MOSFET structure would be very competitive when compared to the conventional lateral silicon RESURF MOSFETs, particularly in the higher voltages [29].

The structure of the Lateral Trench MOSFET with an epi RESURF region is shown in Figure 23. The n-epi region on top of the p-substrate constitutes the RESURF region that supports the applied voltage. Since the channel length of this MOSFET is determined by the vertical diffusion of the p-base and n+ source, a deep submicron channel length can be achieved without the use of deep submicron photolithography. Simulation results indicate a low specific-on-resistance of about 0.8 mΩ-cm^2 for a blocking voltage of 80 V. Besides, a reduction of 45 % in the gate charge is possible, which translates into an equivalent reduction in the $R_{on} \times Q_g$ product, and thus improving the device's figure of merit.
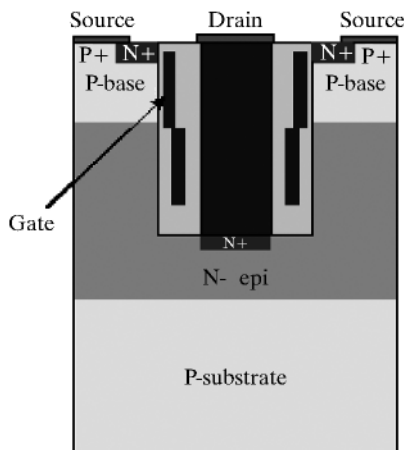

Fig. 24 Integrated thermal and electrical analyses

other software tools. The user inputs the solid-body geometry and material data describing the IPEM layout into the mechanical CAD software such as I-DEAS, which has the capability of exporting the

Fig. 23 Lateral trench MOSFET – 2002 patent disclosure by T. P Chow

6 INTEGRATED DESIGN METHODOLOGY

A multidisciplinary approach to materials optimization, electronic packaging techniques and thermal management is necessary to realize an integrated system. The entire procedure for designing an IPEM, including layout, fabrication and systems applications necessitates integration of CAD tools [29]. An example of integrated analysis used to optimize the design of the active IPEM can be seen in the flowchart shown in Figure 24. In this example, a software tool called iSIGHT is used to integrate and manage the data exchange between all
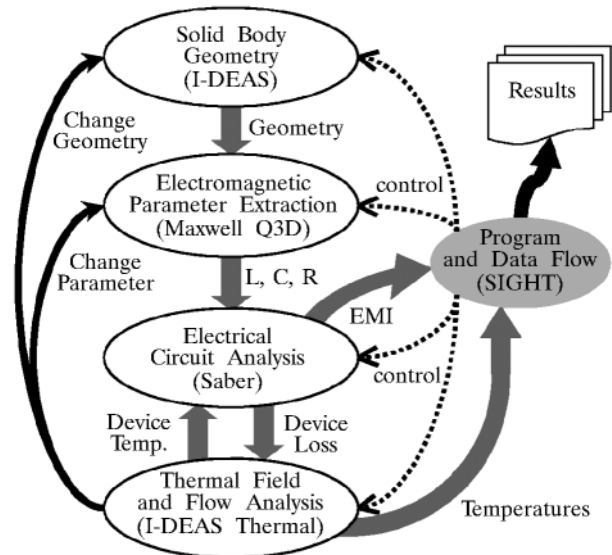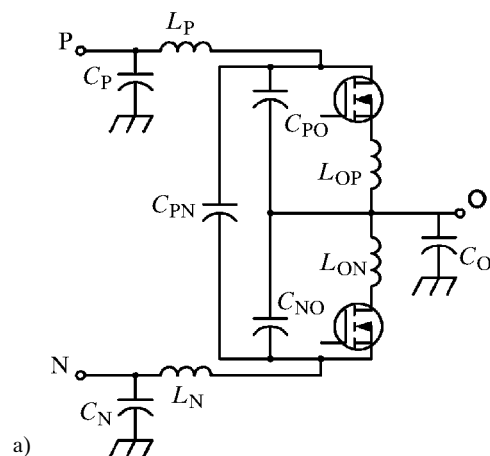

Fig. 25 (a) Partial equivalent circuit of the active IPEM and (b) thermal map of the IPEM

geometry in a number of format files and an optional open architectural library that facilitates software integration. The same geometry and material data is shared by both the electromagnetic field and thermal analysis software packages. The parasitic parameters are extracted by Ansoft Maxwell Q3D and transferred as an equivalent circuit, as shown in Figure 25(a), to the circuit simulation software such as Saber to perform transient, EMI and loss analyses. I-DEAS performs the thermal analysis to produce the temperature map within the IPEM, as shown in Figure 25(c). The interaction between Saber and I-DEAS is managed by iSIGHT until the temperature and device losses achieve convergence. This kind of analysis enables the designer to evaluate the tradeoffs between the electrical and thermal performance at the component and system levels. The user can change the relative layout, size, and material of the structural parts, or even select different heat sink sizes or fluid flows, to achieve satisfactory results [31].

7 CONCLUSION

Advancements in semiconductor technologies have been the major driving force for improving converter size, weight, and cost; mostly due to increase in switching frequency. However, for some high frequency applications, fundamental limits in packaging are being reached. An order of magnitude increase in switching frequency will require substantial reduction in structural inductances associated with device and system-level packaging. Therefore, to provide further improvements in performance, reliability, and cost, it is essential to develop novel integration and packaging technologies in the form of Integrated Power Electronics Modules (IPEMs), which must enable the integration of all the converter functions and not only concentrate on the switching stage.

These novel integration and packaging technologies, in conjunction with suitable devices, sensors and integrated design tools used to exploit the physical properties of available materials have been the focus of the CPES research program. The role of the technologies mentioned above in the IPEM concept is key to achieving high levels of integration and to enable significant growth of the power electronics industry. While technology roadblocks have been found to date, it is evident that further innovations will be necessary as power densities increase. The impacts of systems integration via IPEMs will enable a rapid growth of power electronics applications with reduced costs and design cycles that can be compared to the impacts in computer applications brought up by the VLSI circuit technology.

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Integralni pristup sustavima energetske elektronike. Današnji sustavi energetske elektronike se obično proizvode iz nestandardnih dijelova. Posljedica toga je laboratorijska proizvodnja elektroničkih učinskih pretvarača, povećani troškovi i smanjena pouzdanost. Jedan od mogućih načina prevladavanja ovih poteškoća jest integralni pristup projektiranju i proizvodnji sustava energetske elektronike. Posebice se razmatraju tehnologije razvijene za integraciju učinskih krugova i motora. Ove tehnologije uključuju postupke planarne metalizacije za izbjegavanje žičanih vodova, integraciju pasivnih dijelova učinskih krugova, integraciju strujnih senzora, te razvoj takvih poluvodičkih komponenata koje olakšavaju integraciju i poboljšavaju karakteristike uređaja. Pri projektiranju, zbog multidisciplinarnih aspekata integriranih sustava, treba primijeniti nužne CAD alate. Razvoj integriranih modula elektroničkih učinskih pretvarača (engl. *integrated power electronics modules*, IPEM) ilustriran je na dvije primjene: (1) istosmjerni pretvarač snage 1 kW u asimetričnom polumosnom spoju i (2) elektromotorni pogon snage 1 … 3 kW za grijanje, ventilaciju i klimatizaciju (engl. *heating, ventilation and air conditioning*, HVAC). Na IPEM-u objašnjeni su projektantski i tehnološki kompromisi električkog i toplinskog projekta.

Ključne riječi: konstrukcija elektroničkih sklopova, učinski integrirani krugovi, učinske poluvodičke komponente, senzori, metode integralnog projektiranja

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