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Capacitor-less Buck Converter

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Low-power switched-mode power supply converters are used in applications where size and efficiency are critical. The buck converter size can be reduced by elimination of the bulky filter capacitor. The filtering function of this capacitor can be replaced by an output current ripple compensation circuit. The compensating circuit is applied, based on inductor current measurement and linear amplifier. The proposed compensating algorithm is investigated theoretically by simulation, and verified experimentally.

Key words: dc-dc buck converter, low power, inductor current ripple compensation

Silazni DC-DC pretvarač bez izlaznog kondenzatora. DC-DC pretvarači malih snaga se koriste u uredjajima gdje su važni dimenzije i učinkovitost. Dimenzije pretvarača se mogu smanjiti sa izostavljanjem filtarskog kondenzatora. Umjesto sa kondenzatorom se funkcija gladjenja izlaznog napona može izvesti sa kompenzacijom valovitosti struje zavojnice. Za kompenzaciju valovitosti struje je potrebno mjeriti trenutnu vrijednost struje induktora koja se preko obrade u linearnom pojačalu dodaje u protifazi struji zavojnice. Predloženi kompenzacijski postupak je istraživan teoretski te verificirani simulacijski i eksperimentalno.

Ključne riječi: dc-dc silazni pretvarač, mala snaga, kompenzacija valovitosti struje zavojnice

1 INTRODUCTION

Switched-mode power converters (SMPCs) have won the battle over linear power converters (LPCs) because of their high efficiency and small volume. Nevertheless, because traditional approaches for SMPC implementation rely on discrete components, many modern concepts have joined and integrated diverse functionality in to a single integrated power module (IPEM) [1], [2]. There are tremendous efforts being made to replace physical elements with 'smart' algorithms and approaches, for example, it is far more economically justified to improve the electromagnetic compatibility (EMC) of an SMPC using modulation strategy, than with costly and bulky EMI filters [3], [4], [5], [6]. Lower output voltage, higher output current, and smaller output voltage ripple requirements have greatly increased the difficulty of the power supply design. An improved topology of the inductor switching dc-dc converters is shown in [7], [8].

An output filter for reducing converter output voltage ripple is an extremely important part of the buck converter, and often accounts for a significant proportion of its size and costs [9], [10]. The bulkiness of the output LC filter, when output voltage ripple is taken into account, can be overcome by increasing the switching frequency or applying an active power filter. Switching frequency increase is inevitability related to higher switching losses. Regarding to this an interesting approach, was recently published in [11] where the authors describes special dc-dc converter structure capable to reduce the output voltage ripple. Some approaches in the field of audio amplifiers combine the functionalities of LPC and SMPC [12], [13] in order to maintain good device efficiency and low total harmonic distortion (THD).

The following text presents an approach for eliminating the buck converter output capacitor. Such an approach minimizes the converter's volume and is suitable for System-on-Chip (SoC) or System-in-Package (SiP) applications, where the coil remains the only external component necessary for proper system functionality. The inductor current ripple compensation method is proposed, by focusing on the hybrid structured SMPC and LPC. The proposed current ripple compensating algorithm requires closed control loop [13], [14] and [15] in order to keep converter efficiency on the reasonable level. The operation of the proposed circuit is theoretically investigated and verified with simulations and experiments.

2 THE BUCK CONVERTER'S CURRENT AND VOLTAGE RIPPLE

The basic structure of buck converter is shown in Fig. 1 (a). The inductor current ripple (Δi_L) for the buck con-

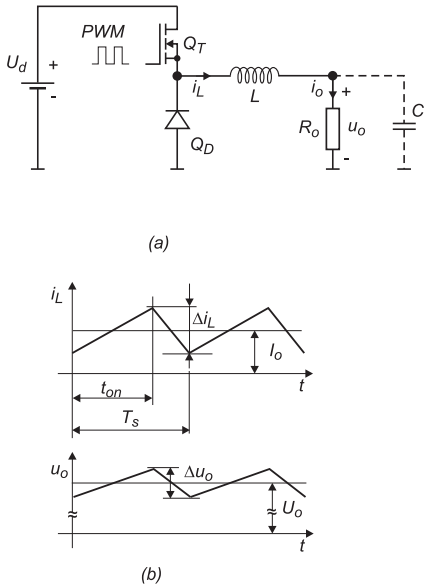

Fig. 1. (a) Buck converter; (b) Inductor current and output voltage ripples (when C is not applied)

verter in continuous current mode operation without filter capacitor can be estimated by:

$$\begin{aligned}\Delta i_L &= \frac{U_d}{R_o}\left(1-e^{\frac{t_{on}}{\tau}}\right)\\ &= \frac{U_d}{R_o}\left(1-e^{\frac{\Delta_p T_s}{\tau}}\right)\end{aligned} \quad (1)$$

where U_d is the input voltage, t_{on} is the switch-on transistor time, $\tau = L/R_o$, T_s is the switching period, Δ_p is the duty-cycle (t_{on}/T_s), L is the inductance, and R_o is the load resistance. Fig. 1 (b) shows the inductor current (or the converter output current $i_L = i_o$) and output voltage waveform when the filter capacitor is not applied. The voltage ripple (Δu_o) can be expressed by:

$$\Delta u_o = R_o \Delta i_L \quad (2)$$

In order to create output voltage ripple in (2), the load-independent, the current ripple Δi_O must be appropriately reduced to almost zero.

3 INDUCTOR CURRENT RIPPLE COMPENSATION PRINCIPLE

In a steady state the inductor current i_L (Fig. 2 (a)) can be described as the sum of the DC current component ($I_L = I_o$) and the AC current component ($i_{RIPPLE}(t)$), as indicated in Fig. 2 (b).

$$i_L(t) = I_o + i_{RIPPLE}(t) \quad (3)$$

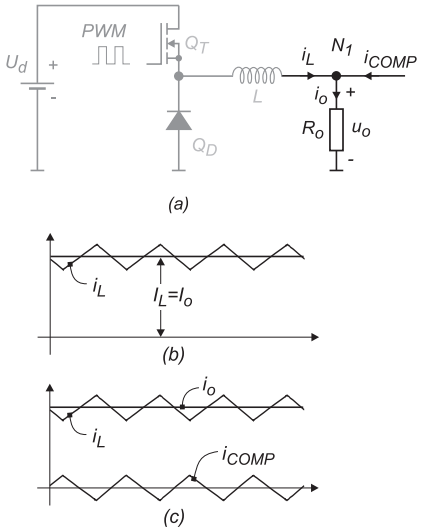

Fig. 2. a) Circuit node consideration; (b) Inductor current; (c) node N_1 currents: i_L, i_o, and i_{COMP}

where the DC output current is evaluated by $I_o = U_o/R_o = \Delta_p U_d/R_o$, where U_o is the average value of u_o. According to the Kirchhoff current law, the converter output current i_o can be expressed by:

$$i_o(t) = i_L(t) + i_{COMP}(t) \quad (4)$$

And by substituting (3) into (4), yields:

$$i_o(t) = I_o + i_{RIPPLE}(t) + i_{COMP}(t) \quad (5)$$

In order to eliminate current ripple the instantaneous current i_o must be equal to its average value I_o, so from (5) it follows that:

$$i_{COMP}(t) = -i_{RIPPLE}(t) \quad (6)$$

It is evident from (6), that the compensating current $i_{COMP}(t)$ must have the same magnitude as $i_{RIPPLE}(t)$ and must be phase-shifted by 180^o, as is shown in Fig. 2 (c).

4 OUTPUT CURRENT-RIPPLE COMPENSATION CIRCUIT

The hybrid-structured converter, consisting of a buck converter and linear amplifier is shown in Fig. 3 (a). Linear amplification is implemented, using a high-voltage/high-current operational amplifier. The shunt resistor R_S, operational amplifier, and resistor R_{COMP} form a current-controlled current source. Measurement of the inductor current ripple is obtained from sensing resistor R_S and by using a filter made of capacitor C_1 and other elements, accompanied by the operational amplifier indicated by A.

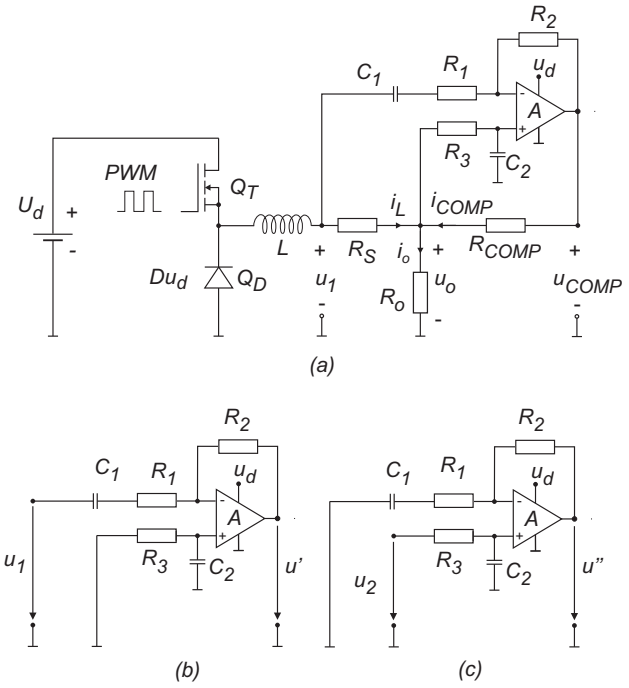

Fig. 3. (a) Hybrid structured buck converter; (b) Inverting amplifier; (c) non-inverting amplifier

The voltage $u_{COMP}(t)$ appears on the amplifier output and generates the compensation current $i_{COMP}(t)$. The compensation voltage $u_{COMP}(t)$ is calculated by the use of the superposition principle.

$$u_{COMP}(t) = u'(t) + u''(t) \tag{7}$$

Therefore, the filter-amplifier circuit can be solved in two steps, as shown in Fig. 3 (b), (c). For further analysis (7) is transformed in the s domain. The output voltages $u'(s)$, and $u''(s)$ are calculated separately for each circuit, as follows:

$$u'(s) = \frac{-sR_2C_1}{sR_1C_1 + 1} u_1(s) \tag{8}$$

$$u''(s) = \frac{1}{sR_3C_2 + 1} \left(1 + \frac{sR_2C_1}{sR_1C_1 + 1}\right) u_2(s) \tag{9}$$

and according to (7) the voltage $u_{COMP}(s)$ is expressed by:

$$u_{COMP}(s) = \frac{u_2(s)(sa_1 + 1) - u_1(s)\left(s^2a_2 + sa_3\right)}{s^2b_1 + sb_2 + 1} \tag{10}$$

where $a_1 = C_1(R_1 + R_2)$, $a_2 = R_2R_3C_1C_2$, $a_3 = R_2C_1$, $b_1 = R_1R_3C_1C_2$ and $b_2 = R_1C_1 + R_3C_2$. From the schemes in Figs. 3 (a),(b) and (c) the voltages $u_o(s)$, $u_1(s)$ and $u_{COMP}(s)$ can be calculated as:

$$\begin{aligned} u_o(s) &= u_2(s) = \big(i_L(s) + i_{COMP}(s)\big)R_o \\ u_1(s) &= i_L(s)\big(R_S + R_o\big) + i_{COMP}(s)R_o \\ u_{COMP}(s) &= \big(i_L(s) + i_{COMP}(s)\big)R_o \\ &+ i_{COMP}(s)R_{COMP} \end{aligned} \tag{11}$$

The current transfer function can be evaluated from (10) and (11) as follows:

$$F_{COMP}(s) = \frac{i_{COMP}(s)}{i_L(s)} = \frac{-s^2c_1 - sc_2}{s^2d_1 + sd_2 + d_3}, \tag{12}$$

where:

$$\begin{aligned} c_1 &= R_3C_1C_2\left(R_o\left(R_1 + R_2\right) + R_2R_S\right) \\ c_2 &= R_oR_3C_2 + R_2R_SC_1 \\ d_1 &= R_3C_1C_2\left(R_o\left(R_1 + R_2\right) + R_1R_{COMP}\right) \\ d_2 &= R_oR_3C_2 + R_{COMP}\left(R_1C_1 + R_3C_2\right) \\ d_3 &= R_{COMP}. \end{aligned}$$

When (12) is observed along the positive imaginary axis than the frequency properties of $F_{COMP}(s)$ is extracted as $|F_{COMP}(j\omega)|$, which can be obtained for all $\omega \geq 0$. In order to obtain the magnitude and phase frequency margin it is necessary to use instead of complex variable s only $j\omega$ ($s = \sigma + j\omega$, where $\sigma = 0$). The Bode plot of consists of two plots: gain versus frequency and phase versus frequency. The magnitude $A_{hf}(\omega)$ of (12) can be evaluated as:

$$\begin{aligned} A_{hf}(\omega) &= |F_{COMP}(j\omega)| \\ &= \frac{\sqrt{(-\omega^2c_1)^2 + (\omega c_2)^2}}{\sqrt{(d_3 - \omega^2d_1)^2 + (\omega d_2)^2}} \end{aligned} \tag{13}$$

and phase margin:

$$\varphi(\omega) = \pi + \arctan\frac{c_2}{c_1\omega} - \arctan\frac{d_2\omega}{d_3 - d_1\omega^2} \tag{14}$$

After inspection of (13), (14) and the Bode plots shown in Fig. 4(a), it is evident that the DC inductor current component is attenuated significantly while the phase of high frequency components is inverted. When $\omega = 0$, and $\omega = \omega_s$, it follows that $A_{hf}(0) \doteq 0,\ (-\infty\ dB)$ and $A_{hf}(2\pi f_s) = 1,\ (0\ dB)$ respectively. The phase shift φ of i_{COMP} is 180^{o} at the frequency ω_s. Therefore, a filter with appropriate chosen parameters fulfills condition (6) during steady state operation.

The relation between the inductor and output currents is obtained from (4) and (12) as follows:

$$\frac{i_o(s)}{i_L(s)} = 1 + \frac{i_{COMP}(s)}{i_L(s)} = \frac{s^2e_1 + se_2 + d_3}{s^2d_1 + sd_2 + d_3}, \tag{15}$$

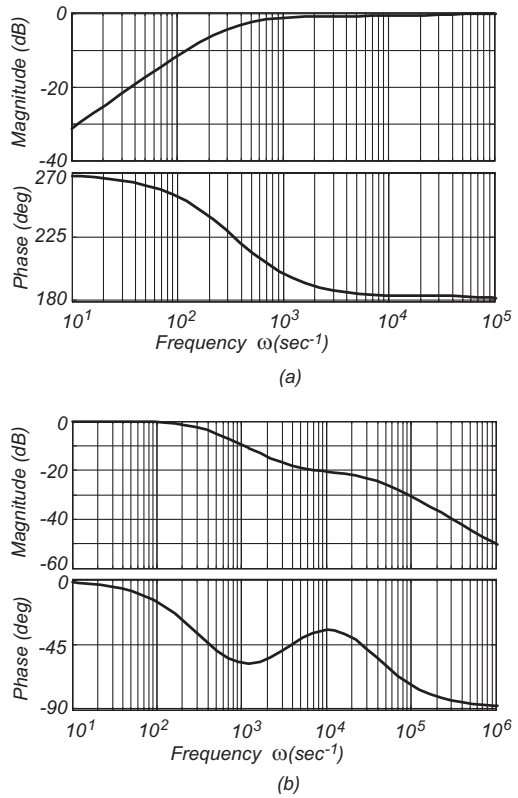

Fig. 4. (a) Transfer function $i_{COMP}(s)/i_L(s)$; (b) Transfer function $i_o(s)/i_L(s)$

where:

$$e_1 = R_3C_1C_2\left(R_1R_{COMP} - R_2R_S\right)$$
$$e_2 = R_{COMP}\left(R_1C_1 + R_3C_2\right) - R_2R_SC_1.$$

If $R_1R_{COMP} = R_2R_S$, (15) is simplified to:

$$F_o(s) = \frac{i_o\left(s\right)}{i_L\left(s\right)} = \frac{se_2 + d_3}{s^2d_1 + sd_2 + d_3}. \tag{16}$$

The Bode plot of (16) is shown in Fig. 4 (b). The magnitude $A_{lf}(\omega)$ can be evaluated as:

$$A_{lf}(\omega) = |F_o(j\omega)| = \frac{\sqrt{(d_3)^2 + (\omega e_2)^2}}{\sqrt{(d_3 - \omega^2 d_1)^2 + (\omega d_2)^2}}. \tag{17}$$

After inspection of (17) when $\omega = 0$, and $\omega = \omega_s$, it follows that $A_{lf}(0) = 1$, $(0\ dB)$ and $A_{lf}(2\pi f_s) = 2.24 \times 10^{-2}$, $(-33\ dB)$. Therefore the output current i_o will only contain DC and the high frequency components of the inductor's current will be rejected by gain of $-33\ dB$.

5 THE PRINCIPLE VERIFICATION

The operation of circuit shown in Fig. 3 (a) with and without proposed compensation was simulated by the MATLAB-SIMPOWERSYSTEM program and afterwards was verified by experimental prototype. The continuous and discontinuous conducting mode of Buck-converter operation was considered.

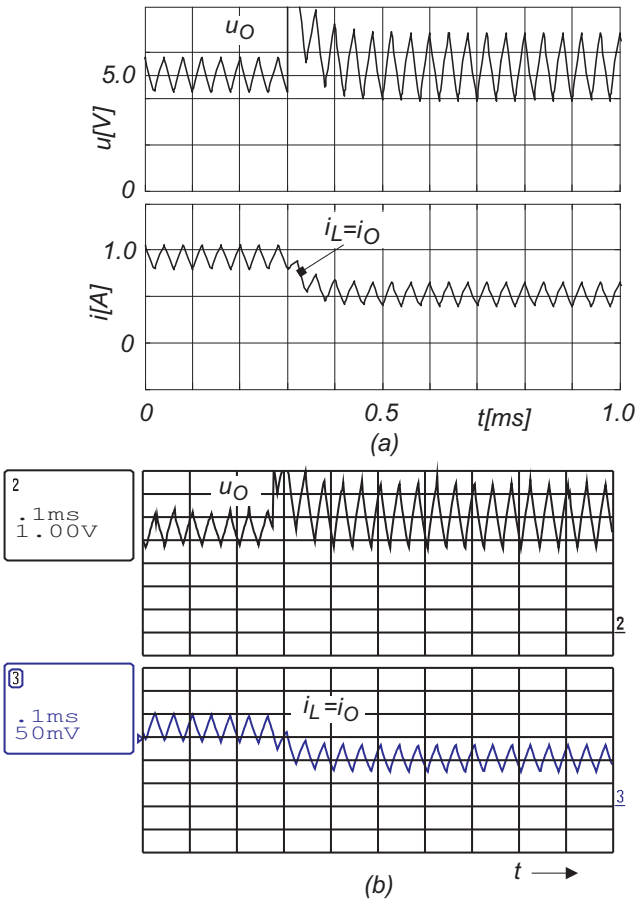

Fig. 5. (a) Simulation of an open loop operation; (b) Experiment; (x-axis $100\ \mu s/div$, y-axis: $1\ V/div$ voltage u_O; y-axis: $0.25\ A/div$, currents $i_L = i_O$

5.1 Simulation and experiment of the Open-Loop System without Compensation (Continuous and Discontinuous Current Mode of Operation)

The simulation and experimental results for the capacitor-less buck converter, are shown in Figs. 5 (a) and (b) respectively. The inductor current's response, its ripple and output voltage's response and its ripple are as predicted by (1) and (2). The output voltage is set at $5\ V$ by the duty cycle Δ_p. The variables are observed in steady and transient states. At $300\ \mu s$ the load changes from $R_o = 5\ \Omega \longrightarrow 10\ \Omega$. It is evident from the voltage response that the output voltage ripple is load-dependent due to more or less constant inductor current ripple. The current and voltage ripples are as is predicted by (1) and (2).

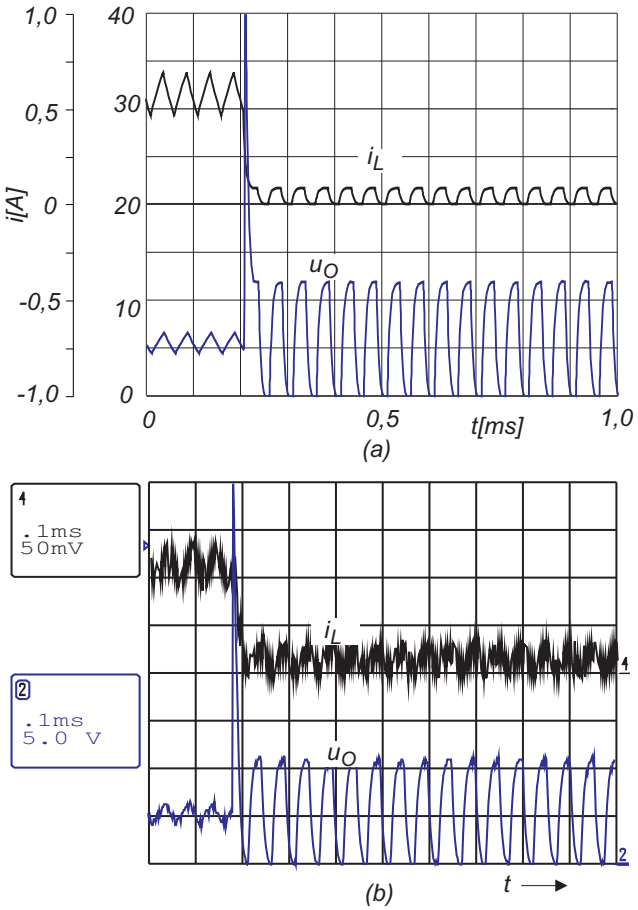

Fig. 6. (a) Simulation; (b) Experiment; (x-axis $100\mu s/div$*, y-axis: voltage* $5V/div$ *voltage* u_o*; y-axis:* $0.25A/div$ *currents* $i_L = i_o$*)*

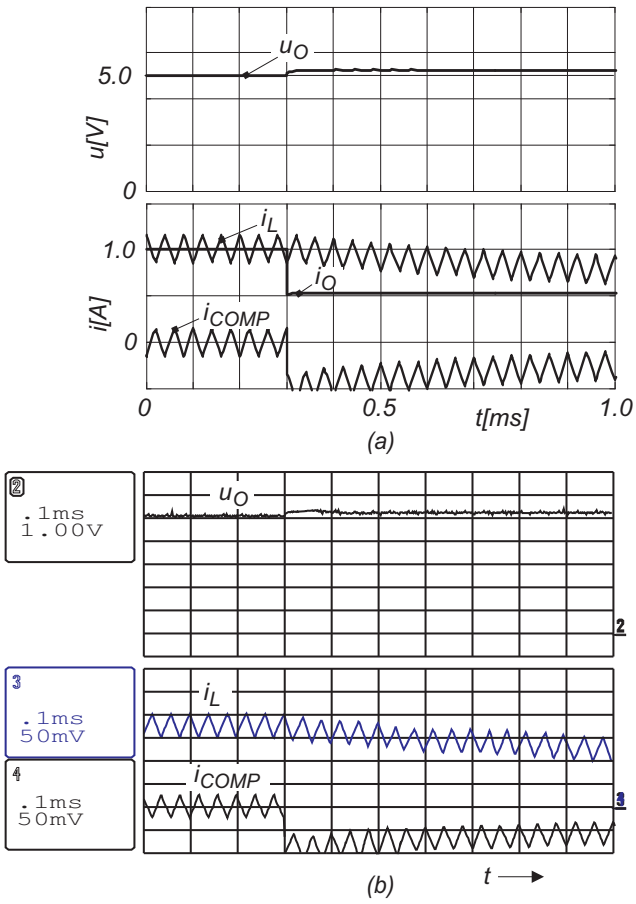

Fig. 7. Open loop operation (a) Simulation; (b) Experiment (x-axis $100\mu s/div$*, y-axis:* $1V/div$ *voltage* u_o*; y-axis:* $0.25A/div$ *currents* $i_L = i_o$*)*

The calculation of the current and voltage ripple indicated in (1) and (2) are in agreement with the simulation and experimental results shown in Figs. 5 (a) and (b). The operation of the converter in discontinuous current mode was also investigated by simulation and verified by experiment as is shown in Figs. 6 (a) and (b) respectively.

5.2 Simulation and experiment of the Open-Loop System with Compensation (Continuous and Discontinuous Current Mode of Operation)

The output current ripple and, consequently, the voltage ripple is compensated for, as proposed in the section 4. The simulation and experimental results are shown in Figs. 7 (a) and (b) respectively. The simulation and experimental results were performed during transience under the same condition indicated in chapter 5.1. According to the Bode plot in Fig. 4 (b), and from (17), it is evident that the compensating voltage u_{COMP} generates the suitable current i_{COMP}, thus reducing the output voltage ripple. The output voltage ripple can be evaluated by considering, (1),(2), and (17). It follows that the voltage ripple Δu_o can be estimated as:

$$\Delta u_o = |F_o(j\omega)|\, \Delta i_L R_o \tag{18}$$

The compensation principle was also investigated in discontinuous current mode of operation. It is indicated that the load step change causes the same voltage response as is known from Buck converter theory and praxis when capacitor is applied in the circuit. Figs. 8 (a) and (b) show the simulation and experimental results respectively when load was changed from 10Ω to 180Ω.

The voltage ripple, indicated by (18) is actually evaluated under the converter's steady-state operation, but according to the results in Figs 7 (a) and (b), 8 (a) and (b) the current i_{COMP} is not DC-free during the transient. Such responses cause an additional dissipation on the compensating amplifier A. A control of output variables (output voltage u_o and inductor current i_L) need to be introduced

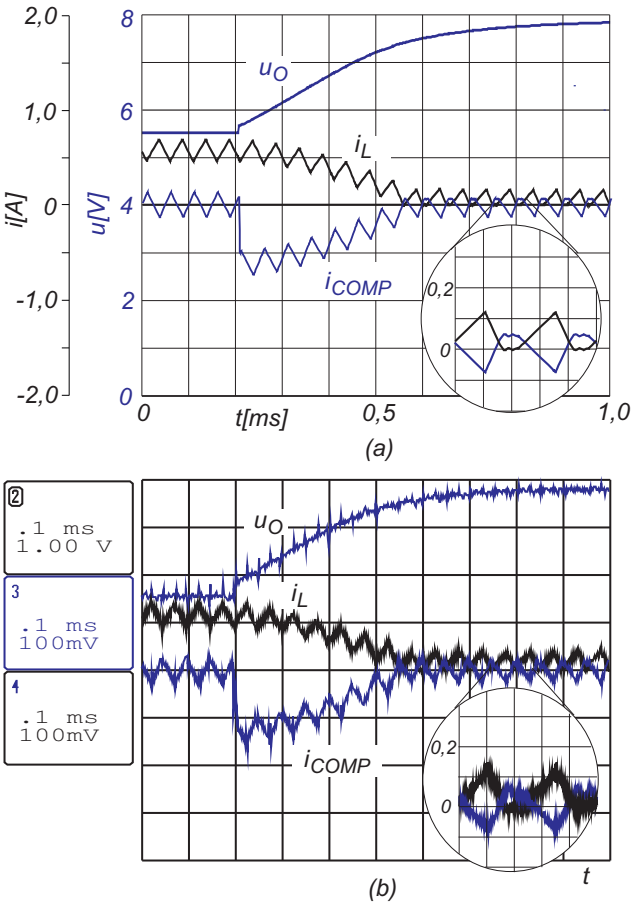

Fig. 8. Open loop operation DCM with the compensating circuit: (a) Simulation; (b) Experiment; (x-axis $100\mu s/div$, y-axis $0.5A/div$: currents i_L, i_{COMP}, y-axis $1V/div$: voltage u_o)

in order to reduce the influence of this undesired phenomena. After inspection of many control principles, the current mode control is applied, as suggested in [15] and [16].

5.3 Output Current-Ripple Compensation and Current Mode Control; Simulation and Experiment

The current-mode control denotes the multi-loop control where the voltage loop is superior to the current-control loop. The current-mode control principle, shown in Fig. 9 was first considered by simulation and afterwards by experiment. PWM based on synchronized clock pulse and appropriate compensating ramp is applied for the current mode control as suggested in [17] and [16]. The PI controller is chosen for voltage control. The parameters of the PI controller were designed, based on the standard model received by injected-absorbed current method [15]. The operation principle is verified under the transient response (R_o was changed from $5\,\Omega \longrightarrow 10\,\Omega$). Fig. 10 (a) shows the currents and voltage responses. There is an expected voltage overshot during the transience. The current

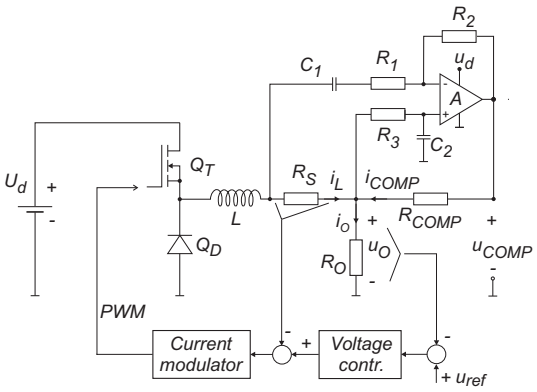

Fig. 9. Hybrid structured buck-converter with voltage and current control loop

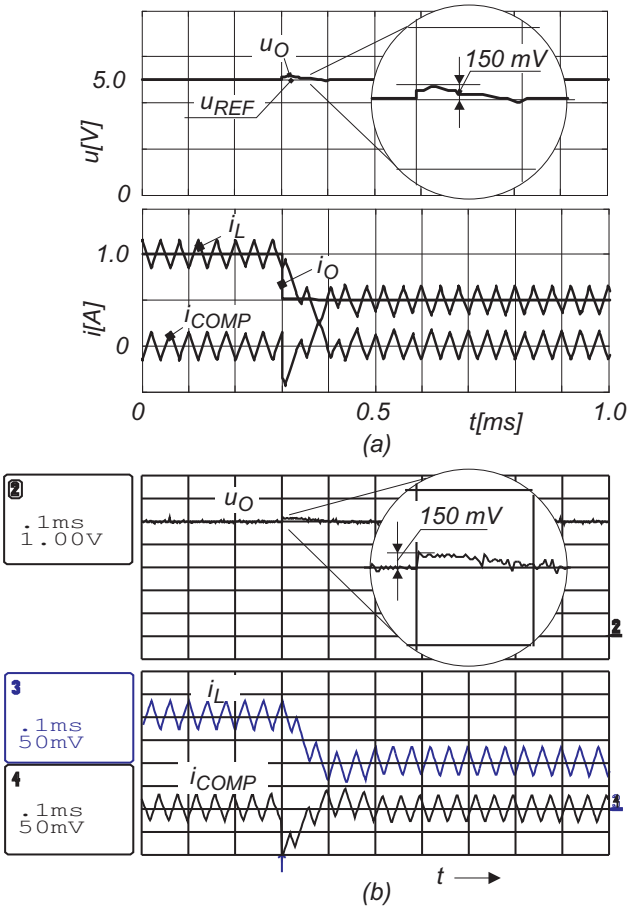

Fig. 10. Current-mode controlled: (a) Simulation; (b) Experiment; (x-axis $100\mu s/div$, y-axis: y-axis $0.25A/div$: currents i_L, i_{COMP}, y-axis $1V/div$: voltage u_O)

mode control was applied in the buck-converter prototype based on the scheme shown in Fig. 9. The experiment was performed under the same conditions as in simulation. The measured voltage ripple in a steady state was equal to the predicted voltage ripple by (18). The current-mode controlled buck converter experimental results are shown in Fig. 10 (b). In addition, the transient behavior in the experiment was the similar as predicted by the simulation (Fig. 10 (a)).

5.4 Power Dissipation of Linear Amplifier

Before evaluating power dissipations, it must be noted that the prototype was initially built to demonstrate the compensation principle, therefore, the used components are not optimized to achieve minimal power dissipations. The power dissipations on the sensing resistor R_S, compensating resistor R_{COMP} and on the output stage of the linear amplifier A are calculated. To simplify the dissipation calculations, the inductor current (Fig. 11) can be expressed as: 5

$$i_L(t) = \begin{cases} \frac{\Delta i_L}{t_{on}} t - \frac{\Delta i_L}{2} + I_o, & t_1 \le t < t_2 \\ \frac{-\Delta i_L}{T_s - t_{on}} t + \frac{\Delta i_L (T_s + t_{on})}{2(T_s - t_{on})} + I_o, & t_2 \le t < t_3 \end{cases} \tag{19}$$

The power dissipation on resistors R_S and R_{COMP} is calculated as:

$$P_{R_S} = \frac{R_S}{T_s} \int_0^{T_s} i_L^2(t) dt = \frac{R_S}{12} \Delta i_L^2 + I_o^2 R_S, \tag{20}$$

$$\begin{aligned} P_{R_{COMP}} &= \frac{R_{COMP}}{T_s} \int_0^{T_s} (i_L(t) - I_o)^2 dt \\ &= \frac{R_{COMP}}{12} \Delta i_L^2 \end{aligned} \tag{21}$$

The output stage of the linear amplifier, used for compensating circuits works in AB class. Fig. 12 (a) shows the scheme of the output amplifier stage. The compensation voltage u_{COMP} could be evaluated as:

$$\hat{u}_{COMP} = u_o \pm \hat{i}_{COMP} R_{COMP} \tag{22}$$

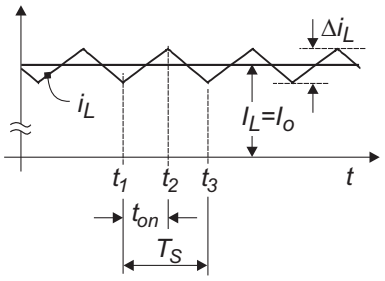

Fig. 11. The inductor current waveforms

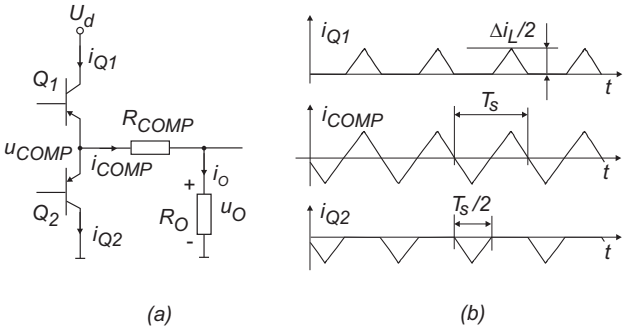

Fig. 12. (a) Amplifier output stage; (b) The current waveforms

where $\hat{}$ denotes the peak values of the compensating voltage and current respectively. According to the diagram in Fig. 12 (b) the current peak is $\hat{i}_{COMP} = \Delta i_L/2$. In order to evaluate transistor dissipation, it is convenient to use $\hat{u}_{COMP} \doteq u_o$. In this case, the dissipation on both transistors can be evaluated as:

$$P_A = P_{Q1} + P_{Q2} = (U_d - u_o) I_{Q1} + u_o I_{Q2}, \tag{23}$$

where I_{Q1} and I_{Q2} are the average values of i_{Q1} and i_{Q2}. Due to the same wave-shapes' yields:

$$I_{Q1} = I_{Q2} = \frac{1}{T_s} \int_0^{T_s/2} i_{Q1}\, dt = \frac{\Delta i_L}{8}. \tag{24}$$

From (23) and (24) and [9] the dissipation can be calculated as:

$$P_A = U_d \frac{\Delta i_L}{8} = U_d \frac{(U_d - u_o)\Delta_p}{8 L f_s}. \tag{25}$$

If controlled Buck converter is considered (see Fig.9) the difference between usual structure with the output capacitor and proposed structure without the output capacitor is only in the components R_{COMP} and *A*. Therefore the power dissipations on the compensating resistor R_{COMP} and linear amplifier *A* must be calculated in order to compare the efficiency between the usual Buck converter structure and the proposed structure. According to (21) and (25) in steady state the power dissipations on the resistor R_{COMP} and linear amplifier *A* are in direct correlation with the inductor current ripple Δi_L. To evaluate the power dissipations for the worst case scenario the dissipations are calculated at duty-cycle $\Delta_p = 0.5$, where according to (1) the inductor current ripple Δi_L is maximal. The calculated dissipation results and efficiency factor for the both converter structures are summarized in Table 1. The result are obtained at two different load levels, that is $R_o = 5\,\Omega$ and $R_o = 10\,\Omega$. The efficiency factors η_1 and η_2

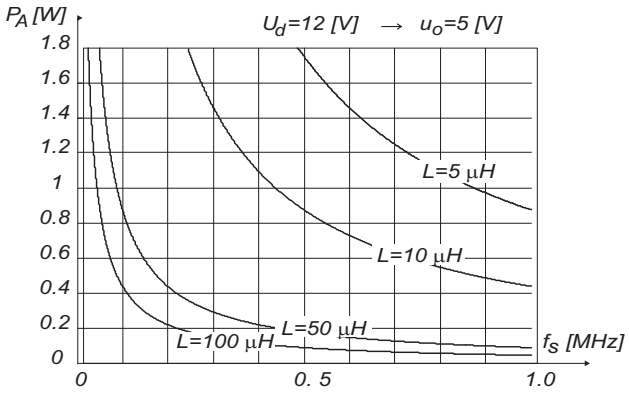

Fig. 13. Converter parameter's design diagram

for the usual Buck converter structure where an ideal coil and an ideal switch is assumed for the proposed structure are calculated as follows:

$$\eta_1 = \frac{P_o}{P_o + P_{R_s}} \tag{26}$$

$$\eta_2 = \frac{P_o}{P_o + P_{R_s} + P_{R_{COMP}} + P_A} \tag{27}$$

From the results give in Table 1, it is evident that dissipation on the compensating resistor is practically negligible, while dissipation on the sensing resistor is even grater than one of the linear amplifier in case of load $R_o = 10\,\Omega$. Dissipation on the sensing resistor can be easily and fairly reduced by using the lower value for the sensing resistor. In this case the elements accompanying the operational amplifier must be recalculated. Relatively high dissipation on the linear amplifier which reduces the overall efficiency is the main drawback of the proposed compensating principle. This is especially true when the inductor-current ration $(\Delta i_o/I_o)$ is above recommended level 0.3 [9], [16]. However from (25) it is evident that power dissipation on the linear amplifier depends on inductance L and the switching frequency f_s as shown in Fig. 13. So the dissipation on the linear amplifier can be minimized by appropriate circuit design in order to achieve the reasonable converter efficiency.

Table 1. Calculated power dissipations

$R_o[\Omega]$	5	10
$\Delta i_L[A]$	0.293	0.293
$I_o[A]$	1.091	0.571
$P_o[W]$	5.950	3.265
$P_{R_S}[W]$	0.599	0.167
$P_{R_{COMP}}[W]$	0.004	0.004
$P_A[W]$	0.439	0.439
η_1	0.91	0.95
η_2	0.85	0.84

6 CONCLUSION

This paper deals with the low power buck converter output voltage ripple minimization by compensating the inductor current ripple by using filter based operational amplifier. The operational amplifier can be incorporated into single-chip buck converters. The additional amplifier do not occupy to much surface in the silicon. The single-chip buck converter will have the same dimension, but on the output there is no need for capacitor in order to smooth the output voltage.

Operational amplifier output transistors are designed to cover the magnitude of compensating current ripple. The compensating circuit was also capable to cover the buck-converter operation in light mode (discontinuous inductor current). The drawback of the described approach becomes evident in the case of load current step change, which implies that this principle can be used only under the closed-loop converter operations. The obtained experimental results are promising and enables the improvement of the low power single chip buck converter's applications.

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