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A Review of Si MOS-gated Power Switches and PiN Rectifiers

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Revolutionary advances and developments have been made in power semiconductor device technologies during the last decades which have allowed the improvement of power electronic systems in terms of their efficiency and reliability. The advent of MOS-gated power switches such as the power MOSFET and the IGBT showing high input impedance has been a real breakthrough in the design and fabrication of power electronic systems. This paper reviews the recent progress in the development of Si MOS-gated power devices and rectifiers. The evolution of these devices' technologies together with the introduction of revolutionary device concepts is also discussed. Concretely, the introduction of trench technologies for power MOSFETs and the use of the super-junction concept for breaking the 1D-silicon limit are highlighted. Developments in IGBTs such as those based on the use of thin wafers and strategies for optimising the plasma distribution in PT IGBTs during the on-state are also addressed. Finally, advances in PiN diode technologies including new concepts for both the anode and the cathode structures are also reviewed. These approaches have allowed the reduction of the PiN total losses and a soft reverse recovery behaviour, leading to a more rugged device.

Key words: MOS-gated power devices, power MOSFETs, CoolMOS, super-junction devices, IGBTs, PiN rectifiers

Prikaz stanja silicijevih MOS upravljanih učinskih sklopova i PiN ispravljača. U posljednjim desetljećima svjedočimo razvoju sustava učinske elektronike u pogledu povećanja efikasnosti i pouzdanosti. Napredak je omogućen zahvaljujući izvanrednom napredku koji je postignut na području učinskih poluvodiča. Pojava MOS upravljanih učinskih sklopova s visokom ulaznom impedancijom, kao što su MOSFET i IGBT, rezultirao je probojem u projektiranju i proizvodnji sustava učinske elekronike. Ovaj članak daje uvid u napredak koji je u posljednje vrijeme ostvaren u razvoju silicijeve MOS upravljane učinske elektronike i ispravljača. Uz dosadašnji razvoj tehnologije navedenih komponenata, u članku je uključen i osvrt na revolucionarne koncepte budućeg razvoja. Konkretno, u radu su objašnjene tehnologija rova za MOSFET i korištenje koncepta super spoja za probijanje granice jednodimenzionalnog silicija. Razmatrana su i poboljšanja IGBT-ova koja se baziraju na uporabi tankih pločica a strategijama optimiranja distribucije plazme u PT IGBT-ovima za vrijeme aktivnog stanja. Konačno, prikazan je i napredak u tehnologiji PiN dioda koji uključuje nove strukturalne koncepte katode i anode. Ovi pristupi su omogućili smanjenje ukupnih gubitaka PiN diode i blagu dinamiku reverznog oporavka, što rezultira povećanjem robusnosti sklopa.

Ključne riječi: MOS upravljani učinski sklopovi, učinski MOSFET, CoolMOS, super-junction sklopovi, IGBT sklopovi, PiN ispravljači

1 INTRODUCTION

Power Electronics plays a key role in the generation-storage-distribution cycle of the electrical energy. This is related to the fact that the main portion of the generated electrical energy is consumed after undergoing several transformations, many of them carried out by power electronic converters. Improvements in power electronic systems are strongly related to advances in power semiconductor device technologies since the largest portion of the power losses in power electronic systems are dissipated in their power semiconductor devices. Semiconductor power device technologies have evolved during the last decade improving the efficiency, and lowering the size and weight of power devices as well as increasing their ruggedness. The social impact of discrete power devices is impressive due to their huge market covering applications as low as 20V up to several kV. Today, discrete power devices are based on the mature and very well established Silicon technology, which allows increasing the efficiency of the electrical energy management for a more rational use of energy. Power discrete devices can be broadly classified into two categories: power switches and rectifiers.

The introduction of the power MOSFETs in the 70s and the IGBT in the 80s represented two important breakthroughs in power semiconductor device technology and made possible the development of highly efficient power electronic systems due to their high input impedance. The continuous improvement in microelectronics and the introduction of novel concepts for power device structures have led currently to Si power switches with a high electrical performance. In addition, improvements have also been made in power rectifiers allowing the development of more reliable and rugged devices which is of major concern in the power electronic circuits. This paper presents an overview of recent advances and developments in discrete Si MOS-gated power switches and rectifiers which have conducted to the high efficient and reliable devices currently used in power electronic systems.

2 POWER MOSFETS

Power MOSFETs were introduced in the 70s replacing BJTs (Bipolar Junction Transistor) due to their inherent high input impedance. The basic structure is the DMOS (Double Diffused MOS) transistor which is characterized by a double diffused process for the channel formation together with a drift region for supporting the voltage in the off-state. These power devices are mainly addressed to low voltage and high frequency applications, such as telecom, power supplies, automotive and domestics. Lateral architectures have been devoted to Smart Power ICs combining power DMOS switches monolithically integrated with logic and analog circuitry. However, the current capability of these lateral power devices is limited by the surface area consumed for the drift region, and consequently real power MOS devices show a vertical architecture with a parallel association of individual unit cells in the top side of the chip and a common drain on the back side. For low voltage applications (V_{BR}<100 V), the channel resistance is a significant portion of the total specific on-resistance ($R_{ON\text{-}SP}$), and a major breakthrough in optimizing $R_{ON\text{-}SP}/V_{BR}$ trade-off was the introduction of trench technologies. These technologies have allowed increasing cell density integration, and progress in cell pitch reduction accounts for much smaller $R_{ON\text{-}SP}$ values in low voltage MOSFETs [1-5]. Developments on lithographic processes have permitted the reduction of the cell pitch, and values as low as 0.6 μm have been made possible with the use of deep ultraviolet lithography [6]. Although the reduction of the cell pitch size reduces $R_{ON\text{-}SP}$, it also increases the device switching losses. The Miller charge (Q_{GD}) is increased for a given Si area, and as a result the reduction of the $R_{ON\text{-}SP} \times Q_{GD}$ figure of merit is of interest for the device losses reduction. In this sense, new device concepts, like the NexFET from Texas Instruments [7] aimed at high-frequency power conversion, have been proved to be effective in reducing the Miller capacitance and to improve the $R_{ON\text{-}SP} \times Q_{GD}$ figure of merit by a factor of 2 in comparison with trench power MOSFETs.

The drift region required to support the blocking voltage increases $R_{ON\text{-}SP}$ as V_{BR} is increased. This was the reason of the introduction of conductivity modulated power structures such as the IGBT for V_{BR} > 400-600V. The minimum contribution of $R_{ON\text{-}SP}$ due to the drift region increases as $V_{BR}{}^{2.5}$, which is known as the 1D-Silicon limit. A breakthrough in power MOSFET was the introduction of device structures that broke this 1D-limit in the late 90's. The concept was based on the charge compensation principle [8], typical of power structures known as super-junction devices. Super-junction power devices were commercially introduced in 1998 by Infineon (CoolMOS) [9], and are now available with voltage ranges between 500 and 900V. The cross-section of the CoolMOS structure is shown in Fig. 1.

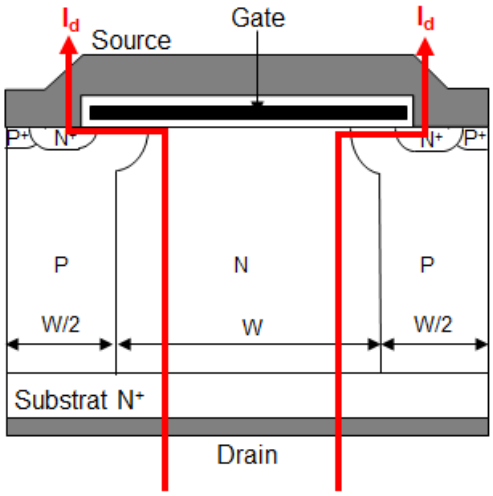

Fig. 1: Schematic cross-section of the CoolMOS structure

As one can see, the CoolMOS is characterized by the presence of alternate p-type and n-type columns, W being their width. The p-type columns are performed by multiple local p-type implantations followed by n-epilayer growth steps. As a result, compensating acceptors are located in the lateral proximity to the drift region donors, the doping value of the p-type columns being adjusted for an effectively compensation of the n-regions. The n-type and p-type columns are depleted even at very low voltages, and the interaction between lateral and vertical electric field components yields to a nearly rectangular shape of the vertical electric field in the blocking mode. This effect is similar to that shown in RESURFed devices [10], and the resulting vertical electric field distribution contrasts to the triangular shape in the case of conventional power

MOSFETs. As a result, the n-type doping level can be significantly increased for a given V_{BR} value in comparison with a conventional power MOSFET, thus lowering $R_{ON\text{-}SP}$ below the 1D-Silicon limit. Therefore, in a super-junction device, the current flows through highly doped vertical n-type columns (see Fig. 1), and consequently more charge is available for current conduction compared to the case of a conventional power MOSFET. In addition, the CoolMOS achieves extremely short switching times due to the sudden nearly intrinsic depletion of the laterally stacked p-n columns, and as a result switching losses are also lower than in the case of conventional power MOSFETs.

An alternative to the CoolMOS structure based on the trench compensation concept has been also proposed. In order to reduce the cell pitch (2W) in a CoolMOS structure, higher number of epilayer growth and selective p-type implantation steps are required to reduce the lateral thermal diffusion of p-type columns. An approach that offers both reduced $R_{ON\text{-}SP}$ and process complexity is that followed in the trench compensation devices. These devices use deep trench etching and epitaxial re-growth for making the alternate doped pillar structure. By an optimized trench filling epitaxial growth technique, 680V devices with an extremely low $R_{ON\text{-}SP}$ of 7.8 $m\Omega cm^2$ have been reported by Denso [11]. Another alternative is the deposition of two epitaxial layers (n and p-type) on the vertical walls of deep trenches, which was first reported by Infineon [12], showing a theoretical 50% reduction of $R_{ON\text{-}SP}$ in comparison with a 600V CoolMOS. Recently, ON Semiconductor has also reported the UltiMOS structure [13], which is a local charge balanced trench super-junction MOSFET characterized by the selectively growth of both n-type and p-type thin layers on the vertical walls of a deep trench structure. Figure 2 shows a microphotograph of a 730V device with an $R_{ON\text{-}SP}$ of 23 $m\Omega cm^2$.

The requirement for a precise charge compensation of n-type and p-type columns limits the application of this technology for low breakdown voltages (<200V), since the process window deviation for obtaining charge balanced devices gets narrower as column doping is increased and its width (W) is decreased [14]. Although recent advances in low voltage super-junction devices have been reported [15], a theoretical solution in this case is the oxide-bypassed VDMOS [16], which uses a metal-thick oxide structure inside deep trenches in the drift region instead of p-type columns. In this structure, the oxide thickness helps to control V_{BR}, the field plate structure depleting the n-type columns laterally. Hence, this super-junction device based on a field plate structure connected to the source accounts for a higher n-type doping resulting in a reduced $R_{ON\text{-}SP}$. An optimization of this structure in terms of the vertical electric field distribution requires an asymmetric structure, which is characterized by an oxide thickness increase in the vertical direction (GOB, Gradient Oxide-Bypass) [17].

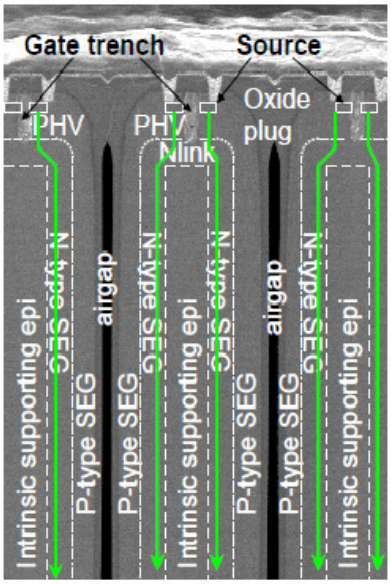

Fig. 2: Microphotograph of the UltiMOS structure [13]

A similar structure is the RESURF stepped oxide (RSO) transistor, which includes a trench field plate in the drift region isolated by a thick oxide layer, as shown in Fig. 3a. 85V RSO MOSFETs with an $R_{ON\text{-}SP}$ of 0.58 $m\Omega cm^2$ have been reported [18], although this structure exhibits relatively large switching losses. This is because of the high gate-to-drain Miller capacitance (C_{GD}) due to the fact that the polysilicon gate layer largely extends along the drift region. To overcome this drawback, some innovative structures have been reported to take benefit of the low conduction losses of a super-junction field plate structure and a reduced Miller charge to decrease switching losses. One example is the Split-Gate (SG)-RSO MOSFET which uses an isolated field-plate between the gate and the drain to reduce the Miller charge, as shown in Fig. 3b. As it can be seen, the split polysilicon layer is isolated from the upper region, which connects to the gate and the lower region, which connects to the source. The impact of splitting the field-plate in reducing Q_{GD} will allow trench MOSFET to be used in high frequency switching DC-DC circuits, where switching losses might amount to more than 50% of losses. 35V SG-RSO MOSFETs with an $R_{ON\text{-}SP}$ of 3.8 $m\Omega mm^2$ and Q_{GD} of 0.9 $nCmm^{-2}$ have been demonstrated [19].

Figure 4 shows the $R_{ON\text{-}SP}/V_{BR}$ trade-off of different power MOSFET technologies, highlighting the 1D-Silicon (VDMOS) limit and the improvement of super-junction structures in minimizing $R_{ON\text{-}SP}$. According to this figure, the super-junction theoretical limits (both the CoolMOS and the GOBVDMOS) break the 1D-Silicon limit for

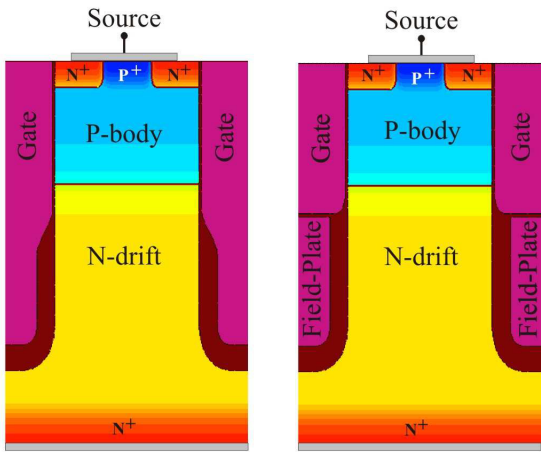

Fig. 3: Cross-section of (3a) RSO and (3b) SG-RSO MOSFET structures

$V_{BR} > 100V$. In addition, the CoolMOS limit shifts down as the pillars width (W) is reduced, thus further improving the $R_{ON\text{-}SP}/V_{BR}$ trade-off. The GOBVDMOS limit shown in Fig. 4 accounts for a mesa width of 2.5 μm, and the plotted experimental results of RSO [18] and SG-RSO [19] structures correspond to much lower mesa width values. However, the effectiveness of super-junction concepts decreases as V_{BR} is reduced, especially for $V_{BR} < 100V$.

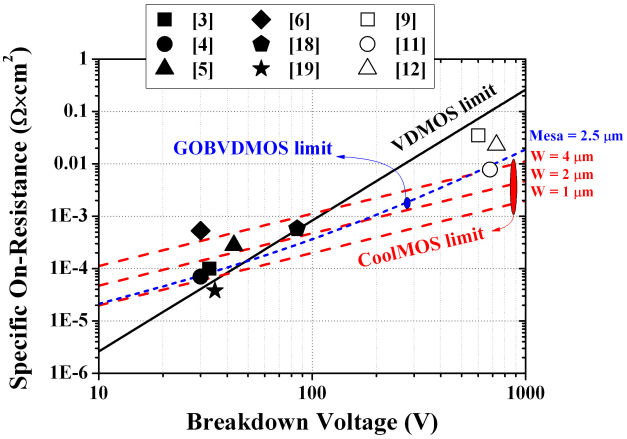

Fig. 4: Comparison of different power MOSFET technologies in terms of $R_{ON\text{-}SP}/V_{BR}$ trade-off

3 IGBTS

The IGBT (Insulated Gate Bipolar Transistor) is the most widely used power semiconductor switch covering a wide broad of applications such as domestic, industrial motor control, traction, renewable energy sources, etc. Today, commercial IGBTs with V_{BR} values from 600V to 6.5kV are available, and 8kV devices have also been demonstrated [20]. The development of high performance and robust IGBTs in the last years has also conducted to the improvement of the reliability of power inverters, especially in harsh environment conditions due to the severe stresses on power devices [21, 22]. The IGBT was introduced in the early 80s [23], and it combines the high input impedance of power MOSFETs with a higher current capability due to the bipolar conduction. Basically, the main difference in comparison with the power MOSFET is that the n^+- drain is replaced by a p^+- anode, which injects holes into the n-base in the forward conduction mode reaching high injection regime (injected carrier concentration is higher than the background doping level), thus modulating the n-base conductivity. The first IGBT structures were prone to show the latch-up mechanism due to the activation of the inherent parasitic thyristor structure, which accounts for the lost of gate control and eventually to device destruction. Improvements in device design and process technology leading to submicron features in the basic cell have allowed today latch up-free IGBTs.

There are basically two different types of IGBTs depending on the extension of the space charge region in the blocking mode [24]. In the first one, the space charge region extends all over the low doped n-base region, and the electric field distribution shows a trapezoidal shape. This is known as a punch-through (PT) structure, and an N-buffer layer between the n-base and the p^+- anode is needed to prevent that the space charge region reaches the anode. On the other hand, the non-punch-through (NPT) IGBT is characterized by the fact that at breakdown the n-base thickness is larger than the extension of the space charge region, and therefore the electric field distribution has a triangular shape.

The first PT IGBTs were fabricated with an epitaxial process technology in which the N-buffer and the n-base region were grown on a p^+- substrate. This technology dominated the market of 600V for several years. Killing lifetime techniques such as electron or proton irradiations are used to reduce turn-off losses since the current tail is governed by the recombination process of minority carrier excess in the base region. In addition, this also accounts for the reduction of the current gain of the PNP bipolar transistor, just preventing the risk of latch-up. Higher breakdown voltages require a thicker and more resistive n-base region, which makes the epitaxial process a non viable solution. NPT IGBT structures [25] overcome this techno-

logical limitation for high voltage devices. The n-base region is thicker than that of the PT counterparts, and a very shallow, low doped p^+- anode is diffused in the backside. As a result, the NPT IGBT is robust against latch-up and shows a higher short-circuit robustness [26]. In addition, NPT IGBTs show a positive temperature coefficient of the forward voltage drop, which makes easier their paralleling, as it is the case in high current IGBT power modules. In the past, these features made NPT devices very attractive even in the range of 600V. However, the total losses of NPT IGBTs are higher than those of PT IGBTs. Concretely, on-state losses are higher due to the thicker n-base region, and switching losses are also higher since the current tail in PT IGBTs is significantly shorter than in the NPT IGBT. As a consequence, the improvement of IGBT electrical performances has been addressed through the PT concept in the last decade.

Recent advances in IGBT performance are related to the optimization of the free carrier plasma distribution in the n-base during the on-state. The first generations of IGBTs showed a plasma distribution that decreases from anode to cathode. One effective way to reduce the on-state voltage drop is increasing the carrier concentration at the cathode side. In addition, the increase of the carrier excess near the cathode region does not represent an increment of the turn-off losses, since this charge is effectively and rapidly removed by the electric field at the very onset of the turn-off process [27].

A great effort was dedicated in the 90s to develop thyristor based structures with MOS gate control. This is the case of the MCT [28] based on a triple diffusion process and other MOS-thyristor structures compatible with an IGBT process technology [29-31]. The idea was to increase the plasma distribution via a double injection from both the anode and the cathode. However, these structures did not gain the commercial attention for two reasons. The first one was the low values of the maximum controllable current for a real device prior to the activation of the parasitic thyristor inherent to all the structures. Secondly, the improvement of plasma distribution in the n-base of modern IGBTs opened the possibility to compete them with GTOs in very high voltage applications. The first reported structure with enhanced plasma distribution was the IEGT (Injection Enhanced insulated Gate bipolar Transistor) [32]. This structure was a 4.5 kV Trench-IGBT with very low forward voltage drop, although the concept can also been applied to a planar IGBT structure [33]. It was shown that the voltage drop in this structure is reduced by decreasing the area of the PNP bipolar transistor; i.e., increasing the distance between adjacent p-bodies. However, the channel resistance is increased when separating the p-bodies and, consequently, there is an optimal distance which minimizes the on-state forward voltage drop. Note that this strategy is completely different to the design of power MOSFETs, in which high cell density integration is desired to reduce $R_{ON\text{-}SP}$. The hole current is lowered when reducing the area percentage of the p-body region, increasing the plasma distribution at the cathode side and lowering the voltage drop [34]. This solution can be applied to both planar and trench IGBT structures. As an example, Fig. 5 shows the cross-section of a trench IGBT based on this principle, in which the channels are only located in the middle of the cell between adjacent trenches [35]. Another alternative [36] consists in an IGBT structure in which several individual cells are not contacted; therefore, the on-state voltage drop is reduced since the enhanced plasma effect is higher than the increase of channel resistance.

A different strategy to enhance the plasma distribution in the vicinity of the cathode consists in incorporating an additional n-type layer that acts as an effective barrier for the hole flow. This is the case of the CSTBT (Carrier Stored Trench gate Bipolar Transistor) from Mitsubishi [37], where the built-in potential across the n-buried/n-base junction prevents the hole flow. A similar concept has been adopted by ABB [38] to prevent the hole current flow into the p-body region. The cross-section of this IGBT structure is shown in Fig. 6, and it is characterized by an n-diffusion below the p-body. This n-diffusion prevents the hole flow, and electrons are provided by the channel to maintain charge neutrality, increasing in this way the plasma distribution near the cathode. These solutions, that include a hole barrier for the hole flow, do not need neither to reduce the number of contacted IGBT cells nor to increase the distance between adjacent p-bodies, although they can also been considered.

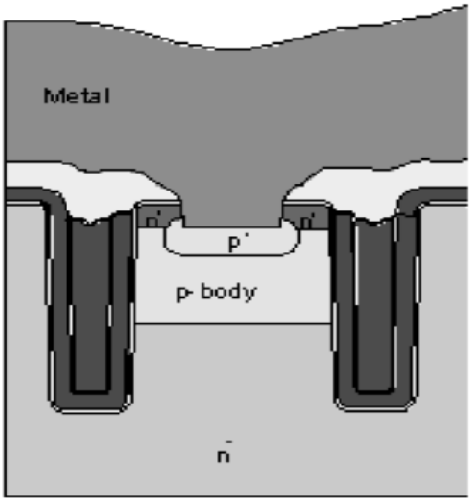

Fig. 5: Cell structures for new trench IGBT generations [35]

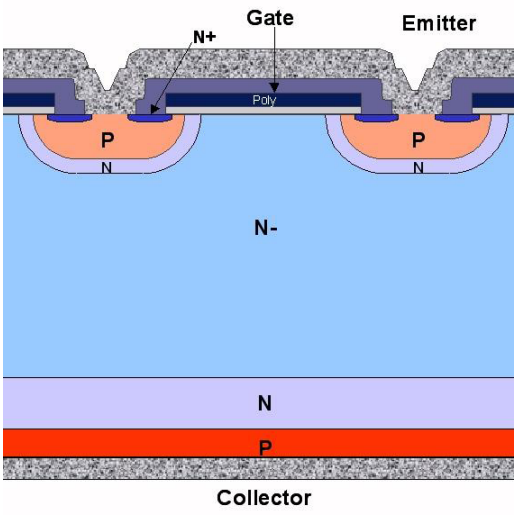

Fig. 6: Cross-section of the enhanced-planar IGBT [38]

In addition to the above mentioned measures for optimizing the plasma distribution in the n-base layer, modern IGBTs are characterized by a vertical shrink of the n-layer giving rise to a thin base region. This concept is applied to IGBTs in the 600V-6.5kV range, and has been possible by new processes on ultrathin silicon wafers for low voltage IGBTs [39, 40]. The combination of a thin n-base with a low-doped field stop (FS) layer results in a drastic reduction of the overall losses [41]. The FS concept is based on using an n-layer with increased doping in front of the p-anode, and accounts for a trapezoidal electric field distribution in the off-state instead of the triangular one of the NPT structure. The electrical behavior of the FS IGBT is closer to that of the NPT IGBT, since the fabrication process is based on a homogeneous substrate and the p^+- anode consists in a very shallow and low doped diffusion. As in the NPT IGBT, the device shows a positive temperature coefficient of the forward voltage drop, which makes easier the device paralleling. In addition, the tail current in the turn-off process is shorter than in the NPT counterpart since a lower portion of the stored plasma remains close to the p^+-anode. On the other hand, there has also been reported theoretical analysis to apply the super-junction concept to the IGBT [42, 43].

Reverse Blocking IGBTs are of interest in applications like AC Matrix Converters. The development of such IGBT structures was limited by the fact that the bottom p-n junction in a NPT IGBT also requires an edge termination to support the voltage in the reverse blocking mode. This is performed by leading the bottom p-junction to the front side of the wafer by a deep p-diffusion through the whole wafer [44-46]. Figure 7 shows the cross-section of an IGBT structure with deep diffusion isolation with reverse blocking capability. Due to the need of bidirectional blocking, only NPT IGBT structures can be considered since the inclusion of a buffer layer at the anode side would eliminate the reverse blocking capability. Therefore, the on-state voltage drop is higher than that in FS IGBTs. In addition, the realization of the deep isolation diffusion implies a waste of area, especially as V_{BR} is increased. Other techniques for overcoming this loss of area have been considered such as the use of deep trenches for replacing the deep isolation diffusion.

Another concept is the reverse conducting IGBT (RC-IGBT), which is based on the monolithic integration of an IGBT with an antiparallel diode. This can be done by implementing a shorted anode structure interrupting the p^+-anode diffusion and including an n^+-layer. Several attempts have been made in the 600V-1.2kV range [47, 48] although some measures must be taken to improve both the IGBT and the free-wheeling diode since both aspects contradict each other. In this sense, an interesting RC-IGBT structure rated 3.3kV has been reported [49], whose cross-section is shown in Fig. 8. As it can be seen, the structure includes a hole barrier layer (n-diffusion below the p-well) for optimizing the IGBT performance as indicated above and also acting as a reduced p-emitter efficiency for the diode. In addition, a local lifetime control can also be used below the p-body region.

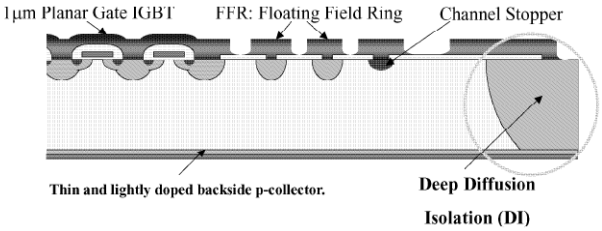

Fig. 7: Cross-section of the RB-IGBT [45]

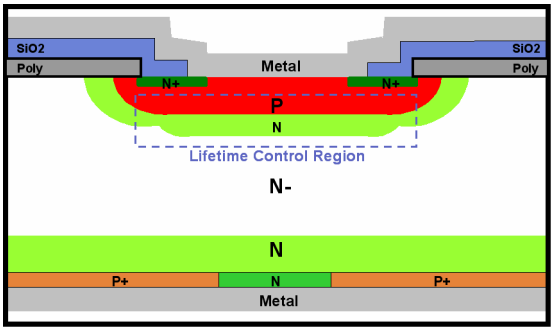

Fig. 8: RC-IGBT cross-section [49]

4 POWER RECTIFIERS

The most important Si rectifier for high-voltage applications is the PiN diode. Today, PiN diodes with V_{BR} values up to 6.5 kV are commercially available and mainly used as freewheeling diodes for IGBTs based applications such as traction, motor control and HVDC converters. A key point in the design of HV diodes is to ensure soft recovery behaviour. The improvement in IGBT technologies has resulted in the appearance of high performance devices, and pushes the need to develop new diode generations for improving reverse recovery softness and safe operating area.

The PiN diode is a $p^+n^-n^+$ structure where the n- base is flooded of plasma during the on-state. For achieving soft recovery behaviour, a lower plasma level at p^+-anode side than at the n^+-cathode side must be ensured. Many efforts have been done to fulfil this requirement for the plasma distribution in the drift region of the structure. Among them, there are PiN diodes with anode structures for reducing the anode area that is injecting holes in the drift region. An example is the merged PiN/Schotttky diode (MPS) in which the p-diffusion is interrupted by Schottky areas [50]. This approach reduces the hole injection and lowers the carrier concentration at the p-n junction side. A variation of this approach is the trench oxide PiN Schottky [51] in which the p-regions are performed at the bottom of trench cells while the Schottky contact is at the surface. In both approaches, the area of layers injecting holes is reduced and, consequently, the free carrier densities at the p-n junction side are lowered.

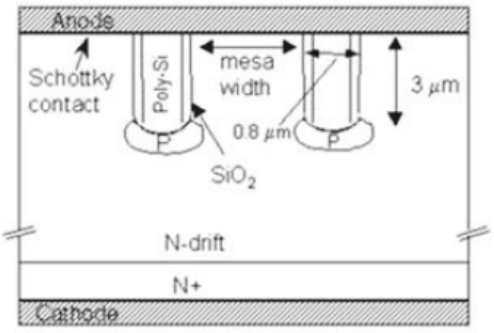

Fig. 9: Schematic cross-section of the trench oxide pin Schottky diode [51]

There are also other concepts for getting the desired plasma distribution without using anode structures for reducing the area of hole injection. One is based on the use of a local recombination centre profile close to the p-anode. This structure is the CAL (Controlled Axial Lifetime) diode [52] in which the peak and location of the recombination centre profile is adjusted by the energy and dose of helium implantation. Diodes of several kVs have been commercialised based on this concept, which allows obtaining a suitable plasma distribution in the on-state if the recombination centre peak is located close to the p-n junction [53]. Another solution which is used by Infineon in commercial diodes up to 1.7 kV is the EMCON diode (Emitter-Controlled Diode) [54]. The EMCON diode implements a shallow p-anode of low emitter efficiency on the top side and a backside n^+-emitter, which allows obtaining the desired plasma distribution without using local lifetime adjustment although it can be used to further reduce the p-emitter efficiency for low reverse recovery current peaks. This technological approach has been demonstrated for robust diodes up to 3.3 kV.

All the above mentioned approaches for the anode structure have resulted in high performance PiN diodes up to 1.7 kV. Nevertheless, for higher voltages they do not provide a reliable solution, mainly as the device ruggedness is concerned [55]. Improvements in high-voltage diodes have been done by optimising the n-n+ junction to prevent the appearance of high electric field peaks at this junction during reverse recovery with dynamic avalanche. In fact, an Egawa-type field distribution [56] with high electric field peaks at both p-n and n^-n^+- junctions results in a double-sided dynamic avalanche and device destruction [57]. A strategy for reducing the electric field peak at the n^-n^+- junction consists in lowering the negative charge of free electrons by injecting holes from the cathode side. An example of this solution is the Field Charge Extraction (FCE) diode [58] whose cross-section is drawn in Fig. 10.

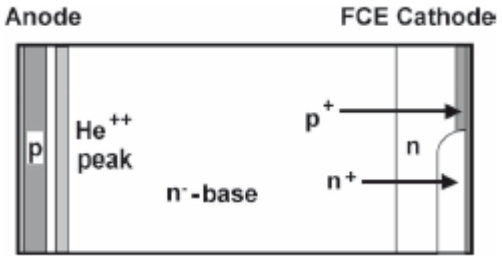

Fig. 10: Cross-section of the FCE structure [58]

As it can be seen, a p^+-diffusion is added to the cathode side which accounts for hole injection and the compensation of electrons generated by dynamic avalanche. This approach can also be used together with local helium implantation at the anode side for the sake of soft recovery behaviour. Another PiN structure based on the same idea is the Controlled Injection of Backside Holes (CIBH) diode [59], which is characterised by the presence of buried floating p-layers at the cathode side, which prevents the forma-

tion of high electric field peaks and avalanche generation at the n^-n^+-junction. Figure 11 shows a schematic cross-section of the CIBH structure. FCE and CIBH diodes with improved dynamic ruggedness and soft recovery behaviour have been reported at 6.5 and 3.3 kV, respectively. Another measure to improve dynamic ruggedness by avoiding avalanche generation at the n^-n^+-junction is the use of an adjacent N-buffer to this junction, which reduces the risk of reaching an Egawa-type electric field distribution [60]. 3.3kV freewheeling diodes with a high dynamic avalanche capability have been demonstrated [61]. In addition, it has recently reported a new high voltage diode technology [62] using a double-sided local lifetime control with helium irradiation on both the anode and cathode sides of the diode. Currently ABB is commercialising diodes up to 6.5kV with this technology, offering reduced total losses and soft reverse recovery behaviour and high ruggedness.

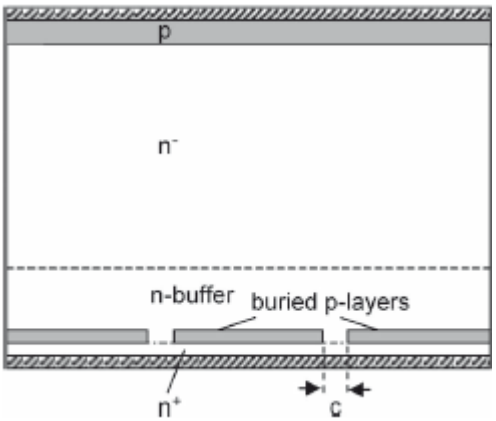

Fig. 11: Schematic CIBH diode cross-section [59]

5 CONCLUSION

This paper reviews the most important developments carried out in discrete Si MOS-gated power switches (MOSFETs and IGBTs) and rectifiers that have conducted to highly efficient and ruggedness devices for power electronic systems. As far as power MOSFETs is concerned, the high integration density by the use of trench technologies is mandatory for low voltage applications (<100V), and further improvements are expected to be related with a reduction of the features size conducting to a high integration level and reduction of the on-state forward voltage drop. In addition, measures for reducing the Miller capacitance have to be taken into account to reduce switching losses. The introduction of super-junction based devices for higher voltage applications have been shown to be crucial in breaking the 1D-Si limit allowing unipolar power devices to compete with the IGBT in the 600-900V applications range. From the introduction of the IGBT in the 80s, important improvements have been made in optimising the internal plasma distribution in the on-state together with the use of thin wafers. Highly efficient and ruggedness IGBTs from 600V to 6.5kV are commercially available, and devices up to 8kV have been demonstrated. The maturity and well established IGBT process technologies have conducted to withdraw of the development of MOS-thyristor structures to compete with GTOs in high power applications. Improvements are expected in a further optimisation of high voltage structures, and also in the incorporation of new functions on future commercial IGBTs such as reverse blocking and reverse conducting.

Finally, commercial PiN rectifiers with soft recovery behaviour are available. This has been made possible by optimising the plasma distribution in the drift region. The solutions were firstly made on structures with voltage capabilities up to 1.7kV, these strategies being also appropriate for commercial devices with higher voltage ranges. Although a high effort has been made in the cathode engineering to increase the ruggedness of high voltage PiN diodes, further improvements are expected in a near future.

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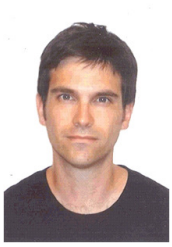

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