ISSN 1330-3651(Print), ISSN 1848-6339 (Online)
UDC/UDK 621.373:[654.16:004.771]

A LOW POWER SERO BASED VCO IN 0,18-µm CMOS PROCESS

Jubayer Jalil, Mamun Bin Ibne Reaz, Siti Sarah Binti Md Sallah

Original scientific paper

A 3-stage single-ended ring oscillator (SERO) based voltage controlled oscillator (VCO) has been proposed to operate from 2,4 GHz to 5,42 GHz for short range wireless communication systems, such as Wi-Fi, Bluetooth and Zigbee. Single-ended delay cell has been adopted to form the proposed VCO in standard 0,18-µm CMOS process. This VCO consumes only 664,51 µW of power. To achieve wide tune range of 55,72 %, control voltages are varied from 0,7 V to 1,8 V. The post-layout simulation result of phase noise is −107,59 dBc/Hz at 1 MHz offset from the centre frequency of 4,3 GHz. The circuit is designed and simulated using Mentor Graphics environment.

Keywords: *complementary metal oxide semiconductor (CMOS), PLL, single-ended ring oscillator (SERO), VCO*

Oscilator reguliranog napona (VCO) zasnovan na nesimetričnom prstenastom oscilatoru (SERO) male snage u 0,18-µm CMOS postupku

Izvorni znanstveni članak

Oscilator reguliranog napona (VCO) s trostepenim nesimetričnim prstenastim oscilatorom (SERO) postavljen je za rad od 2,4 GHz do 5,42 GHz u bežičnim komunikacijskim sustavima uskog frekventnog područja kao što su Wi-Fi, Bluetooth i Zigbee. Primijenjeno je jednostrano vrijeme kašnjenja ćelije da bi se predloženi VCO postavio u standardni 0,18-µm CMOS postupak. Taj VCO troši samo 664,51 µW snage. Da bi se postiglo široko frekventno područje od 55,72 %, reguliranje napona varira od 0,7 V do 1,8 V. Rezultat fazne buke nakon simulacije je −107,59 dBc/Hz kod 1 MHz pomaka od srednje frekvencije od 4,3 GHz. Strujni krug je projektiran i simuliran korištenjem Mentor Graphics okruženja.

Ključne riječi: *komplementarni metal oksid poluvodič (CMOS), PLL, nesimetrični prstenasti oscilator (SERO), VCO*

1 Introduction

The rapid development of higher frequency devices by very large scale integration (VLSI) technique has mainly taken place owing to the advent of CMOS process and its downscaling features [1, 2]. The voltage-controlled oscillator (VCO) is as one of the important modules in the phase locked loop (PLL) circuit for designing a high-data-rate wireless and wire-line communication devices. Its applications include clock/data recovery circuits of serial data communication, chip clock distribution, disk drive read channels and integrated frequency synthesizers [3, 4]. Typically, the VCO can be built using either the LC resonator or the ring oscillator in CMOS process [5, 6, 7]. The design of ring oscillator involves many performances, such as tuning range, phase noise and power dissipation. The LC resonator can operate at higher frequencies, and it possesses a better noise performance, but it requires the area-starving spiral inductor and has deficiency of narrow tuning range [5]. On the contrary, the ring oscillator can easily achieve a wider tuning range, and without the presence of inductance, the ring oscillator circuit becomes compact and smaller in size.

A basic ring oscillator (RO) consists of a number of delay stages, with the output of the last stage connected in a positive feedback loop to the first input. In order to achieve oscillation, the RO must provide a phase shift of 2π and have a unity voltage gain at the oscillation frequency. These criteria are known as Barkhausen criteria for oscillation. Each delay stage must give a phase shift of π/N, where N is the number of delay stages. The remaining phase shift is provided by a direct current (dc) inversion. The simplified block diagram of single-ended RO is shown in Fig. 1. The RO with single-ended delay stage consists of odd number of stages which are necessary for the dc inversion.

The delay cells of the RO can be single-ended or differential [8]. Among them, the single-ended RO (SERO) is a chain of inverters composed of an NMOS and PMOS transistor, and the number of delay cells must be odd. The propagation time in this type of cell is set by the charge in each node and the current through the load that may consist of a resistor for fixed frequency or PMOS transistors.

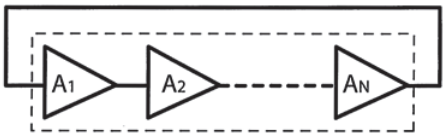
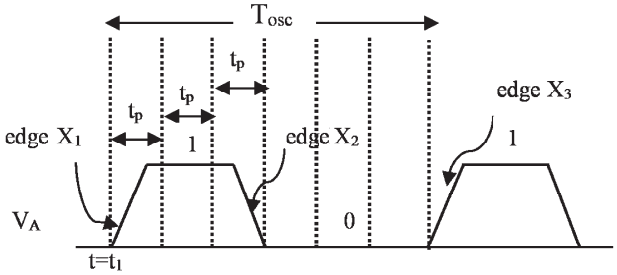


Figure 1 Single-ended ring oscillator block diagram structure



$$\text{Total phase shift in loop} = \pi$$
$$\text{Total propagation time in loop} = 3t_p$$
$$\therefore \frac{\pi}{2\pi} = \frac{3t_p}{T_{osc}} \Longrightarrow T_{osc} = 6t_p$$

Figure 2 Simple functional waveform and period calculation of the 3-stage SERO based VCO.

To explain the basic working principle of the SERO, let us consider a three-stage SERO (N=3), in which at time, t_1 the output of the first stage, voltage changes to logic 1 (denoted by edge X_1) as shown in signal waveform in Fig. 2. When this logic 1 propagates to the end, it creates a logic 1 at the third stage, which, when fed back

to the input of the first stage, creates a logic 0 in the first stage output denoting edge X_2. When this logic 0 is propagated again through the loop, it toggles the output voltage of the first stage and trigger edge X_3. For every single cycle, there is a downward as well as an upward transition, and the intrinsic propagation delay times of each delay cell, high-to-low (t_{PHL}) and low-to-high (t_{HPL}), are associated with these transitions. Nevertheless, t_{PHL} and t_{HPL} could be equal or not depending on the specific delay cell configurations, and so the average propagation delay can be implied by the arithmetic mean of transition times, $(t_{PHL} + t_{HPL})/2$.

Both single-ended and differential topologies can be used in designing fully integrated CMOS VCOs. Compared with the differential RO, the output stage of the SERO is always saturated. For this reason the SERO exhibits better PN performance for an equal number of stages while also consuming very low power [9], and shows superior thermal noise performance [10]. Moreover, it is easy to design for high frequency application.

2 Methodology

The oscillation frequency, f_o of the RO is primarily determined by the propagation delay time of the delay cells (T_d) and the number of delay stage (N) given by,

$$f_o = \frac{1}{2N \cdot T_d}. \quad (1)$$

Therefore, the easy technique to enhance the oscillation frequency is by reducing the number of stages and the propagation delay time. The number of delay stage will affect the performance of tuning range. In this work, three stages of single-ended structures are used so that the proposed VCO can attain higher frequency and wider tuning range compared to the differential architecture based VCOs. Moreover, it has better phase noise than differential ring oscillator for equal stages, frequency and power [9]. Control techniques of SERO based VCO can be performed by various methods, such as by changing loads, changing the strength of an inverter in the loop and varying the supply voltage. Our proposed design shown in Fig. 3 implements a three stage of RO structure in which the strength of an inverter is changed by adding two transistors (PMOS and NMOS). Generally this sort of topology of delay cell is known as the current starved inverter cell. In this RO, the delay of push-pull type element (i.e. inverter) is changed by changing the rate at which the total capacitance is charged. According to Fig. 3, an adjustable current source limits the peak current of the inverter and varies the delay time.

Theoretically, by using a minimum number of transistors and minimum stages of delay cells, it allows reaching the widest possible frequency. Difficulties of implementing resistors and capacitors in CMOS technologies caused the load tuning to be not widely used for single-ended ROs. Thus, PMOS transistors are used in this design as loads and NMOS tail transistors are used as control transistors.

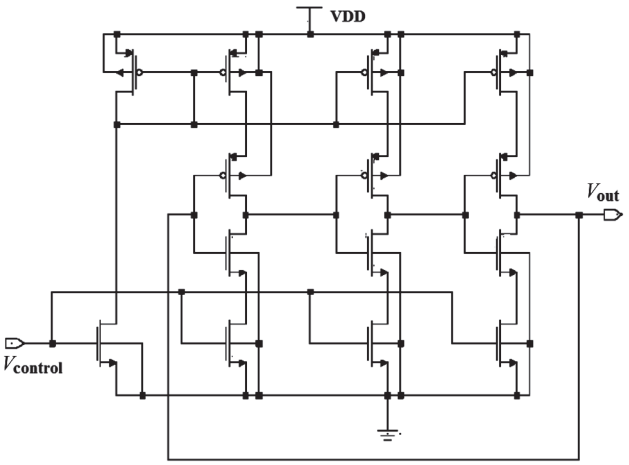


Figure 3 Schematic of the proposed single-ended ring oscillator

3 Results and discussion

The performances of the SERO based VCO circuit are determined by using simulation tools Design Architect (DA) and IC Station of Mentor Graphics in CEDEC 0,18 μm CMOS process. The width of all transistors is set to minimum size of 0,9 μm in order to get the highest frequency of the oscillator. A supply voltage of 1,8 V is utilized for low voltage applications. The proposed oscillator circuit must satisfy some specifications, such as wide tuning range, low power dissipation and low phase noise to realize in real applications. The transient analysis of this work is shown in Fig. 4. with a $V_{control}$ of 1 V. By changing the control voltage from 0,7 to 1,8 V, the frequency of the three-stage ring VCO varies between 2,4 GHz to 5,42 GHz as shown in Fig. 5. Fig. 6 shows a simulation result of the phase noise of −107,59 dBc/Hz at 1 MHz and −133,44 dBc/Hz at 10 MHz offset from the centre frequency 4,3 GHz. The better phase noise result has been achieved by employing three delay stages with fast switching operations, because phase noise increases by cascading more delay stages.

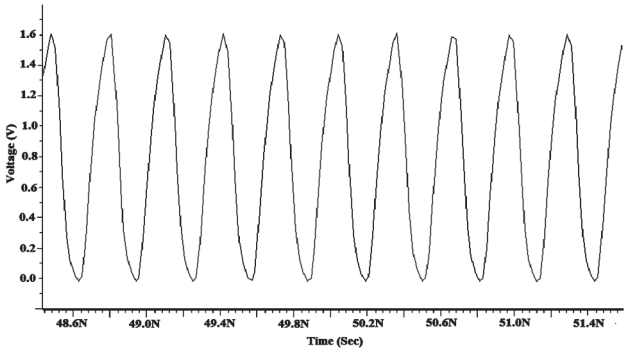


Figure 4 Transient analysis output of SERO

The simulation shows good frequency stability against power supply variations. The proposed VCO also consumes lower power, which is 664,551 μW. The layout of the circuit is shown in Fig. 7, and the total core chip area is 152,21 μm^2. The number of stage in this SERO is attractive not only for the purpose of operational speed but also for reducing the power dissipation and saving in the area for its IC fabrication.

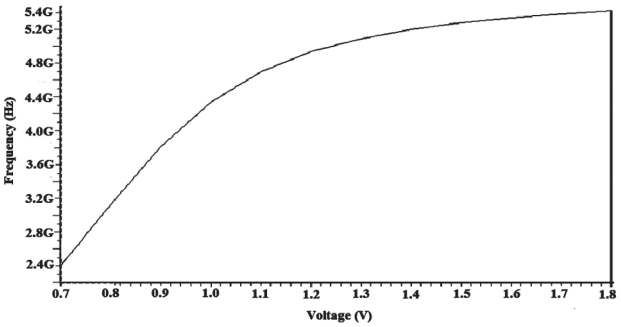


Figure 5 Frequency tuning range versus control voltage

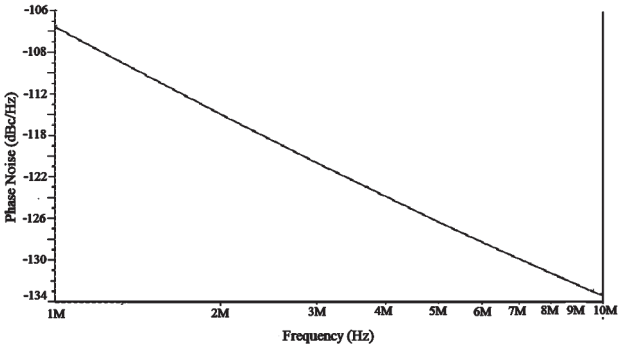


Figure 6 Single side-band phase noise performance

In Tab. 1, the performance of the post-layout simulation results of the proposed design is compared with previous research works of integrated ring oscillator. Despite dissipating very low power, the single-ended RO in this work oscillates at a higher and wider tuning frequency than those of [11], [12] and [13]. Though phase noise results of [5] and [11] are better in comparison with our design, they are operating at lower gigahertz range consuming considerable amount of power. Provided in [7], the figure of merit (FOM) of the proposed SERO based VCO can be calculated from the power dissipation and the phase noise of the simulated oscillation frequency as

$$FOM_{\mathrm{dB}} = L\cdot\Delta\omega + 10\cdot\lg\left(\frac{power_{DC}}{1\,\mathrm{mW}}\right) - 20\cdot\lg\left(\frac{\omega_0}{\Delta\omega}\right), \quad (2)$$

where $L{\cdot}\Delta\omega$ is the phase noise in $\Delta\omega$ offset frequency and ω_0 is the frequency of oscillation of the VCO. The achievable FOM is determined −182,19 dBc/Hz.

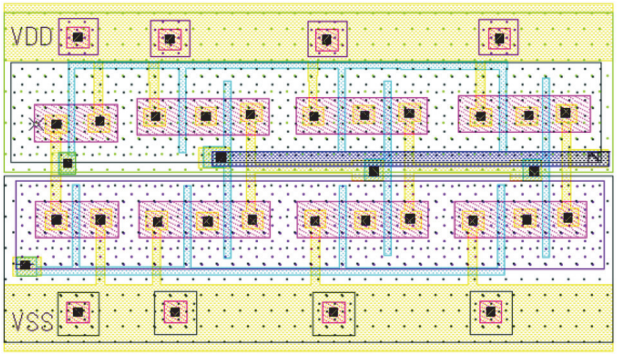


Figure 7 Core layout of the SERO

Table 1 Performance comparisons of CMOS ring oscillator based VCO

Parameters	This work	[5]	[13]	[12]	[11]
CMOS process / µm	0,18	0,065	0,13	0,13	0,35
Power supply / V	1,8	1	1,8	1,5	3,3
Tuning range / GHz	2,40 ÷ 5,42	0,4857 ÷ 1,0116	3,03 ÷ 5,36	7,3 ÷ 7,86	0,381 ÷ 1,15
Center frequency / GHz	4,3	0,645	5,22	7,64	0,866
Phase noise @ 1 MHz (dBc/Hz)	−107,59	−110,8	−107,7	−103,4	−126
Power dissipation / W	$641{,}33\times10^{-6}$	10×10^{-3}	100×10^{-3}	60×10^{-3}	$7{,}48\times10^{-3}$

4 Conclusion

In this paper, a wide tuning range of SERO based VCO is illustrated in a high frequency with a low power supply in 0,18-µm CMOS process. The oscillatory frequency becomes faster when the stage number of ring oscillator is smaller. The tuning range of the single-ended ring oscillator is from 2,4 GHz to 5,42 GHz while the control voltage is set from 0,7 V to 1,8 V. The best simulation of phase noise is achieved −107,59 dBc/Hz at 1 MHz from 4,3 GHz carrier frequency. The total power dissipation is 641,33 µW, and the core chip area is 152,21 μm^2. This SERO based VCO has reached higher and wider tuning frequency with a good phase noise and very low power dissipation compared to other works, and can be suitable for portable, multi-standard wireless devices.

5 References

[1] Dai, C. Y.; Zhou, J.; Nie, B.; Chen, K. A 60 GHz voltage-controlled oscillator with a 3.6 GHz tuning range in 180 nm CMOS technology. // Proceedings of Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics / Shanghai, 2009, pp. 93-96.

[2] Jasim uddin, M.; Nordin, A. N.; Reaz, M. B. I.; Bhuiyan, M. A. S. A CMOS power splitter for 2.45 GHz ISM band RFID reader in 0,18 µm CMOS technology. // Technical gazette. 20, 1(2013), pp. 125-129.

[3] Anand, S.; Razavi, B. A CMOS clock recovery circuit for 2.5-Gb/s NRZ data. // IEEE journal of solid-state circuits. 36, 3(2001), pp. 432-439.

[4] Song, H.; Kim, D. S.; Oh, D. H.; Kim, S.; Jeong, D. K. A 1.0-4.0-Gb/s all-digital CDR with 1.0-ps period resolution DCO and adaptive proportional gain control. // IEEE journal of solid-state circuits. 46, 1(2001), pp. 424-434.

[5] Kim, J. -M.; Kim, S.; Lee, I. -Y.; Han, S. -K.; Lee, S. -G. A low-noise four-stage voltage-controlled ring oscillator in deep-submicron CMOS Technnology. // IEEE transactions on circuits systems II: express briefs. 60, 5(2013), pp. 71-75.

[6] Ciu, H. C.; Cheng, C. S.; Yang, Y. T.; Wei, C. C. A 10 GHz low phase noise CMOS voltage controlled oscillator using dual-transformer technology. // Solid-state electronics. 52, 5(2008), pp. 765-770.
[7] Jalil, J.; Reaz, M. B. I.; Ali, M. A. M. CMOS differential ring oscillator: Review of the performance of CMOS ROs in communication systems. // IEEE microwave magazine. 14, 5(2013), pp. 97-109.
[8] Abidi, A. A. Phase noise and jitter in CMOS ring oscillators. // IEEE journal solid-state circuits. 41, 8(2006), pp. 1803-1816.
[9] Hajimiri, A.; Limotyrakis, S.; Lee, T. H. Jitter and phase noise in ring oscillators. // IEEE journal of solid-state circuits. 34, 6(1999), pp. 790-804.
[10] Toh, Y.; McNeill, J. A. Single-ended to differential converter for multiple-stage single-ended ring oscillators. // IEEE journal solid-state circuits. 38, 1(2003), pp. 141-145.
[11] Thabet, H.; Meillere, S.; Masmoudi, M.; Seguin, J. L.; H. Barthelemy, H.; Aguir, K. A low power consumption CMOS differential ring VCO for a wireless sensor. // Proceedings of 9th IEEE International New Circuits and Systems Conference (NEWCAS) / Bordeaux, 2011, pp. 81-84.
[12] Liu, H. Q.; Goh, W. L.; Siek, L.; Lim, W. M.; Zhang, Y. P. A low noise multi GHz CMOS multiloop ring oscillator with coarse and fine frequency tuning. // IEEE transactions on very large scale integration (VLSI) system. 17, 4(2009), pp. 571-577.
[13] Tiao, Y. S.; Sheu, M. L. Full range voltage-controlled ring oscillator in 0.18-µm CMOS for low-voltage operation. // Electronics letter. 46, 1(2010) pp. 30-32.

Authors' addresses

Jubayer Jalil
Faculty of Engineering and Built Environment
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 Bangi, Selangor, Malaysia
E-mail: jubayer.jalil@gmail.com

Mamun Bin Ibne Reaz, Professor
Faculty of Engineering and Built Environment
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 Bangi, Selangor, Malaysia
E-mail: mdmamun.reaz@gmail.com

Siti Sarah Binti Md Sallah
Faculty of Engineering and Built Environment
Department of Electrical, Electronic and Systems Engineering
Universiti Kebangsaan Malaysia
43600 Bangi, Selangor, Malaysia