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EVOLUTION OF DIGITALLY CONTROLLED OSCILLATORS

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Subject review
Current trend of using digital or all-digital phase-locked loops (PLLs) in various communication devices introduces the usage of digitally controlled oscillator (DCO). This review paper discusses the evolution of DCOs in modern electronic devices as well as their performances in local oscillators. Even though the DCO implementation is preferable to its analog counterpart, improvements are still going on to get high performances in terms of power consumption, speed, chip area, frequency range, supply voltage, portability and resolution. This paper mainly describes the evolution of DCO, how it turns from a conventional VCO to DCO for deep-submicrometer CMOS process. The focus is to analyse and track the advances in DCO base on its performance level.

Keywords: *All-Digital PLL (ADPLL), Complementary Metal Oxide Semiconductor (CMOS), Digitally Controlled Oscillator (DCO), Digital PLL (DPLL)*

Razvoj digitalno kontroliranih oscilatora

Pregledni članak
Suvremeni razvoj uporabe digitalnih ili potpuno digitalnih ciklusa s faznim podešavanjem (PLLs) u različitim uređajima za komunikaciju vodi ka primjeni digitalno kontroliranog oscilatora (DCO). U ovom se preglednom članku daje razvoj DCO-a u modernim elektroničkim uređajima kao i njihovo funkcioniranje u lokalnim oscilatorima. Iako se implementacija DCO preferira u odnosu na analogne, i dalje se radi na poboljšanjima u potrošnji energije, brzini, veličini čipa, raspona frekvencije, ulaznog napona, prenosivosti i rezolucije. U radu se uglavnom opisuje razvoj od oscilatora kontroliranih voltažom (voltage controlled oscillators- VCO) do digitalno kontroliranih oscilatora za "deep-submicrometer CMOS" postupak. Fokus je na analizi i praćenju unapređenja DCO-a na razini funkcionalnosti.

Ključne riječi: *digitalno kontrolirani osciloskop (DCO), digitalni PLL (DPLL), dopunski metal oksid poluvodič (CMOS), potpuno digitalni PLL(ADPLL)*

1 Introduction

Oscillators are designed to oscillate the frequency range used in synthesizers or local oscillators. The oscillation frequency needs to be controlled by an input as desired depending on the corresponding applications. In analog PLL, the oscillation frequency is controlled by a voltage input which is in analog form. This form of oscillators is called voltage controlled oscillator (VCO). VCOs are extensively used in CMOS technology. As the technology of CMOS scaling improves from decade to decade, CMOS process is called deep-submicrometer or down-sizing. CMOS deep-submicrometer became very cumbersome to be implemented in the traditional form of VCO which uses passive devices. This issue was provoked because its highly non-liner frequency versus voltage characteristics and low-voltage headroom make it susceptible to the power/ground supply and substrate noise [1]. Thus, a low-voltage frequency tuning for deep-submicrometer CMOS oscillator was very difficult to achieve. Besides, the CMOS down-sizing causes the supply voltage to be reduced as well, but it is inevitable in order to avoid breakdown and reliability issues. Moreover, the extreme high cost and power consumption made the manufacturers to handle a high risk at that time.

To overcome these issues a digital sensitive approach can be implemented to control the frequency of oscillation in a deep-submicrometer CMOS process [2]. Finally, VCO was replaced by DCO. The only change in DCO is that the comparator in the ramp core of VCO is replaced with reset pulses generated from a counter or microprocessor. DCO produces a stable digital frequency with smooth tuning.

The trend using DCO, which is fully digital-intensive approach, is increasingly popular from time to time. Digital circuits are more preferable than analog circuits because it suits well to CMOS process. Introducing fully digital-intensive approach benefits the CMOS field in terms of cost, size, flexibility, reliability and power consumption [3].

The DCO allows efficient implementation of direct frequency modulation with an all-digital phase locked loop (ADPLL) with a digital control [4]. It is a key component for the high performance fully-integrated ADPLL architecture, which enables system-on-a-chip (SoC) implementation of wireless systems [5, 6]. The programmability of digital circuits is highly desirable for software defined radios, discrete-time receivers for Bluetooth radios and transmitters for mobile phones.

2 Background

Oscillator related to CMOS field was having a serious issue in designing polyphonic synthesizers in the early 1980s. VCO designs with monophonic synthesizers uses a low amount of oscillators causing musical instruments a hard time in tuning stability. When manufacturers introduced polyphony synthesizers by designing VCOs with a large number of oscillators, tuning problems became worse and it was very costly. This severe problem came to an end by introducing DCOs in the market. DCO was a cheaper, more reliable and stable oscillator design. The DCO was desired by most manufacturers at that time as an improvement over the unstable tuning of VCOs. VCO and DCO share the same limited range of waveforms and the same ramp core. The analogue wave shaping for DCO was the same as VCO, but there were vast simplicity and arbitrary waveforms of digital systems, such as direct digital synthesis. This development then led to the vast use of fully digital oscillator designs in musical instruments.

Nowadays, the digital baseband (DBB) design constantly migrates to the most advanced deep-

submicrometer digital CMOS process available, which usually does not offer any analog extensions and has very limited voltage headroom [4]. Unfortunately, the design flow and circuit techniques required are analog intensive and utilize process technologies that are incompatible with a DBB [7]. Deep-submicrometer CMOS processes present new integration opportunities on one hand, but make it extremely difficult to implement traditional analog circuits, on the other. For example, frequency tuning of a low-voltage CMOS analog oscillator is an extremely challenging task due to its highly nonlinear frequency versus voltage characteristics and low-voltage headroom making it susceptible to the power/ground supply and substrate noise. In such low supply voltage case, not only the dynamic range of the signal suffers but also the noise floor rises, thus causing even more severe degradation of the signal-to-noise ratio. Circuits designed to ensure proper operation of RF oscillators depend on circuit techniques that operate best with long-channel, thick-oxide devices with supply voltage of 2,5 V or higher, otherwise DCO could be good alternate choice for low voltage design.

VCO of analog frequency tuning is not compatible with deep sub-micron CMOS [3] and the reasons can be summarized as below:

- Varactors are highly non-linear
- Voltage headroom is squeezed
- Analog voltage resolution is unreliable
  - Analog interface is difficult for integration (with limited number of oscillators)
- Low supply voltage causes breakdown and reliability issues.

2.1 MOS Varactor

Varactors are used in voltage controlled capacitors as part of PLL and frequency synthesizers. For example, varactors are used in the tuners of television sets to tune electronically the receiver to different stations.

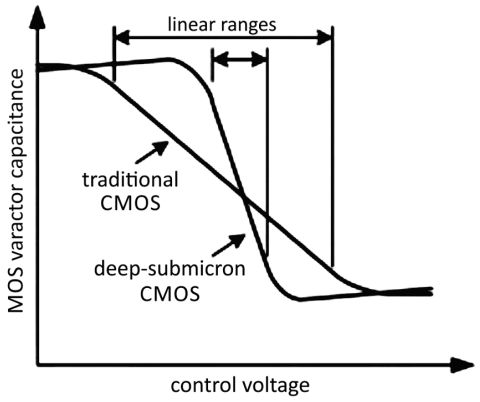

Figure 1 MOS varactor capacitance characteristics in traditional CMOS [7]

2.2 Overview of DCO and its circuit core

DCO is designed so that the oscillator is controlled digitally. To control the frequency range of oscillator using a digital-intensive approach, digital control words in binary bits are fed into the oscillator. These digital control words are integrated in a DCO core to control the frequency range of oscillator. Figure 2 shows the schematic diagram of LC-DCO core which consists of LC tanks in the three varactor banks and a NMOS-only cross-coupled pair.

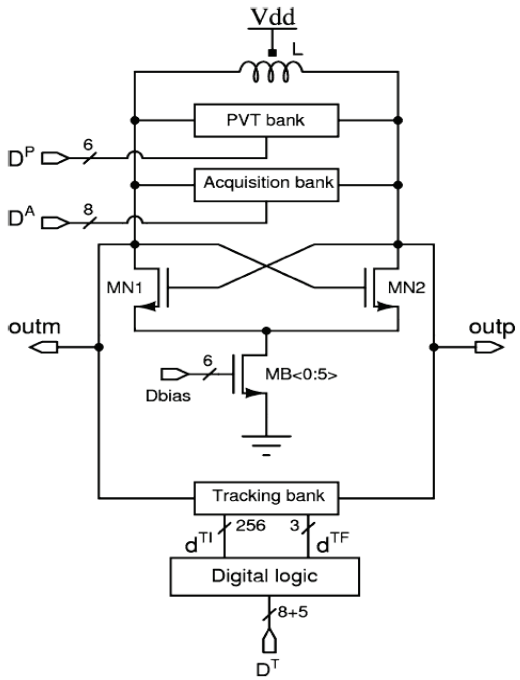

Figure 2 LC-topology of DCO core [4]

2.2.1 LC tank

Varactor array is segmented into three banks which are process/voltage/temperature (PVT) calibration bank, acquisition bank and tracking bank. Each bank consists of a LC tank which comprises an array of capacitors. The amount of capacitor depends on the amount bits in a digital control word. If the control word has 8 bits, then 8 capacitors are used. Figure 3 shows the LC tank inside the segmented varactor array. PVT bank becomes active when cold power rises. Acquisition bank is active during channel selection. Tracking bank is active during transmission and reception [7].

LC tank plays an important role in oscillation frequency and phase noise performance. The tank inductance and capacitance determines DCO oscillation frequency. The frequency range of oscillator is controlled by the LC tank design. To stay tuned with the advance CMOS technology, the LC circuit design is improved on the conventional DCO.

2.2.2 Other components in DCO core

In cross-coupled NMOS pair is the active device to realize the negative resistance, which compensates for the LC-tank loss [4]. For the implementation of deep-submicron process the cross-coupled pair of transistors needs to have sufficient small-signal transconductance at a given bias current to fulfil the start-up condition of the oscillator. Large transistors limit the tuning range of the oscillator caused by increased parasitic capacitance. It is found that transistors with minimum channel length cause noise in the oscillator [4].

The 6-bit digital input through the bank of NMOS transistors used as switches controls the current consumption [8]. Biasing current is digitally tuned for performance optimization. This shows that DCO performs better than VCO in tuning stability.

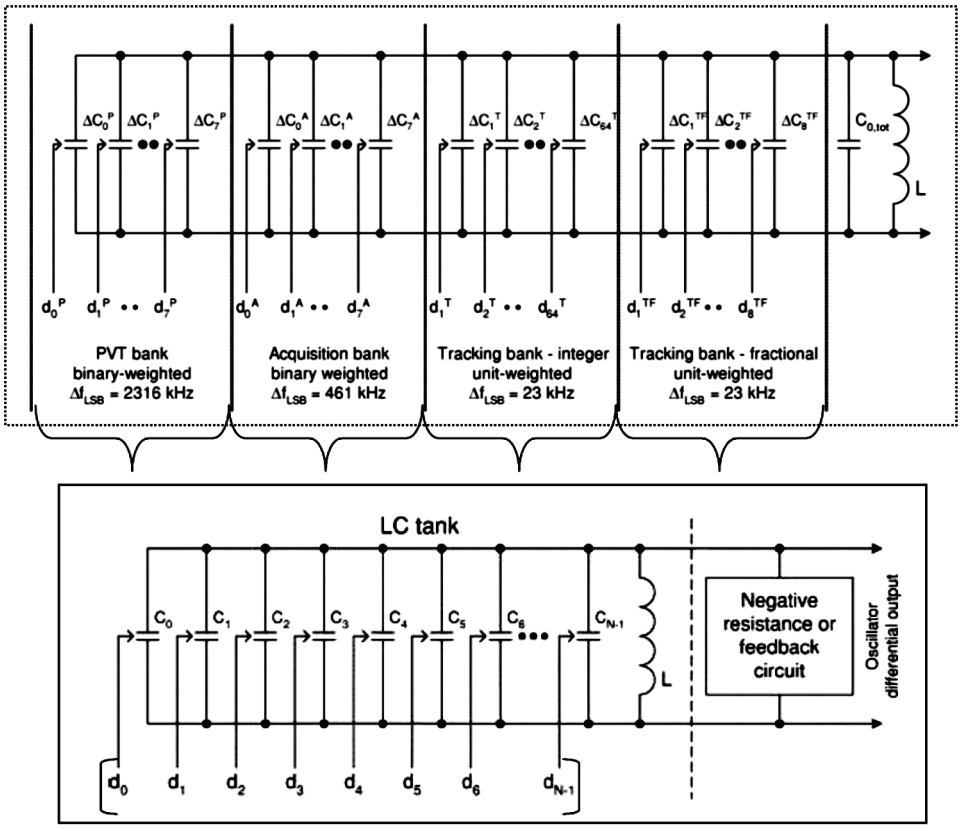

Figure 3 LC tank in each of the four varactor banks [4]

3 DCO performance

The evolution of DCO performance is based on CMOS scaling, supply voltage, resolution, power consumption and frequency tuning range. The performance evolution for each parameter base on proposed researches is described below.

3.1 Technology scaling

Downsizing of CMOS components has been the driving force for DCO evolution. The CMOS technology development has been advanced with the downscaling of component size since the replacement of vacuum tubes with transistors few decades ago. This advanced technology process which leads to deep-submicrometer CMOS benefits a lot to the circuit characteristics. Now, we are able to integrate millions of CMOS transistors in nano-scale in a silicon chip with few centimetres square. As the technology advances, the latest microprocessor operates at 3 GHz and is expected to increase further as well as RF communication devices [10, 11].

3.2 Supply voltage in DCO implementation

Supply voltage is the most important reason for the replacement of VCO with DCO. Supply voltage is the operating voltage for any oscillator. When the CMOS downscaling was brought into the electronic field, the supply voltage also needed to be reduced. Reduction of supply voltage in an analog-intensive circuit causes breakdown and reliability issues. Thus, the supply voltage must be small in order to achieve a high performance level. ADPLL uses the cell-based design approaches other than LC or RC based, so it can be easily integrated into the digital system [16 ÷ 19].

3.3 Resolution in DCO implementation

High resolution for oscillators is important in order to receive a fine tuning especially in musical instruments. Table 1 explains the improvement on resolution for the last 10 years with the proposed algorithms and their achievements.

DCV cells have good performance in resolution and linearity. Besides DCV, DCM or the combination of both DCV and DCM are also exploited to build the fine-tuning stage. Generally, for simple driving capability modulation (DCM), the driving current of each delay cell is changed by controlling number of enabled tri-state buffers/inverters. Although this design concept is straightforward, it has a poor performance in linearity and power consumption, and the resolution is insufficient as well [11, 22]. A new approach of varactor-interpolator fine-tuning stage (VIFST) introduced in [23], where cell-based DCO has been realized to achieve better monotonic response, has a very high frequency resolution and simple circuitry. Here, the VIFTS consists of digitally-controlled varactors (DCVs), dummy DCVs and an interpolator. In DCV, the gate capacitance is changed slightly by the

control code to get high delay resolution. In this type of DCO, cascading structure is adopted to preserve the control code resolution and extending operating frequency range.

3.4 Power consumption in DCO implementation

Power consumption of DCO should be reduced to save overall power dissipation to meet low power demands in SoC designs. ADPLL has a major disadvantage of large power consumption and 50 % of total power is contributed by DCO [18]. Power consumption is very important in portable battery operated devices. Thus, power saving has become major design concern in modern electronic devices. Table 2 shows the improvement in power consumption in recent years. As the time passes, the power consumption has been reduced by improving the circuit design.

Low power requirements continue to be demanding for consumer and various different applications. All DCOs in PLLs being manufactured today require a cost sensitive power aware energy efficient design that can enable better systems. Developing the CMOS technology and design to support very low power operations is very challenging due to increasing device variations and random fluctuations. So, we not only rely on the improvement of technology, but have to look for novel circuit techniques and circuit topologies.

Table 1 Comparisons of resolution in DCO implementation

Ref. No.	Year	Algorithms	Achievements
[19]	2002	Shunt capacitor technique-fine tune the capacitance loading	High resolution but non-linear
[18]	2003	Uses an inverter ring	Insufficient resolution for most applications
[20]	2003	Uses a bank of tri-state inverter buffers	Delay resolution can be controlled by the number enable buffers but uses a large silicon area and high power consumption
[3]	2003	Shunt capacitor technique	High resolution
[21]	2004	Uses of a fixed capacitance loading	High resolution
[12]	2005	Uses of digitally controlled varactor (DCV)	Good performance but high power consumption
[22]	2011	Employing DCV & hysteresis delay cell (HDC)	High resolution with fine tuning
[23]	2012	Varactor-interpolator fine-tuning stage	Very high resolution

Table 2 Comparisons of power consumption in DCO implementation

Ref. No.	Year	Algorithms	Achievements, mW
[19]	2002	Shunt capacitor technique	1
[20]	2003	Uses a bank of tri-state inverter buffers	164
[16]	2003	Uses inverter ring	100
[12]	2005	Uses digitally controlled varactor (DCV)	18
[14]	2008	Base on a ring oscillator implemented with Schmitt trigger based inverters	2,3
[23]	2010	Driving strength controlled delay with two NAND gates as inverters	0,7
[15]	2011	Low power Schmitt trigger inverters	0,5677

The advanced DCO have an improvement to increase the delay tuning range using binary controlled pass transistor arrays and Schmitt trigger based inverters [15]. The Schmitt trigger based inverter has a higher V_{M+} (low to high switching threshold) and lower V_{M-} (high to low switching threshold) compared to the conventional inverters as shown in Fig. 4. Thus, the advance DCO circuit provides the same tuning range with smaller capacitance loading, which is useful for power consumption reduction. Furthermore, in conventional DCO circuit, the slope of the input signal to each stage decreases gradually due to the large delay between each stage. The steep slope of the output signal from the Schmitt trigger based inverter minimizes this problem to a certain extend.

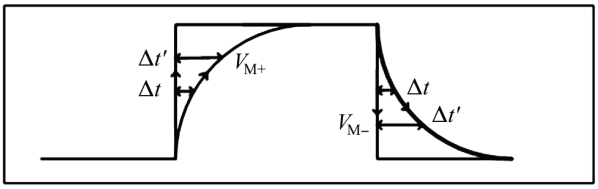

Figure 4 Delay comparison of Schmitt inverter and conventional inverter [15]

3.5 Frequency tuning range in DCO implementation

Direct-frequency-synthesizers-based DCOs require a high frequency or a multiple-phase clock. Nature of frequency generation causes difficulty to the DCOs to operate at high frequency range. Tab. 3 shows the performance of frequency tuning range.

Table 3 Comparisons of frequency tuning range in DCO implementation

Ref. No.	Year	Approaches	Achievements
[25]	2002	Ring DCOs	Hardly operate in gigahertz because the digital frequency tuning units normally slow down the oscillation significantly
[21]	2004	Combination of digital to analog converter (DAC) and a ring-based VCO	Operating in gigahertz but the analog control signal degrades the phase noise performance
[1]	2005	LC tank oscillator	First multi-gigahertz DCO for wireless application 2,4 GHz
[4]	2006	Improved LC tank oscillator	Generation of 3,2 GHz
[26]	2007	Incrementally-sized fine bank	3,05 GHz ÷ 3,65 GHz
[27]	2012	4 × LC core	5,6 GHz ÷ 11,5 GHz

Typical digital CMOS processes do not provide high-quality inductors, and inductors occupy a large area. However, use of different technique and novel circuit structure improves DCO's wide tuning operation. Recently, various DCOs of ring topology have been developed to achieve a wide frequency range with a hierarchical structure using a coarse delay stage and a fine delay stage likewise other LC oscillators.

4 Discussion and concluding remarks

A brief performance analysis of the latest advancements on the design of DCOs helps to find out the subject matters where most of the design effort needs to be put for the development of the circuit. Submicron CMOS quadrature DCO based on LC resonator tank can easily be operated at gigahertz frequencies and its phase noise performance is the best compared to ring counterpart. However, for wide tuning range with optimum power, the ring based DCO is a suitable choice for chip designers. As far as portability is concerned, only cell-based DCO can easily be ported to multiple processes in a short time and this approach is also cost-effective in VLSI design. Moreover, in cell based DCO, it is achievable the effect of supply voltage reduction on the choice of the oscillator topology to any downsizing CMOS process.

A short review on DCO for both DPLL and ADPLL in communication discipline has been presented. The main design trade-offs between frequency resolution, tuning range and power have been described. Evolution of DCO gives a big change in the performance of the oscillator. As time migrates to advance CMOS technologies, improvements on the DCO lead to high level of performance and it is because of the oscillator's fully controlling of digital-intensive method. DCO performs better in terms of power consumption and frequency tuning range. DCO gives a linear tuning especially in musical instruments, however, it has potential application in RF transceivers if wide tuning range and small frequency resolution can be attained. Hence, DCO will be improved more in future in line with the advance CMOS technology for a better performance. As advances in down-scaling CMOS technology allow for smaller transistors, the trade-offs in the design of DCO need to be studied and exploited in the never ending search for faster and low power DCO implementation.

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