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TESTS OF IEEE 1588-BASED SYNCHRONIZATION SYSTEM IN SUBSTATION

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Original scientific paper
As a synchronization method, IEEE1588 standard has been applied in substation, it should be tested and verified ensure synchronization accuracy and node interoperability. A comprehensive testing method for the IEEE1588 is proposed in this paper. Furthermore, IEEE1588 clock testing platform is built to support the proposed testing method. Based on the analysis of the clock synchronization error and the performance testing principle method, the accuracy and stability of master clock and slave clock were evaluated. Secondly, the conformance testing to adopt performance response was achieved by designed specific case, based on the above, and then to analyse the conformance implementation details. According to testing requirements, test bed designed. Finally, the experiment based on substation devices was carried out using the IEEE1588 clock testing platform. The feasibility of the proposed methods was further verified with the testing results.

Keywords: *conformance testing; device under test (DUT); IEEE 1588; performance testing; precision time synchronization; substation*

Testovi sinkronizacijskog sustava u trafostanici utemeljeni na IEEE 1588

Izvorni znanstveni članak
Kao metoda sinkronizacije, IEEE1588 norma je primijenjena u trafostanici, to bi trebalo osigurati ispitanu i provjerenu sinkronizacijku točnost i čvora interoperabilnosti. Metoda sveobuhvatnog testiranja za IEEE1588 se predlaže u ovom radu. Nadalje, IEEE1588 platforma testiranja ure izgrađena je kao podrška predložene metode ispitivanja. Na temelju analize sinkronizacije pogreške ure i metode ispitivanja načela značajke, ocjenjene su točnost i stabilnost glavne ure i pomoćne ure. Drugo, ispitivanje usklađeno s normom za usvajanje odziva značajke je postignuto dizajniranjem konkretnog slučaju, na osnovi navedenog, a potom analizirati pojedinosti provedbe sukladnosti. Prema zahtjevima ispitivanja, dizajnirana je testna osnovna ploča. Konačno, pokus utemeljen na uređajima transfostanice proveden je uporabom IEEE1588 platforme testiranja ure. Izvedivost predloženih metoda dodatno je potvrđena s rezultatima testiranja.

Ključne riječi: *tispitivanje usklađenosti; ispitivanje značajke; precizna sinkronizacija vremena; trafostanica; uređaj pod testom (DUT)*

1 Introduction

The nodes, deployed in different locations of distributed measurement and control systems, will track certain physical phenomenon and make respective control decision by data collection and information fusion. Whereas, these control decisions are premised on system clock synchronization. For instance, control command depends on synchronous monitoring data of each node in various networks [1-3]. Therefore, clock synchronization plays an important role in these systems [4-5].

There are a variety of synchronization ways in the power control system, such as Network Time Protocol (NTP), IRIG-B, GPS and so on. However, these ways have some deficiencies. For example, the accuracy of distribute clocks at either end of network is millisecond due to the fact that NTP runs on clients and servers only by software implementation. Moreover, the dedicated cabling, increasing deployment and maintenance costs, is necessary for IRIG-B to deliver the timing signals. The methods mentioned above do not provide compatibility. GPS, using satellite signals to realize time synchronization, is unavailable in the underground and indoor environments [6]. However, high-accuracy standardization for time synchronization in substation network is necessary. The IEEE 1588 precision time protocol (PTP) provides not only sub-microsecond synchronization accuracy in a standard method but also compatibility and interoperability between heterogeneous systems. These characters can enable many sophisticated extensions of power applications. It seems to be a promising way to handle the synchronization requirements of the substation network [7-8].

The node time character should be tested to ensure its interoperability and quality in IEEE 1588-Based Substation network [9-10]. Nevertheless, there are few researches on the test of IEEE 1588-Based Synchronization System. The conformance testing of ordinary clocks which realizes major common protocol functions was discussed in [11]. In [12], an IEEE 1588 testbed was established to check the character of the system and verify its devices accuracy. In order to evaluate the influence of synchronization accuracy caused by environmental temperature change and network load increased, the external factors influencing the synchronization system were tested by reproducible method in [13].

Therefore, the researches mentioned above have some defects such as:

1) The testing method is not comprehensive. For instance, the clock stability is not measured and the performance response is neglected.

2) The test object is single, and the transparent clock and the master clock are rarely involved.

3) The insufficient test instrument makes the test carried out by simple software and oscilloscope implementation, difficult.

According to the characteristics of the IEEE1588 clock synchronization protocol and the aforementioned study, a test method combining performance testing with conformance testing is proposed in this paper. And an IEEE1588 clock test bed is designed to satisfy the synchronization system test demand. Based on the flexible configuration, a comprehensive test of the clock node was carried out.

The rest of the paper is organized as follows. The principle and testing requirement of IEEE 1588

Synchronization System in substation network is presented in Section 2. In Section 3, the test method for clock accuracy and stability is introduced, and the transparent clock resides time test method is analysed. In Section 4, the conformance testing method combined with the performance testing is developed on the basis of the typical testing case. Lastly, an IEEE1588 clock test bed is designed. The test results for substation devices are demonstrated and analysed in Section 5. The conclusion is provided in Section 6.

2 Principle and tested analysis of IEEE1588

IEEE 1588 is a precision clock synchronization protocol. It is applicable to local area network of measurement and control system. IEEE 1588-Based Synchronization System includes ordinary clock, transparent clock and boundary clock (power industry prefers transparent clock) [14]. The systems connect clock nodes by Ethernet and use clock synchronization mechanism to realize sub-microsecond accuracy.

2.1 Synchronize mechanism of IEEE1588

With the cooperation of software and hardware, the system will record the transmission time and reception time and add time stamp to each message. Hence, receiver will calculate the time error and path delay and then realize the synchronization of slave clock and master clock [15].

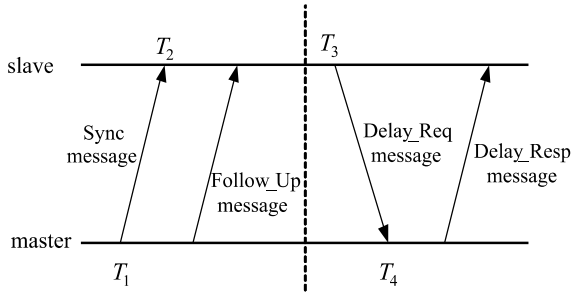

Figure 1 Structure of system communication

The system adopts master-slave level to realize clock synchronization, as shown in Fig. 1. Firstly, master clock periodically transmits Sync message (once every second). Then the master records the Time Stamp of transmission (T_1). When the slave clock receives the Sync message, it will record Time Stamp of transmission (T_2). Afterwards the master clock transmits the Follow_up Message, including the transmission time of Sync message (T_1). Suppose the path delay is T_{Delay}, T_{Offset} can be calculated as

$$T_{\text{Offset}} = T_2 - T_1 - T_{\text{Delay}}, \tag{1}$$

In fixed network structure and low network load change system, path delay T_{Delay} changes little [7]. As shown in Fig. 1, slave clock transmits Delay_Req message to master clock and records its transmission time T_3. After receiving the Delay_Req message, the master clock will record the receive time T_4. The master clock then will transmit Delay_Resp message T_4, T_{Delay} can be calculated as

$$T_{\text{Delay}} = T_4 - T_3 - T_{\text{Offset}}. \tag{2}$$

Combining Eqs. (1) and (2), we can get

$$T_{\text{Offset}} = \frac{(T_2 - T_1) - (T_4 - T_3)}{2}, \tag{3}$$

$$T_{\text{Delay}} = \frac{(T_2 - T_1) + (T_4 - T_3)}{2}. \tag{4}$$

Based on Eqs. (3) and (4), the data of T_{Offset} and T_{Delay} can be get. Then, the slave clock can be modified to master clock. This synchronization method separates the measurement and transmission of the message to make the time stamp more precise. The system clock can reach the sub-microsecond accuracy under the special hardware implementation.

2.2 Tested analysis of IEEE1588

Since the protection and control function of substation are utterly depending on simultaneous monitoring data, the precise clock synchronization plays a significant role in substation network, and IEEE 1588-Based Synchronization System can satisfy the system requirement. The application structure of substation network based on IEEE1588 is shown in Fig. 2. In this mode, system node includes master clock, slave clock and transparent clock. Compared with NTP standard, IEEE1588, which has the similar design concept and operation, is a more advanced, complex standard and its precision is higher than NTP while the timing performance of IEEE1588 heavily depends on the network condition and implementation architectures, such as components, network load and network configuration.

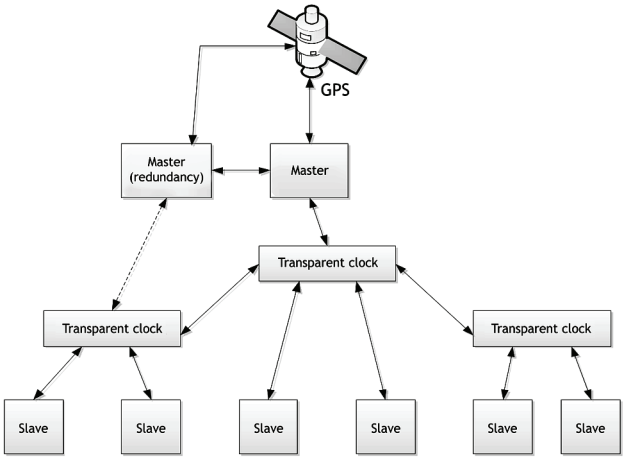

Figure 2 Structure of IEEE 1588-based synchronization system in substation network

The analysis of IEEE1588 principle and implementation mechanism shows that many factors influence clock synchronizing system performance [16]. Main factors are shown below: protocol stack delay fluctuation, communication path delay asymmetry, time stamp accuracy, network components delay fluctuations,

stability problem and so on [15]. We can conclude that there are 3 kinds of problems: 1) node clock realization technologies; 2) protocol conformance; 3) the influences of external factor. Paper [13] discusses and tests external factor influence such as temperature change, network load, etc. As a result, the system testing in this paper focuses on protocol conformance testing and clock performance, analysis of internal factors affects synchronization performance and measures time accuracy and stability.

3 Performance testing

In substation network, IEEE 1588-based synchronization system includes various clock types and their performance affects system function. The precision and stability are most important issues for master clock and slave clock while the important issue for the transparent clock is the resident time.

Clock performance can be judged by clock expected precision and clock stability. The time interval error (TIE) and time deviation (TDEV) are therefore appropriate index [17]. TIE is the relative time delay of given tested clock signal and ideal clock signal in the specific time period. The TIE of tested device can be obtained from the following:

$$TIE(t,\tau)=\left[x(t+\tau)-x(t)\right]. \tag{5}$$

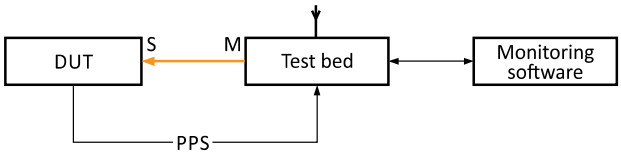

Figure 3 Structure of IEEE1588 test

The test structure is presented in Fig. 3. DUT achieves clock synchronization with test bed through network, and the pps accesses test bed, Monitoring software calculates the expected precision and stability analysis of DUT clock.

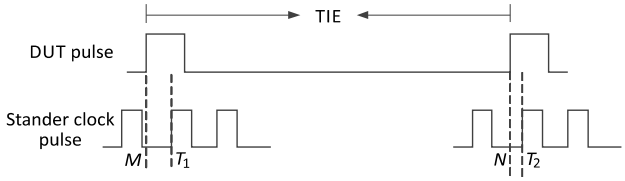

Figure 4 Principle of TIE test

The time interval error (TIE) measuring principle is illustrated in Fig. 4. The standard clock frequency of test bed is f_0, corresponding to the period $T_0 = 1/f_0$. Counting the pulse number M and Nat the rising edge of the CUT pulse, T_1 and T_2 are the time interval between the rising edge of CUT pulse t with rising edge of the standard clock pulse. Then, the measurement pulse time interval T_x is:

$$T_x=\left(N-M\right)\cdot T_0+T_1-T_2. \tag{6}$$

However, according to the pulse number, the test time interval is

$$T_x=\left(N-M\right)\cdot T_0. \tag{7}$$

Based on the above analysis, we can get the DUT time interval error. The measurement error obtained from Eqs. (6) and (7) is $\Delta=T_1-T_2$, and the maximum value is one quantization clock cycle T_0 due to the fact that the rising edge of CUT is inconsistent with the rising edge of stander clock and there is time scale error. Therefore, we can get

$$\Delta T'_x=\Delta\left(N-M\right)\cdot T_0+\left(N-M\right)\cdot\Delta T_0. \tag{8}$$

Combining Eqs. (7) and (8), we have：

$$\frac{\Delta T'_x}{T'_x}=\frac{\Delta\left(N-M\right)}{\left(N-M\right)}+\frac{\Delta T_0}{T_0}. \tag{9}$$

Based on the principle of pulse count, $\Delta\left(N-M\right)=\pm1$, $N-M=T'_x/T_0$, then:

$$\Delta T'_x=\pm T_0+T'_x\cdot\frac{\Delta T_0}{T_0}. \tag{10}$$

From Eq. (10), test accuracy is affected by test bed standard clock frequency. Improving the clock frequency and stability can effectively reduce error. Therefore, rubidium atomic frequency standard is introduced in the test bed design to improve test precision.

Based on the TIE, we can analyse the clock stability [18]. Time deviation (TDEV), which is used to describe the fluctuation of frequency source, is the most common measure of time stability. It is calculated with Eq. (11) [19].

$$TDEV(n\tau_0)=\sqrt{\frac{1}{6n^2(N-3n+1)}\sum_{j-1}^{N-3n+1}\left[\sum_{i=j}^{n+j-1}\left(\chi_{i+2n}-2\chi_{i+n}+\chi_n\right)\right]^2}. \tag{11}$$

$n=1,2,\ldots$, inter part

Time error and time deviation are closely connected and demonstrate clock performance from different angles. The clock precise error and stability can be estimated with time error and time deviation test.

4 Conformance testing

Conformance Testing is the key point to ensure the realization of IEEE1588. For the convenience of conformance testing, some industries have made the related industrial specification. Aiming at substation，IEEE PC37.238 specification has been introduced to ensure interoperability and deterministic control of power devices [20].

Conformance testing can be divided into two categories: 1) IEEE 1588 inner mechanism test 2) IEEE 1588 specification test. Paper [9] and [10] have carried out conformance testing to the BMC partial algorithms and protocol specifications, such as Testing for Invalid

Delay_Resp Messages, testing for invalid Follow_Up Messages and testing for attribute value。

However, these literatures adopt pc-clock realized by software to test and estimate the conformance of protocol according to message information. They have the following defects: 1) The test should be completed depending on master clock, oscilloscope and other equipment. 2) Conformance testing and performance testing are isolated, and the protocol conformance is not analysed based on the tested clock performance. Therefore, test bed based on hardware clock is designed in this paper according to the judgment of message logic to combine the performance testing and conformance testing.

4.1 Conformance testing method

There are three test types of interactive interface and DUT in testing system: IEEE1588 event message, IEEE1588 management message and PPS of DUT. Applying excitation at the interface of DUT and observing the response are necessary for the conformance testing of IEEE1588 protocol.

In synchronization system, an important method for applying excitation in conformance testing is the test bed messages. Clock test bed is set by PC monitoring software and sent excitation message according to designed testing case while tested response can be reflected by message information and clock performance. As one DUT response, IEEE1588 message communication is the foundation of system operation. Test bed should equip the ability of message acquisition and accordingly to judge the correction of message logical processing of tested equipment. Meanwhile, it also should equip the ability of performance testing, evaluate whether the clock accuracy of tested clock coincides with excitation. Conformance testing is realized on the basis of the above two testing methods.

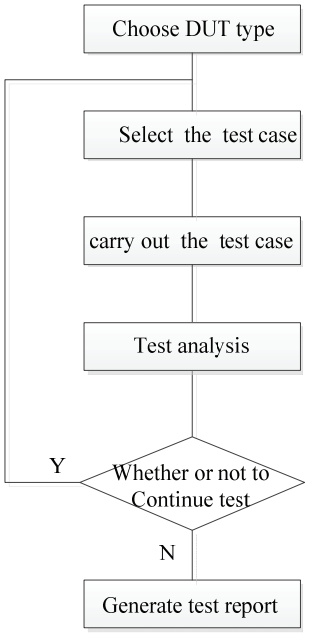

Figure 5 IEEE 1588 conformance testing process

IEEE 1588 conformance testing process is shown in Fig. 5. Select the suitable test case and carry out the test according to the DUT clock type. After completion of the conformance testing, generate the test report and judge whether the testing passed or not, provide the implementation details of the testing if the case testing has not passed.

4.2 Grandmaster Priority1 test

The hardware clock adoption in test bed can not only test ordinary conformance cases (realized by pc-clock), but also realize conformance cases combined with performance testing while grandmaster Priority1 testing is a typical case in data set comparison algorithm. Data set represents clock information. Data set comparison algorithm selects the best clock by comparing the two data sets. This test verifies whether DUT based on Priority1 can carry out correct processing. Data range of Priority1 is 0÷255 and priority prefers is small value.

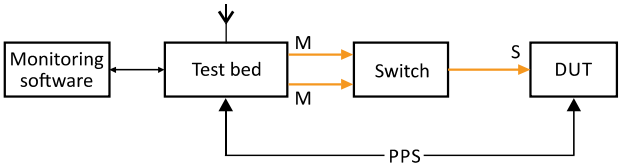

Figure 6 Structure of grandmaster Priority1 test

Test construction is shown in Fig. 6. DUT is connected to two master clocks inside the test bed by switchboard. GrandMaster Identity of the announce messages of hardware clock A and hardware clock B set as 0x 00 00 00 FF FE 00 00 00 and 0x 11 11 11 FF FE 11 11 11. Besides grandmaster Priority1, other fields are the same. Set clock A and clock B as two-step clock, and follow_up message correction field of hardware A is 0000040000000000, correction field of hardware B is 0000020000000000. Therefore, slave clock distinguishes grandmaster Priority1 in synchronizing process and hereby to synchronize with higher priority master clock.

The precision testing of tested slave clock can be realized by PPS. When slave clock is synchronized with clock A, the precision error is about 67,1 ms. When it is synchronized with clock B, the precision error is about 33,6 ms. The Priority1 logical processing can be judged by modifying the priority of hardware clock and observes the respective clock jitter.

4.3 Invalid follow_up message test

In synchronizing process, whether the follow_up message is from current master and whether the sequence number ID of follow_up message corresponds to Sync message will be firstly confirmed when the follow_up message is received by the slave clock. If fit, it will be default as correct follow_up message. Otherwise, it will be abandoned. In paper [10], the invalid follow_up message test was carried out. Nevertheless, it is difficult to insert a suitable invalid follow_up message testing for PC-clock because of the independent test bed and master clock. Moreover, present test method can only get the

logical processing procedure but whether the slave clock performance is influenced is unknown.

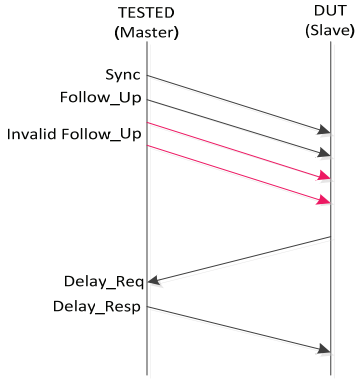

Figure 7 Invalid Follow_Up message test

The test bed has embedded master clock in the test bed. It is convenient to deploy invalid Follow_up message. Test bed sets clock Priority1 as master clock, inserts PPS to test bed and records DUT clock accuracy error as normal Offset. To normal follow_up message, the followUpModification is set as 225 (about 33,6 ms), i.e., 0x 0000 0200 0000 0000. Then the slave clock time error is 33,6 ms.

As shown in Fig. 7, the invalid Follow_Up message is inserted in two frames at least. The FollowUp Modification value was set to be 0. First frame of invalid message is source PortIdentity fault and second is sequence Id fault. On this basis, it is necessary to observe whether there is a vibrate in DUT time offset and the message field processing is correct to carry out invalid Follow_up message test. Meanwhile, no accuracy error vibration indicates invalid Follow_Up message is abandoned.

5 Test bed design

Based on the test requirement, an IEEE1588 clock test bed which includes monitoring software and test bed was designed in this paper. The test bed clock is implemented by hardware. In this way, the shortcoming of software clock can be avoided [9], and the conforming testing and performance test can be supported. Nevertheless, the calculated time is not accurate.

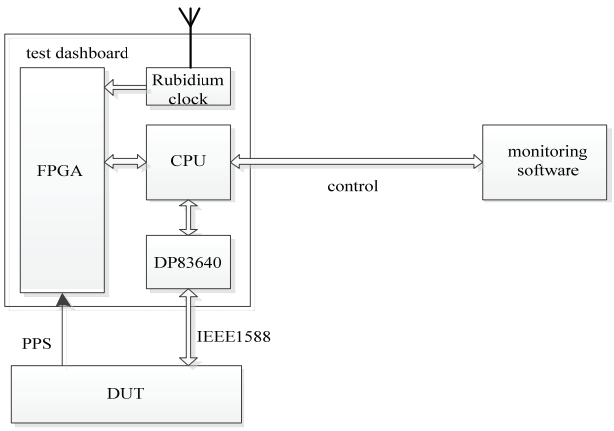

Figure 8 IEEE 1588 test structure

5.1 Hardware system structure

The clock synchronization system based on IEEE 1588 includes ordinary clock, transparent clock and master clock, which should be covered in the system test. Before the test, the test bed will be configured with the corresponding monitoring software before testing. After that, the test bed and DUT will interact via IEEE1588 message to realize synchronization and management. Meanwhile, the interactive message will be sent to the monitoring software for analysis as shown in Fig. 8

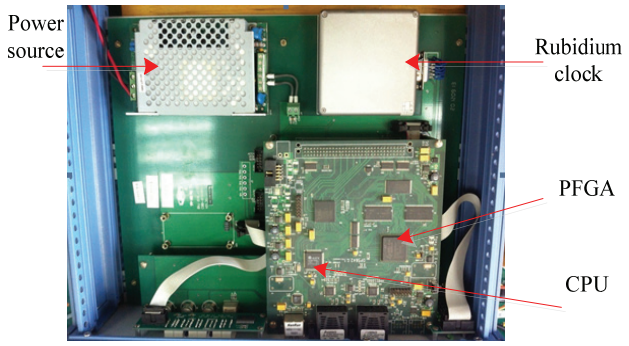

Figure 9 IEEE 1588 test structure

For a convenient test, the clock node should transmit PPS to test bed. DUT PPS is measured in FPGA with high precision rubidium clock and DP83640 [21-22], and time error of DUT clock can be got, the Circuit board is shown in Fig. 9. As a result, the IEEE1588 conformance testing and performance testing structure construct a closed loop system. The slave clock offset and message analysis can intuitively monitor the synchronization of DUT after excitation. It is therefore easy to find defects and estimate time performance of DUT.

5.2 Software architecture

IEEE1588 tester software consists of DSP control software and PC system control software. Software module and data flow is shown in Fig. 10.

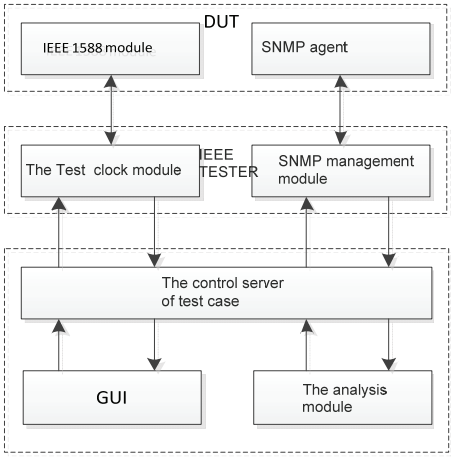

Figure 10 Software architecture diagram of IEEE1588 tester

1) GUI human machine interface module

GUI human machine interface module provides interactive graphical interface for IEEE1588 tester and test engineer. By graphical interface, test engineer selects start/stop test cases. During execution process of test case,

test engineer could monitor test case execution information with graphical interface.

2) The control server of test case

The control server of test case is automatic test control module, which is actually a scheduler. Test case control server is to analyse pre-edited XML file of test case, and then assign each test step of XML file to each module. For example, if the test step is to set the tester parameter and reset the test clock, then assign this step to the test clock module to carry out; If the test step is to set tested equipment parameters, then assign this step to the SNMP management module; If the test step is to set checkpoint, then assign this step to analysis and judgment module; If the test step is to set time delay, then it will be executed by control server itself.

3) Test clock module

Test clock module is a programming module dedicated to IEEE1588 protocol testing program, and itself is a IEEE1588 protocol implementation, but different from IEEE1588 ordinary intelligent device. The difference is to meet the test requirements, it can be configured to Master or Slave mode and it has more configurable parameters. After many parameters open, they can be controlled by test engineer and effectively broaden the test coverage. Test clock module is implemented on DSP of host tester and captures precise time by physical chip DP83640. Test clock module carries out setting tester parameters, reset test clock and other command assigned by test case serve. After setting tester parameters, test clock should be immediately reset to make the test clock operate according to new parameters. When tested equipment is as master clock, testing clock as the simulation slave clock interacts with tested device; when tested equipment is as slave clock, testing clock as the simulation master clock interacts with tested device. Test clock will send all interactive messages to PC system control software for analysis.

4) SNMP management module

In IEEE PC37.238, it regulates IEEE1588 management mechanism to adopt SNMP protocol. If tested equipment supports management mechanism, then management information base (MIB) defined by IEEE PC37.238 should be realized [9], that is tested equipment should be implemented to support SNMP agent of IEEE PC37.238 MIB. After SNMP management module received the command of setting tested equipment parameters sent by test case control server, it will finish the PTP parameters set of SNMP protocol support tested equipment with SET operation; SNMP management module can also capture real-time state information (such as deviation, path delay, port state machine status, etc.) of tested equipment by GET operation, and send to the PC control software system for analysis.

5) Analysis module

The function of Analysis module is to check whether the actual test result is consistent with the expected result. Analysis details are as the following: a) Analysis of all the IEEE1588 messages from interaction of clock module sent by tester host and the tested device; b) Analysis of real-time state information of tested equipment captured by GET operation of SNMP management control module; c) Analysis of timing deviation of tested equipment concluded from the comparison of second pulse output by tested equipment and standard GPS second pulse.

Based on the above mentioned, combining the conformance testing and performance testing, it is convenient to measure the clock ability and find factors which affect clock synchronization. Due to the network load impact on the synchronized ability, this test is carried out under low network load.

6 Experiment

6.1 Slave performance testing

We carry out performance testing and conformance testing with the test bed. For example, choosing a substation merging unit as slave, which is shown in Fig. 3, the TIE of the merging unit is achieved via the performance testing framework.

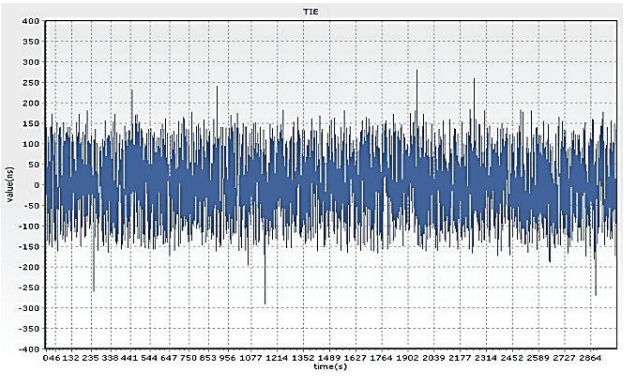

Figure 11 TIE

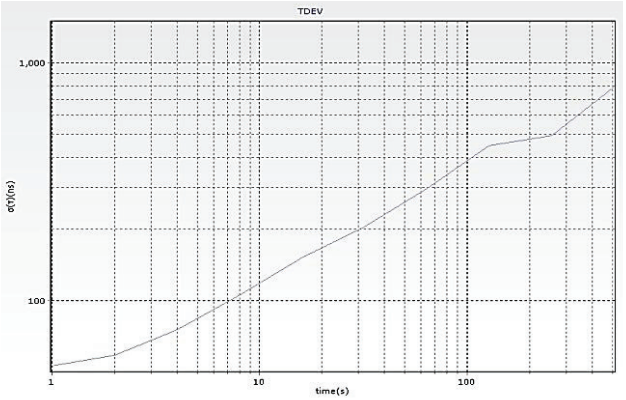

Figure 12 TDEV

Fig. 11 shows the TIE of the merging unit. The results indicate that the average offset correction is about 200 ns to across the 3000 seconds test with the worst case offset corrections as high as 200 ns. The character of the results is consistent with the result presented in paper [11]. The TIE could be attributed to the drift of merging unit oscillator used for holdover frequency reference between Sync cycles. During a single Sync cycle (1 second), the holdover drift error t illustrates that the DUT reference oscillator stability plays an important role in an IEEE 1588 precision time synchronization system. Figure 12 shows the TDEV computed from the TIE data. The results indicate the time stability of merging unit and demonstrate that merging unit clock Stability is guaranteed by IEEE1588.

6.2 GrandMasterPriority1 testing

It can be clearly seen from the Grandclock Priority 1 test in Fig. 13 that the slave accuracy is 33,6 ms. When the main clock grandMasterPriority1 is in case changes, the precision error is about 67,1 ms after vibrating. This phenomenon shows that slave discriminate against grandMasterPriority1and synchronize with the high priority master clock during the synchronization process. Therefore, when observing the corresponding clock offset, we can determine whether the priority logic processing is correct.

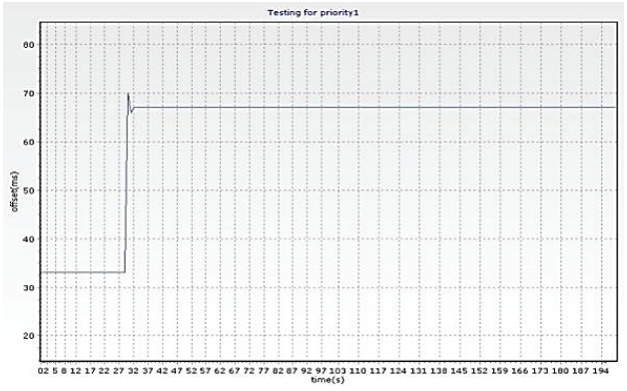

Figure13 Grandclock Priority 1 test

6.3 Invalid Follow_up message testing

The followUpModification value of normal Follow_up message is set as 225 (approximately 33,6 ms) in invalid Follow_up message testing. However, the two invalid Follow_Up frame messages are set to be 0. The first frame source PortIdentity is error, and so is the second frame sequence_Id. However, DUT Precision is maintained at 33,6 ms without vibrating, as can be observed from Fig. 14. Meanwhile, combined with messages analysis, invalid Follow_up message processing logic is correct. There is no effect on slave accuracy.

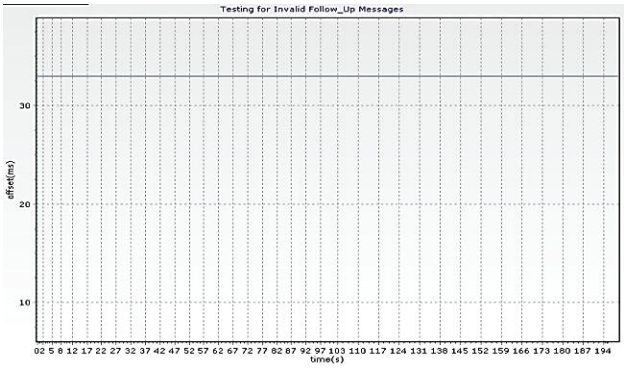

Figure 14 Invalid Follow_up message testing

7 Conclusions

IEEE1588 is considered to be prospective in various applications. Thus, it is significant to test clock synchronization system based on IEEE1588. This paper proposes a conformance and performance testing method with the characteristics and realization principle of IEEE1588, and develops the test bed to verify this testing method.

There are several clock types in IEEE1588 clock system. The testing of different factors which affect clock synchronization system precision should be taken into consideration. In IEEE1588 protocol, conformance testing cases are extensive. This paper takes two cases to design and then to explain the implementation process of conformance testing. The feasibility of conformance testing method, the interoperability and conformance of IEEE1588 node are verified by the designed test platform.

This paper presents the principle and index of IEEE1588 during the performance testing. According to different clock types, this paper adopts corresponding test framework to test and calculate time error and time deviation.

The conformance testing and performance testing method proposed by this paper are effective supplement of present IEEE1588 test. The combination of conformance testing and performance testing can well evaluate system ability and completely test synchronizing system node clock, and it is significant to the promotion of IEEE1588 in substation network.

7 References

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