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SMALL SIGNAL MODELLING AND IMPLEMENTATION OF PUSH-PULL BASED INVERTER WITH PARASITICS

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Original scientific research

The proposed PWM switch modelling technique is a simple method for modelling push-pull based single phase inverters operating in continuous conduction mode. In the design process of converters it is desirable to assess as many critical design parameters and parasitic effects by simulation as possible, since the control is hard to tune after fabrication. The main advantage of this method is its versatility and simple implementation. Furthermore, the introduced model also includes parasitic elements of the components to better estimate the converter behaviour. The resulting circuit is a time averaged model where all currents and voltages correspond to their averaged values. The validity of this model is verified by the given experimental results for a specified design example. This modelling technique helps to design the inverter effectively and better choosing the controller component values to achieve a good dynamic response. Finally, current mode controlled push-pull converter is simulated and compared with proposed modelling technique where a good accordance between them is revealed. Simulation analysis is done by Matlab 9 and Psim 6 software. The overall modelling estimation error was lower than 5 %.

Keywords: *average modelling; current mode control; frequency response; parasitic components; push-pull based inverter*

Modeliranje slabog signala i implementacija pretvarača zasnovanog na push-pull osnovi s parazitskim elementima

Izvorni znanstveni članak

Predložena tehnika modeliranja PWM sklopke jednostavna je metoda za modeliranje jednofaznih push-pull pretvarača koji rade u kontinuiranom modu vodljivosti. U procesu projektiranja pretvarača poželjno je simulacijom procijeniti što veći broj kritičnih parametara dizajna i parazitskih efekata, jer je regulaciju teško podesiti nakon izrade. Glavna prednost ove metode je njezina svestranost i jednostavna implementacija. Nadalje, predloženi model također uključuje i parazitske elemente komponenti kako bi se bolje procijenilo ponašanje pretvarača. Rezultirajući strujni krug je model u kojem sve vrste struje i naponi odgovaraju njihovim prosječnim vrijednostima. Valjanost ovog modela provjerena je dobivenim eksperimentalnim rezultatima primjerka određenog dizajna. Ova tehnika modeliranja pomaže učinkovitom dizajniranju pretvarača i boljem odabiru vrijednosti kontrolnih komponenti za postizanje dobrog dinamičkog odziva. Konačno, simulira se funkcioniranje push-pull pretvarača i uspoređuje s predloženim načinom modeliranja te se pokazuje dobra podudarnost između njih. Analiza simulacije obavljena je pomoću softvera Matlab 9 i Psim 6. Ukupna pogreška u procjeni modeliranja bila je manja od 5 %.

Ključne riječi*: frekvencijski odziv; kontrola moda struje; parazitske komponente; pretvarač koji radi na push-pull (guraj-vuci) osnovi; prosječno modeliranje*

1 Introduction

During the past decades, power electronic research has focused on the development of new families of inverter topologies used in portable applications. Power stages of PWM converters are highly nonlinear systems because they contain at least one transistor and diode, which operate as switches [1, 2].

The converters normally require control circuits to regulate the dc output voltage against load and line variations. Main control aspects are frequency response, transient response, and stability. Linear control theory is well developed and may offer valuable tools for studying the dynamic performance of PWM converters. However, in order to apply this theory, nonlinear power stages of PWM converters should be averaged and linearized [3]. Circuit modelling helps the designer to control and manufacture the converter more effectively. Averaging is the most popular tool for modelling and simulation of switched circuits with a view to dc converters, both in the time and the frequency domains [4].

Since the average model enables a simple small signal analysis, they play an irreplaceable role in the analysis of ac frequency responses of converters [5, 6]. There are two main techniques for switching converters averaged modelling: state space averaging (SSA) and switch network averaging (SNA) methods [7].

The SSA method uses the state space description of dynamic systems to derive the small signal averaged equations and is based on analytical averaging of linear equivalent circuits for different states of a converter determined by the status of transistor and diode [8]. But the SSA method requires considerable matrix algebra manipulation and is sometimes tedious, especially when the converter circuit contains a large number of elements. Moreover, it provides little insight into the converter behaviour. This feature is incongruous especially for design engineers [9]. On the other hand, the circuit averaging method leads to linear circuit models which are relatively simple and provide good intuitive insight into converter behaviour. Then it can be used for deriving various transfer functions, step responses and is compatible with electronic circuit simulators. In addition, control loops for PWM converters can be designed by applying well known linear control techniques [10, 11].

This paper introduces a way to simplification and modelling of a two stage single phase inverter structure by averaging the switch network. In spite of other works that consider the switch network ideal, this work adds the parasitic elements of the switch network into modelling process. The dependent sources are used to model the ideal switching network and the law of energy conservation is used here to model the transistor internal resistance, diode forward resistance and its offset voltage. By replacing the switching network in a PWM converter by its small signal circuit, the entire power stage model is obtained. Finally the model is used to derive and simulate the small signal ac transfer functions of control-to-output (h_{V_o-d}), audio-success-ability ($h_{V_o-V_i}$) and step

responses of the converter. $h_{V_o-V_i}$ means the transfer function of the output to input voltage of the studied circuit. Finally, a current mode controlled push-pull converter is simulated and then is compared with proposed modelling technique, where the results were in accordance with each other exactly. Experimental results for a 100 W inverter reveal the validity and precision of the proposed method.

2 Studied inverter structure

The inverter overall structure is shown in Fig. 1. This inverter has two stages. F_{S1} and D_1 are the switching frequency and duty cycle of block1, F_{S2} and D_2 are for block2 respectively. First block uses an isolated push-pull converter to convert the input voltage V_I (12 V_{DC}) to middle output voltage V'_o (312 V_{DC}) and the second block composed of a full-bridge converter, inverts the middle voltage (V'_o) to alternative rectangular output voltage across the load that is named by V_o (220 V_{rms}).

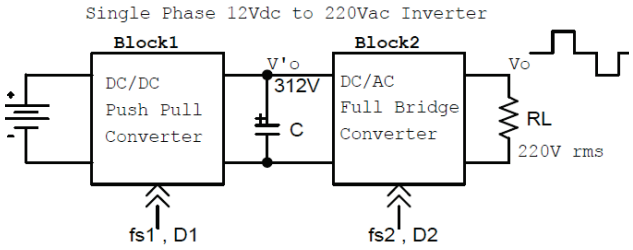

Figure 1 The proposed inverter overall structure

Fig. 2 shows the schematic of inverter blocks.

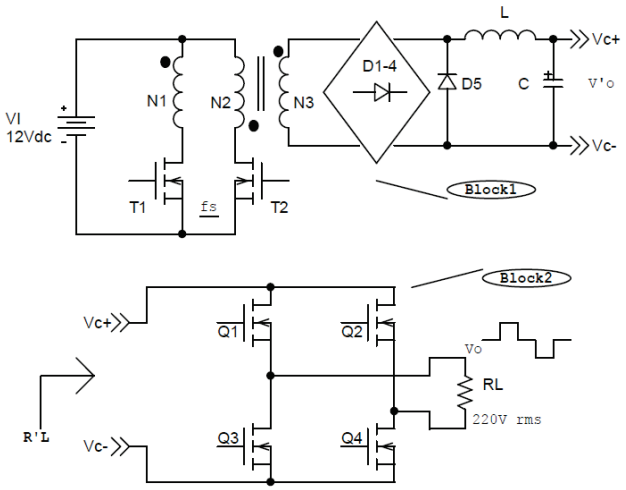

Figure 2 Schematic of proposed inverter

Output voltage waveform is depicted in Fig. 3.

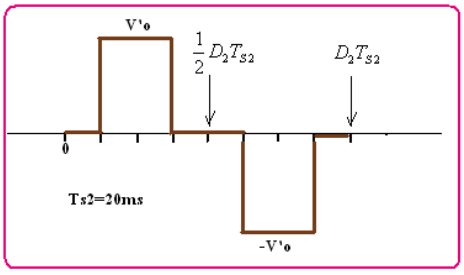

Figure 3 Output voltage waveform

Then effective value of V_o would be as in Eq. (1) [12].

$$V_{Orms} = \sqrt{\frac{1}{T_{S2}} \int_{T_{S2}} V_o^2(t)\,\mathrm{d}t} = \sqrt{D_2}.V'_o. \quad (1)$$

Eq. (2) shows If D_2=0,5 then V_o would be 220 V_{rms}.

$$V'_o = 312\ \mathrm{V},\ V_{o\mathrm{rms}} = 220\ \mathrm{V} \Rightarrow\ D_2 = 0{,}5. \quad (2)$$

By considering the power equality law, the resistance seen from block2 input could be presented by Eq. (3).

$$P_o = P'_o \Rightarrow \frac{V_o^2}{R_L} = \frac{V'^2_o}{R'_L} \Rightarrow R'_L = \frac{R_L}{D_2} = 2R_L. \quad (3)$$

Two primary winding turns of the push-pull transformer are the same and have opposite direction. Then by little circuit manipulation one can make the converter simpler as illustrated in Fig. 4.

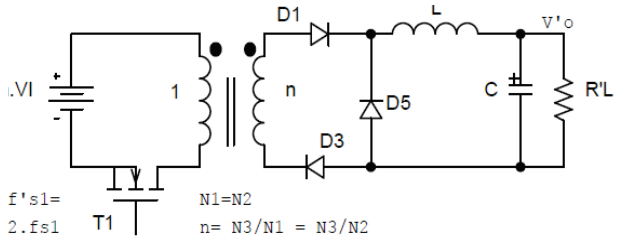

Figure 4 Simplified circuit of block1 converter

In this case switching frequency of transistor is double of the previous value ($f'_S = f_S$). Then by moving the transformer to the left side of T_1, Fig. 4 reduces to Fig. 5.

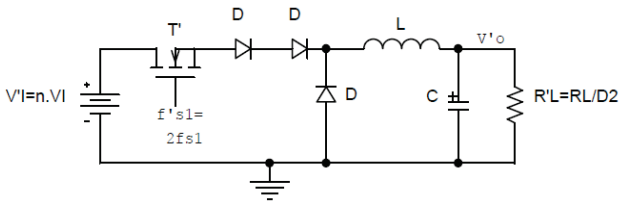

Figure 5 Simplification of Fig. 4 by transformer elimination

3 Averaged switch network modelling

Averaged switch method against the state space one is performable only on the switch network. Fig. 6 shows the single ended two switch network of the studied converter. Typical gate-source capacitance of the Mosfet transistor is about several ten pico farades then is ignorable. Specially since the derived model is valid up to half of the switching frequency this ignored capacitor cannot insert any considerable error to the final model.

Fig. 7 depicts the simplified dc model of the actual network with the averaged resistances moved to the inductor branch. Phrase V_F is the diode forward voltage, r_F is the diode on resistance, r_{DS} is the Mosfet resistance, D is the duty cycle of switching signal. S', D' and L' denote the switch, diode and inductor nodes of actual network respectively. The reflection rules can be applied

to move the parasitic components from one branch to another with considering the energy conservation law. Total resultant resistance is symbolized by phrase *r*.

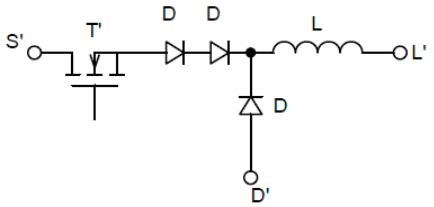

Figure 6 Switching network circuit

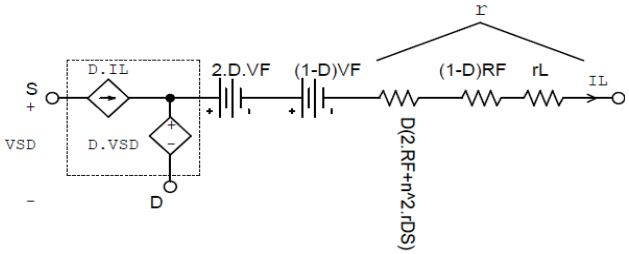

Figure 7 Simplified network with parasitic parts

Only dc and the low frequency components are of interest when studying control aspects of PWM converters. This is because the control signals of the closed loop PWM converters consist of dc and low frequency components. Consequently, low frequency components could be used to characterize the dynamics of PWM systems [13]. The large signal model of this network is visible in Fig. 8.

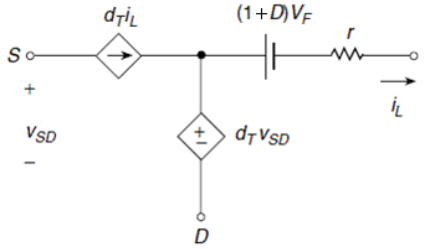

Figure 8 Large signal model of switch network

Where *r* could be stated by Eq. (4).

$$r = D \cdot n^2 r_{\mathrm{DS}} + (1+D)R_{\mathrm{F}} + r_{\mathrm{L}}. \tag{4}$$

Linearization of the large signal averaged model at a given operating point can be performed by expanding the equations to Taylor's series and neglecting the higher order terms that are expressed by Eq. (5) and Eq. (6). By supposing the small signal criterion, neglecting the minor terms will insert only 1 % error into the modelling process. (For example it is supposed that i_l is about 0,01 of I_L.)

$$d_T \cdot i_L = (D+d)(I_L + i_l) = DI_L + Di_l + \mathrm{d}I_L + \cancel{di_l}^{\,0}, \tag{5}$$

$$d_T \cdot v_{SD} = (D+d)(V_{SD} + v_{sd}) = DV_{SD} + Dv_{sd} + \mathrm{d}V_{SD} + \cancel{\mathrm{d}v_{sd}}^{\,0}. \tag{6}$$

Fig. 9 contains both dc and small signal dependent sources. According to Shannon's sampling theorem the yielded dynamic model is valid up to $f_S/2$ [14].

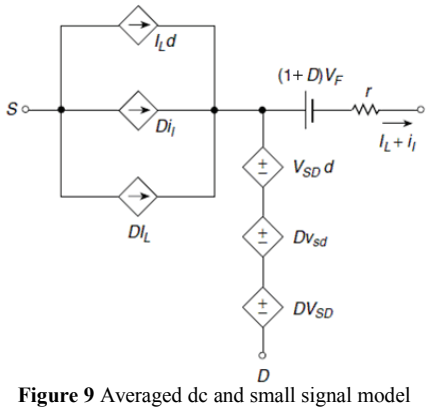

Figure 9 Averaged dc and small signal model

4 Replacing the model in the converter body

By replacing the switch model in converter body, one can derive the dc and small signal transfer functions of audio-success-ability and control-to-output as illustrated in Fig. 9. To study the dynamic behaviour of the inverter, output voltage response to step change in input voltage and duty cycle are also given. DC model can be derived by setting to zero the ac sources.

Now, small signal model can be derived by setting to zero the dc source in Fig. 9 as is depicted in Fig. 10. Small signal audio-success-ability transfer function could be deduced by eliminating the $d \cdot V'_I$ in Fig. 10 which is stated in Eq. (8) and Eq. (9).

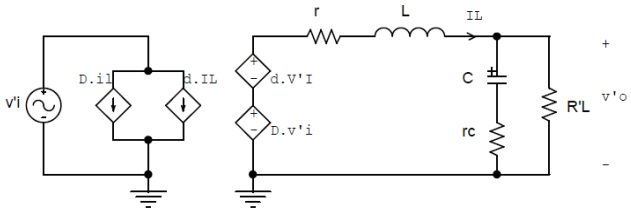

Figure 10 Small signal model of the converter

Considering Eq. (7),

$$Z_1 = r + SL \quad , \quad Z_2 = R'_L \,\|\, (r_C + \frac{1}{SC}), \tag{7}$$

$$v'_o = D \cdot v'_i \frac{Z_2}{Z_1 + Z_2}, \tag{8}$$

$$h_{v_o - v_i}(s) = K_1 \frac{1 + \dfrac{s}{\omega_z}}{1 + \dfrac{s}{Q\omega_o} + \left(\dfrac{s}{\omega_o}\right)^2}. \tag{9}$$

K_1, Q − factor and natural frequency are stated in the following equations:

$$K_1 = D\frac{R'_L}{R'_L + r}, \ \omega_z = \frac{1}{r_C \cdot C}, \tag{10}$$

$$Q = \frac{\sqrt{LC(R'_L + r)(R'_L + r_C)}}{L + CR'_L(r + r_C)}, \tag{11}$$

$$\omega_o = \sqrt{\frac{R'_L + r}{LC(R'_L + r_C)}} = \frac{1}{\sqrt{\tau_C \cdot \tau_L}}. \tag{12}$$

Eq. (13) expresses the time constants of C and L.

$$\tau_C = C(R'_L + r_C), \quad \tau_L = \frac{L}{R'_L + r}. \tag{13}$$

Similarly, it is easy to determine the small signal control-to-output (duty cycle-to-output) voltage transfer function by setting to zero the $D \cdot v'_i$ source in Fig. 10 as stated in Eq. (14) and Eq. (15).

$$v'_o = D \cdot v'_i \frac{Z_2}{Z_1 + Z_2}, \tag{14}$$

$$h_{v_o - d}(s) = K_2 \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \left(\frac{s}{\omega_o}\right)^2}, \tag{15}$$

where K_2 is:

$$K_2 = V'_I \frac{R'_L}{R'_L + r}. \tag{16}$$

Fortunately, control-to-output transfer function has no right half plane zero that is seen in boost and buck-boost types [15]. Damping ratio can be determined using $\xi = 1/(2Q)$. The delay t_d introduced by a power transistors driver and pulse width modulator on the duty cycle can be described by Eq. (17).

$$h_{\text{delay}}(s) = \mathrm{e}^{-st_d} \approx \frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}}. \tag{17}$$

Hence, the delayed control-to-output function is:

$$h_{v_o - d}(s) = K_2 \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + (\frac{s}{\omega_o})^2} \times \frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}} \tag{18}$$

5 Experimental results

Experimental test setup is indicated in Fig. 11. Circuit main components value is tabulated in Tab. 1. Also, by considering (11) and (21), Bode plot of small signal transfer functions of audio-success-ability and control-to-output are depicted in Figs 12 and 13. An external resistor is added to capacitor ESR, first to protect the diode bridge from starting surge current and second to increase the transfer function zero frequency. Small signal model results are valid up to half of switching frequency. For this case, f'_{s1} is equal to $2f_{s1}$, thus Fig. 12 and Fig. 13 data are reliable at frequencies between 0 kHz to 50 kHz. Phase margin of audio-success-ability is +95° and for control-to-output case is 180° approximately.

Since the delay time produced by switching transistor is very low (for example it is about several micro seconds), therefore its influence will appear only in frequency ranges above the switching frequency, so it is negligible.

Audio-success-ability function decreases from 0 dB then its gain margin has negative value, also its phase curve never reaches −180°, thus there is not any concern for unstability condition that may be caused by source voltage disturbance. Control-to-output function bode plot is depicted in Fig. 13, its phase margin is about +90° that makes a good stable boundary against the duty cycle changes. Typical value of duty cycle is 0,2 to 0,8.

Table1 Circuit components value

Symbol	Description	Value
V_F	Diode threshold voltage	0,6 V
R_F	Diode forward	0,075 Ω
r_{DS}	MOSFET on-resistance	0,02 Ω
L	Inductor value	40 µH
r_L	ESR* of inductor	0,08 Ω
C	Middle capacitor value	68 µF
r_C	ESR* of capacitor	0,33 Ω**
N	Switching transformer turn ratio	40
f_{S1}	Push-Pull switching frequency	50 kHz
D_1	Push-Pull duty cycle	0,7
t_d	Estimated delay time	5 µs
f_{S2}	Full-Bridge block frequency	50 Hz
D_2	Full-Bridge block duty cycle	0,5
R_L	Load resistance	450 Ω

* Equivalent Series Resistance, ** externally added resistor is 0,22 Ω

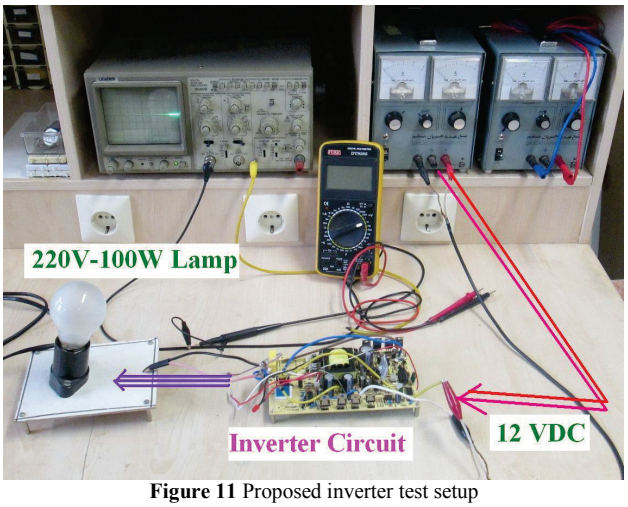

Figure 11 Proposed inverter test setup

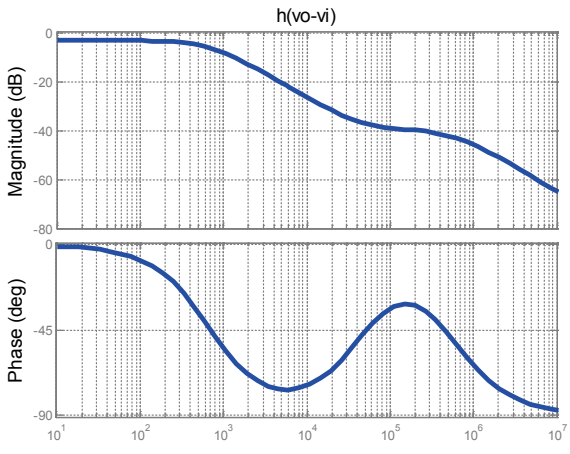

Figure 12 Small signal transfer function of audio-success-ability

According to Tab. 1, converter components value is selected so that its dynamic response stays in the over damped regime (ξ>1). Since any over shoot of V'_o may exceed from transistor and diode breakdown voltage and damages them. Fig. 14 shows the Mosfet gate signals of T_1 and T_2. This figure and consequent ones are traced using analogy Leader type oscilloscope. Inverter output voltage is depicted in Fig. 15. The transient component of the output voltage of inverter is given by Eq. (19), where ΔV_I is the step change of input voltage.

$$v_o(s) = \frac{\Delta V_I}{s} \times h_{v_o - v_i}(s) \Rightarrow v_o(t) = \zeta^{-1}[v_o(s)]. \quad (19)$$

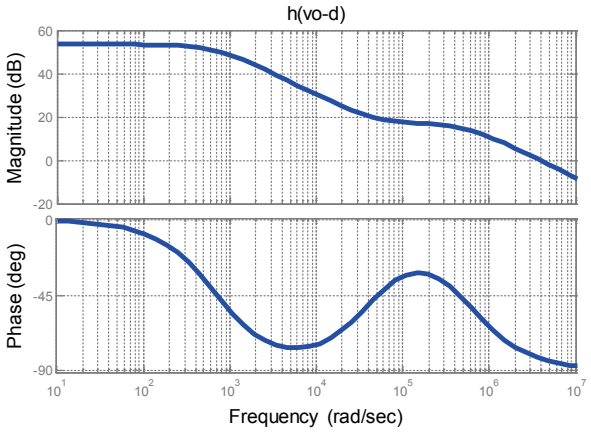

Figure 13 Small signal transfer function of control-to-output

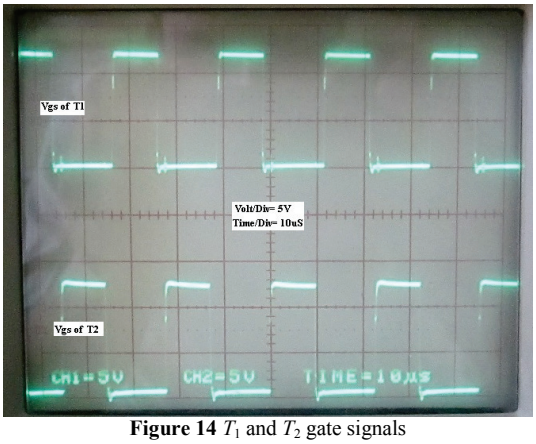

Figure 14 T_1 and T_2 gate signals

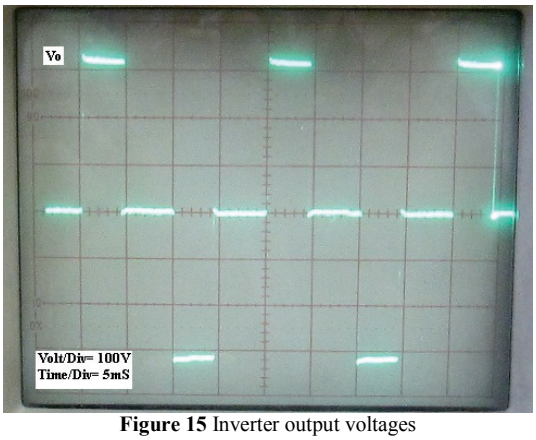

Figure 15 Inverter output voltages

Figs. 16 and 17 show the transient response of output voltage V'_o to a step change of input voltage (12 → 12,7 V). This corresponds to a step change in small signal V_i from 0 to 0,7 V for the experimental and modelling cases.

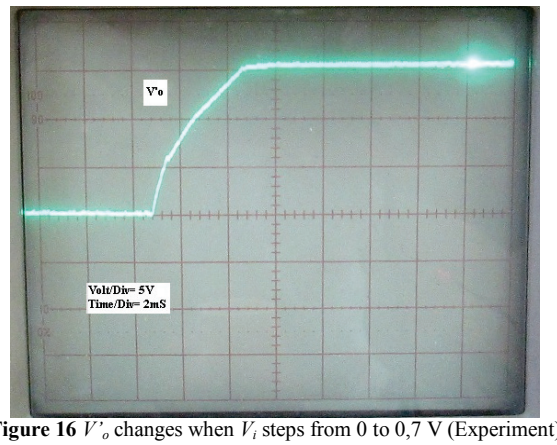

Figure 16 V'_o changes when V_i steps from 0 to 0,7 V (Experiment)

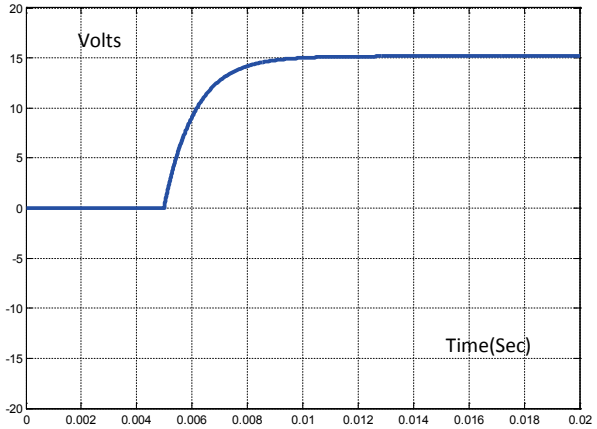

Figure 17 V'_o changes when V_i steps from 0 to 0,7 V (Modelling)

Similarly to Eq. (19) one can deduce the transient response of the converter output voltage to step change of the duty cycle which is expressed by Eq. (20).

$$v_o(s) = \Delta d(s) \times h_{v_o - d}(s) \Rightarrow v_o(t) = \zeta^{-1}[v_o(s)] \quad (20)$$

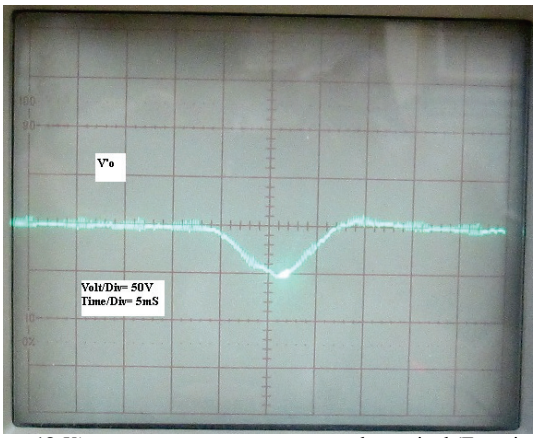

Figure 18 V'_o responses to a temporary step change in d (Experiment)

To have variation, in this case, duty cycle changes from 0,7 to 0,6 and endures 7 ms in this state, then returns to prior value which is stated by Eq. (21), Eq. (22) and depicted in Figs. 18 and 19.

$$d(t) = D + k\left[u(t) - u(t - t_0)\right], \quad (21)$$

where $k = -0{,}1$, $t_0 = 7$ ms.

$$\Delta d(s) = \frac{k}{s}\left(1 - e^{-st_0}\right). \tag{22}$$

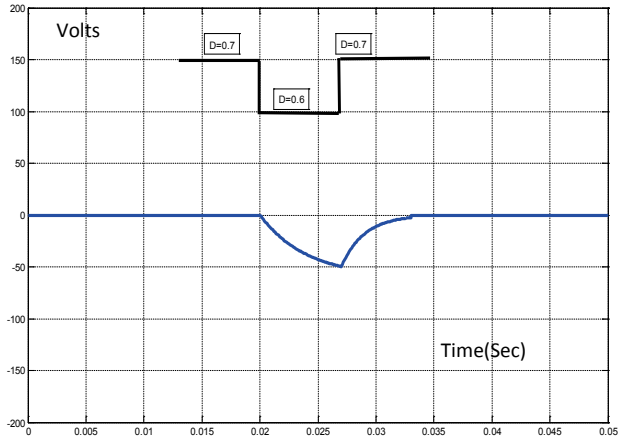

Figure 19 V'_o response to a temporary step change in d (Modelling)

6 Current mode control modelling

Current mode push-pull converter is studied here to better reveal the proposed model benefits. This control method contains two loops: an inner current loop and an outer voltage loop. The technique is called current mode control because the inductor current is directly controlled, whereas the output voltage is controlled only indirectly by the current loop. The key feature of this method is that the inner loop changes the inductor into a voltage dependent current source at frequencies lower than the crossover frequency of current loop. Converter overall schematic is depicted in Fig. 20.

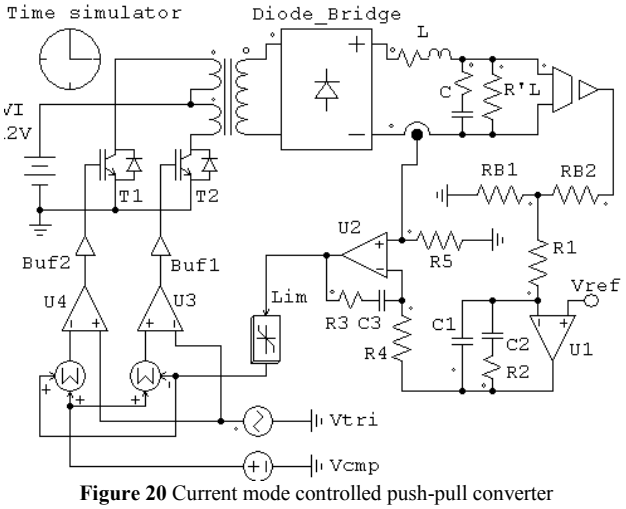

Figure 20 Current mode controlled push-pull converter

Table 2 Components value of converter control stage

Symbol	Value	Symbol	Value
R_{B1}	1 kΩ	C_1	220 pF
R_{B2}	99 kΩ	C_2	4,7 nF
R_1	1 kΩ	C_3	0,1 nF
R_2	100 kΩ	V_{ref}	3,1 V
R_3	2,2 kΩ	V_{cmp}	1 V_{DC}
R_4	100 kΩ	V_{tri}	5 V, 50 kV
R_5	100 kΩ	Limiter	0 ÷ 2,5 V

The duty cycle is determined by the time instants at which the inductor current reaches a threshold signal built by voltage compensator. Components of converter power stage are the same as in Tab. 1 and the components of control sub-circuit are stated in Tab. 2.

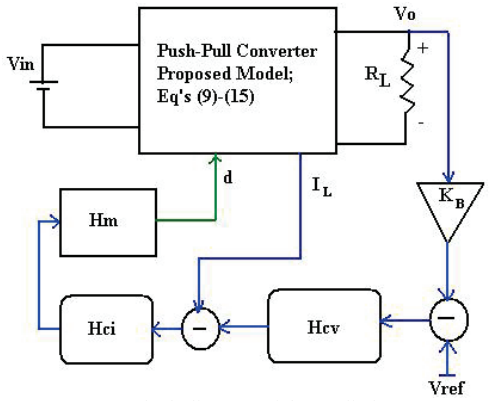

Figure 21 Block diagram of the studied converter

Fig. 21 shows the block diagram of this converter.

The action of the current loop is similar to that of a sample and holds circuit which is a nonlinear time varying system. H_{cv}, H_{ci} and H_m are the transfer functions of voltage compensator, current compensator and modulator stage as stated by Eqs. (23) ÷ (25). Also K_B represents the resistive dividing ratio of R_{B1} and R_{B2}.

$$K_B = \frac{R_{B1}}{R_{B1} + R_{B2}}, \tag{23}$$

$$H_{cv}(s) = -\frac{1}{C_1(R_1 + R_{B1} \,||\, R_{B2})} \cdot \frac{s + \dfrac{1}{R_2 C_2}}{s\left(s + \dfrac{C_1 + C_2}{R_2 C_1 C_2}\right)}, \tag{24}$$

$$H_{ci}(s) = \frac{-\left(R_3 + \dfrac{1}{sC_3}\right)}{R_4}, \tag{25}$$

$$H_m(s) = \frac{\pi^2 f_s^2}{V_{m,\text{tri}} \times s\left(s + \dfrac{\pi^2 f_s}{2}\right)}. \tag{26}$$

Fig. 22 shows the bode plot of current loop transfer function denoted by T_i. Its phase margin is about 70° and therefore guarantees a good stability condition. Current loop function is expressed in Eq. (27).

$$T_i(s) = K_B \times H_{cv}(s) \times H_{ci}(s) \times H_m(s) \times h_{v_o - d}(s). \tag{27}$$

Fig. 23 shows the converter output voltage at the start-up instant. Simulation and modelling results are denoted by "sim" and "mdl" tags respectively.

Fig. 24 shows the converter output voltage in the output load disturbance condition. Here, the output load increases from 300 W to 450 W at t = 20 ms. As you see, it proves a good voltage stabilization capability of the designed control circuit.

Fig. 25 exhibits the condition where the reference voltage changes and enforces the output voltage to step-up from 310 V to 340 V. As you see, the modelling result is in accordance with the simulation result.

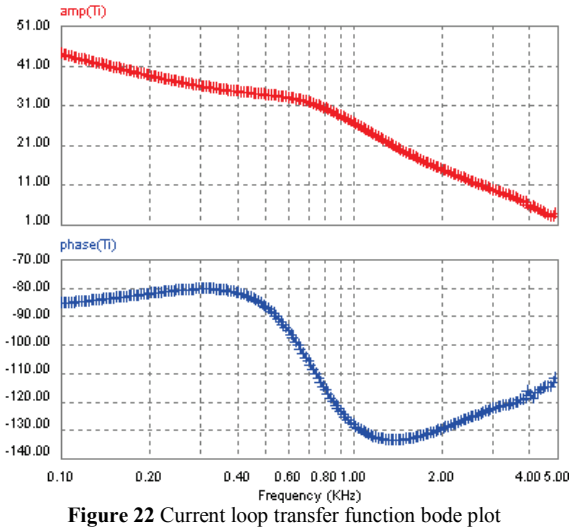

Figure 22 Current loop transfer function bode plot

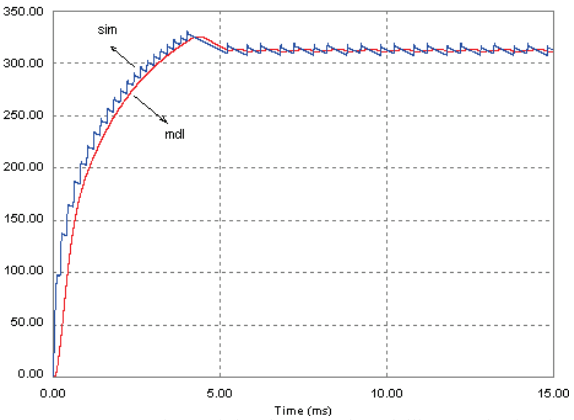

Figure 23 Comparison of simulation and modelling results for the converter output voltage

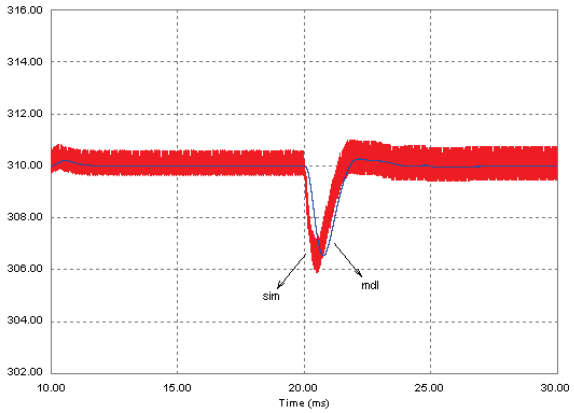

Figure 24 Output voltage when the load changes from 300 W to 450 W

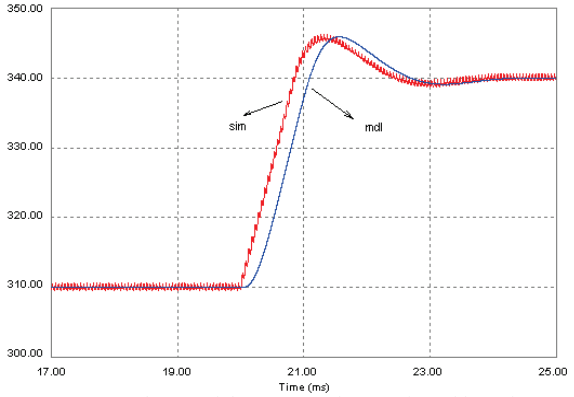

Figure 24 Step change of the output voltage enforced by reference signal

7 Conclusion

In this paper, a schema of a two stage single phase inverter is presented and a methodology to get the dc and ac small signal transfer functions of audio-success-ability and control-to-output is proposed with parasitic elements consideration. This method is based on the averaged switch network model, then this method advantages in comparison with usual state-space averaging method is discussed. Parasitic elements consideration helps the designer to better estimate the quiescent point and dynamic response of the converter. Besides, a current mode controller is designed and simulated. Results demonstrate certain conformity of this model. Finally, experimental results for the given 12 V_{dc} to 220 V_{ac} inverter prove the validity and accuracy of this technique. The total modelling estimation error is lower than 5 %.

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