Computer Aided Design of a Layout of Planar Circuits by Means of Evolutionary Algorithms

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In this paper we focus on a real-life application of Evolutionary Algorithms (EA) to the design of Radio and Microwave Frequency (RF& M) circuits. The task is to find a shape of a circuit that meets certain electrical and technological requirements. Additionally, manufacturing cost should also influence the evaluation of the design. Several methods, those based on the circuit theory as well as on numerical optimization, work quite effectively for many typical applications. However, with complicated tasks improved hybrid algorithms are needed that combine better topology search (for shape finding) with continuous parameter optimization. In this contribution, we overview Evolutionary Algorithms that have been used for the task, and propose a new approach. These approaches differ in encoding method and genetic operators. We provide experimental verification of the proposed approach, and discuss several example designs yielded by the method.

Introduction

In this paper we focus on the Computer Aided Design (CAD) of a class of Radio Frequency and Microwave (RF& M) Circuits, called *Impedance Transformers* (IT) [1,2]. ITs constitute a class of so called two-port (with single input and single output) electronic circuits dedicated to match the *source device* to the *load*. In general, a source is assumed to be an AC voltage generator or any other power source; and as a load, any passive circuit can be considered (e.g. a transmitter antenna, a resistor, and a heating cavity). In many applications ITs not only act as a matching device but as a filter as well.

Most often, ITs are produced in a planar technology as a strip of metal surrounded by air or dielectric media. One or many metal plates shield the whole device. There are several different planar technologies that are used to implement ITs: *strip line, microstrip line, suspended strip line, slot line*, etc. (for more information see [1]). Example of a planar circuit, realized in microstrip technology is presented in Fig. 1. On a lamina plate, called *substrate*, the IT is manufactured as a certain patch of metallization.

The shape of the patch and its dimensions are determined by the electrical specifications of the device. Several analysis methods have been developed so far to evaluate frequency characteristics of planar circuits. The first class of methods, based on circuit theory (CT) [2], is used in almost all state-of-the-art CAD programs [3]. In CT the circuit is decomposed into distributed (transmission lines etc.) and lumped (resistors, inductors, capacitors etc.) elements from the components library. Then, overall characteristics are computed from elements and connections matrices. This simplified model is numerically very efficient and quite accurate. However, discontinuities in a carelessly designed, sharply shaped circuit may produce unwanted *fringing field effects* (FFE) [4], which are hard to analyze and compensate. More accurate circuit analysis requires the application of methods based on the field theory. Many engineers have been using Finite-Difference Time-Domain (FDTD) or Spectral Domain (SD) programs, like [5] for arbitrarily shaped circuit simulation. Although FDTD simulators have been recognized as a reliable and accurate tool for circuit analysis, they are very time and memory consuming. A single analysis usually takes

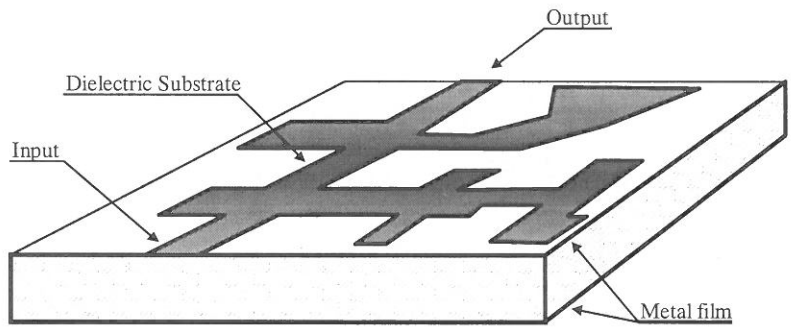

Fig. 1. Example of planar circuit manufactured in microstrip line technology.

from seconds (for circuits with axis or planar symmetry) to hours (for more complicated 3D structures) on Pentium 200 MHz.

Optimization programs are now indispensable tools in the CAD design of the RF& M circuits. Commercially available software uses various techniques [3], like gradient and non-gradient-based methods, simulated annealing, Monte-Carlo techniques, mini-max and Least-p-based optimization [6], combined with the CT analysis method. In these programs, parameters (physical dimensions like length or width of metallization rectangle) of predefined quantity are changed (scaled) within an optimization loop, in order to achieve desired circuit performance. The basic topology of the circuit remains unchanged during program execution. The CT method neglects some field effects, therefore measured circuit response for the implemented circuit may differ from that, calculated for the simplified CT model. In that case, the circuit is usually improved in an experimental way, either by scratching or by manufacturing many prototype units.

FDTD simulation allows to exactly (very close to the measurement results) analyze arbitrarily shaped conductor configuration. Up to now, only a few authors have used wave simulation within an optimization procedure. However, in most cases, the device shape had to be declared by the designer [7,8]. Only two papers present generalized approach to automated generation of RF& M device shape [9,10]. Both approaches use a combination of wave simulation SD [9] or FD-TD [10] with a genetic algorithm.

2. RF&M Circuit Design

2.1. Problem Formulation

The problem of matching the load to the source for the two-port network (see Fig. 2) can be described in the following way:

- power delivered to the load should be maximal,
- power loss and radiation of the matching network should be minimal.

Both the source and the load are characterized by their admittance values, $Y_g(f)$ and $Y_l(f)$, respectively, which are complex functions of the frequency f. The matching network transforms load admittance into $Y(f)$ (formulas for evaluation of the input admittance are given in section 2.3). In the ideal case, when there is no power reflection, it holds [2]:

$$Y(f) = Y_g^*(f) \tag{2.1}$$

where Y^* denotes conjugate to Y.

In the realistic case, condition (2.1) cannot be guaranteed; and in order to design an optimal circuit, the following mini-max problem should be solved:

minimize (by changing(scaling) circuit shape)

$$\{\textbf{maximum of } |\Gamma(f)| \text{ in the given frequency band}\} \tag{2.2}$$

where $|\Gamma(f)|$ denotes *input reflection coefficient* which is given by the following formula [2]:

$$\Gamma(f) = \frac{Y_g^*(f) - Y(f)}{Y(f) + Y_g^*(f)} \tag{2.3}$$

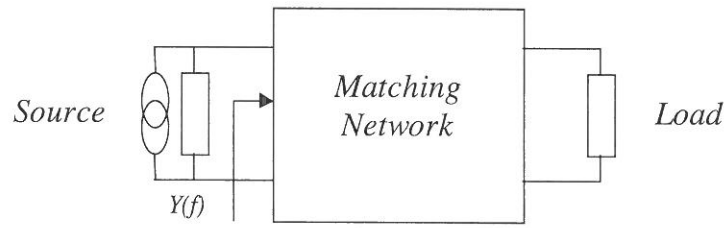

Fig. 2. General representation of two-port network.

Input reflection coefficient is a measure of mismatch. It equals the square root of the ratio of power lost inside the source to the power generated by the source. When condition (2.1) is satisfied $|\Gamma(f)| = 0$. *Input reflection coefficient* can be also expressed in terms of the *scattering matrix* [2]:

$$\Gamma(f) = S_{11}(f) + \frac{\Gamma_l(f)^* S_{12}(f)^* S_{21}(f)}{1 - \Gamma_l(f)^* S_{22}(f)} \quad (2.4)$$

where $S_{11}(f)$, $S_{21}(f)$, $S_{22}(f)$ – elements of the *scattering matrix* [2] of the matching network, and $\Gamma_l(f)$ - *output reflection coefficient* given by:

$$\Gamma_l(f) = \frac{Y_g(f) - Y_l(f)}{Y_l(f) + Y_g(f)} \quad (2.5)$$

The admittance approach (formula 2.3) is frequently used with CT methods [6], while the scattering matrix approach (formula 2.4) is used with both CT algorithms and wave simulation [7,8,9,10]. The choice of the method depends on many conditions. Let us present the most important ones.

- Topology and model of the network:
  - admittance approach can be applied effectively only for circuits consisting of a cascade or tree-like connection of two-ports;
  - scattering matrix approach is a universal one - can be applied for arbitrarily shaped circuit.
- Type of the tool used for analysis:
  - some tools, like wave simulators, produce on the output the *scattering matrix* of the circuit.
- Efficiency of the method:
  - admittance approach is approximately 10 times faster than the scattering matrix approach.

2.2. Circuit Modeling

Several design methods have been developed so far which are based on the simplified (CT) model. These methods can be classified as follows, according to the way they represent and modify the IT design.

In the *Stepped Impedance Method* (SIM), the circuit is shaped as a cascade of interconnected sections of transmission lines (an example circuit is depicted in Fig. 3). Each section, shown as an ellipse, is implemented as a metallization rectangle. The design process consists in optimization of both width and length of each section; the number of the sections is kept constant [13,14,15].

SIM can be generalized to the class of circuits consisting of the main cascade, called stem, which connects input with output, and sections connected as side branches. Example of the tree-shape circuit is depicted in Fig. 4.

The *Continuous Function Method* (CFM) represents the transformer's shape as a continuous function from a certain class (e.g. polynomial) parameterized by a set of coefficients. In this case, the idea of the design process is to find optimal values of those coefficients. The transformer length is kept constant [11].

Another approach, *Discrete Function Method* (DFM), inherits ideas from the last two methods (SIM and CFM). Like the SIM, the circuit is a cascade, or a tree-connection of metallization rectangles (strips), however the length of each, as well as their number, are kept constant (as opposed to the SIM). Thus, the optimization consists of adjusting only the width of each strip. If the length of each rectangle is relatively small in comparison to the total transformer length, the DFM approach might be interpreted as a kind of CFM approach [6,11].

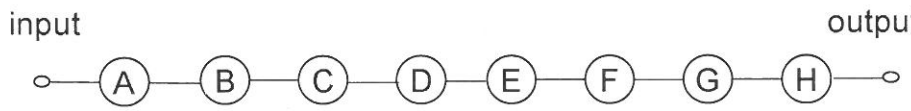

Fig. 3. Example of cascaded matching circuit.

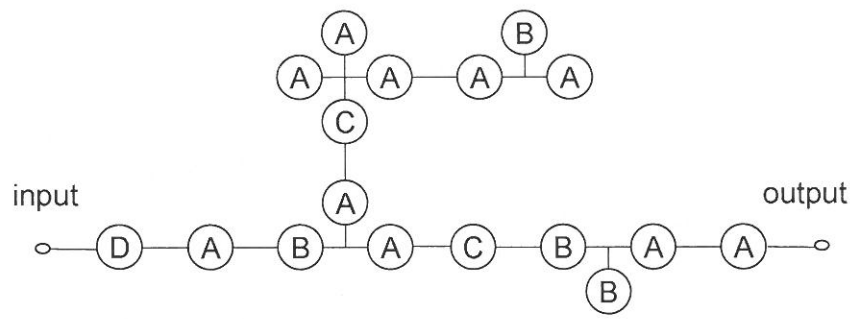

Fig. 4. Example of tree-shape matching circuit.

2.3. Existing Design Methods

While designing matching circuits, a compromise between electrical, technological, and economical objectives should be made.

Matching circuits are designed to match source and load whose admittances are given; the matching is required to be maintained within a given frequency band $[f_{\min}, f_{\max}]$. The design should reduce FFE such that e.g. maximal power reflection coefficient falls below certain admissible level. The design should be realizable, e.g. in the strip line technology, and the width of each strip should fall into the range $[W_{\min}, W_{\max}]$. Finally, the device should be miniaturized.

The design problem can be expressed as a constrained mini-max task (2.2). It can be solved either by using nonlinear programming methods with so called "Least-p norm" (Minkowski norm) [8] or by using a non-smooth optimization method [16]. We concentrate on a simple model of the circuit, which consists of a large number of cascaded or tree-connected sections of transmission lines. Each line section can be described by two parameters:

- characteristic admittance Y_{oj} (or alternatively by its width - w_j),
- line length (we assume it to be constant, equal to l for each section and relatively small).

In general, the aim of the design can be mathematically stated as follows:

$$\text{minimize} \quad \max_{f_i \in F} |\Gamma(Y_0, l, f_i)|, \quad i = 1..n_f \tag{2.6}$$

subject to the box constraints:

$$Y_{o\,\min j} \leq Y_{oj} \leq Y_{o\,\max j}, \quad j = 1..n_e$$

where: Γ : input reflection coefficient (see eq. 2.3, 2.4)

Y_o : characteristic admittance vector

l : line length

F : discrete set of frequencies f_i

n_e : number of circuit elements.

Since we assume equal length for each section, value of l is not subject to the optimization.

2.4. Evaluation of a Design

While designing a circuit, it is possible to estimate its real properties using several approaches. The most accurate, and most computationally intensive, is to use one of the existing FDTD electromagnetic simulators [5,8] that analyze planar circuits by solving the Maxwell equations on a grid. Unfortunately, this method is very time-consuming (for example, simulation may take from minutes to hours of Pentium 200 MHz CPU time, depending on the problem). An alternative approach is to utilize simplified CT models (Pentium 200 MHz CPU time may be reduced to milliseconds); unfortunately, models of such type neglect the FFE and their results are less reliable. This simplification preserves good accuracy of the model only if the influence of FFE is small, which holds in the case of smooth circuits. From the literature [4] it follows that smoothness of the circuit is highly positively correlated with its bandwidth. Thus, enforcing smoothness of the design may confer two benefits: an ability to employ simplified models and an increased possibility of finding a good (maybe globally optimal) design.

For cascaded designs, the input admittance $Y(f)$ is computed using a recurrent impedance transformation formula [1]. Calculations start from load - $Y^{n_e}f$ is set to the load admittance $Y_l(f)$. Then, the admittance is transformed through the cascade. For each jth section:

$$Y^{j-1}(f) = Y_{oj}\frac{Y^j(f) + Y_{oj}\tanh(\gamma l_j)}{Y_{oj} + Y^j(f)\tanh(\gamma l_j)} \qquad (2.7)$$

where γ is wave propagation constant (frequency dependent).

Finally, the input admittance equals $Y(f) = Y^0(f)$.

For tree like shapes, the formulas are slightly different. As before, end admittance of the stem equals load admittance. For cascaded connection of sections, we use formula (2.7), and for the parallel connection of sections j, k etc., it holds:

$$Y^{j-1}(f) = Y_{oj}\frac{Y^j(f) + Y_{oj}\tanh(\gamma l_j)}{Y_{oj} + Y^j(f)\tanh(\gamma l_j)} + Y_{ok}\frac{Y^k(f) + Y_{ok}\tanh(\gamma l_j)}{Y_{ok} + Y^k(f)\tanh(\gamma l_k)} + \ldots \qquad (2.8)$$

```
procedure evolutionary algorithm
begin
    initialize P0
    t:=0
    while not stop_criterion do
    begin
        Ot := reproduce Pt
        crossover Ot
        mutate Ot
        Pt+1 := select (Pt ∪ Ot)
    end
end
```

Fig. 5. Outline of an evolutionary algorithm.

In formulas 2.7, 2.8 we assign terminal admittance of tree branches, either to zero (for an open circuit) or to infinity (for a short circuit).

3. Evolutionary Algorithm Framework

Evolutionary algorithms described below combine the evolutionary-strategy-like $(\mu + \lambda)$ selection scheme [12] together with specific encoding of solutions and genetic operators. The operators (crossover and mutation) are meaningful in the problem domain and are analogous to the electronic circuits design methods. An outline of the evolutionary algorithm is provided in Fig. 5.

The algorithm maintains a population P_t containing μ designs. In each step of the algorithm, an offspring population O_t is created repeating λ times: selecting randomly (with uniform distribution) a design from P_t and duplicating it into O_t. After that, each consecutive pair from O_t undergoes crossover with probability p_c. Then, each design is mutated. There are three possible types of mutation: expansion, contraction and perturbation (described below). During each mutation step, the actual mutation type is chosen from the three above with equal probability. After altering the offspring population O_t, new base population P_{t+1} is created by selecting μ best designs from $P_t \cup O_t$. The whole process is iterated until the stop criterion is satisfied.

We tested two evolutionary algorithms using the same framework. The first method was aimed

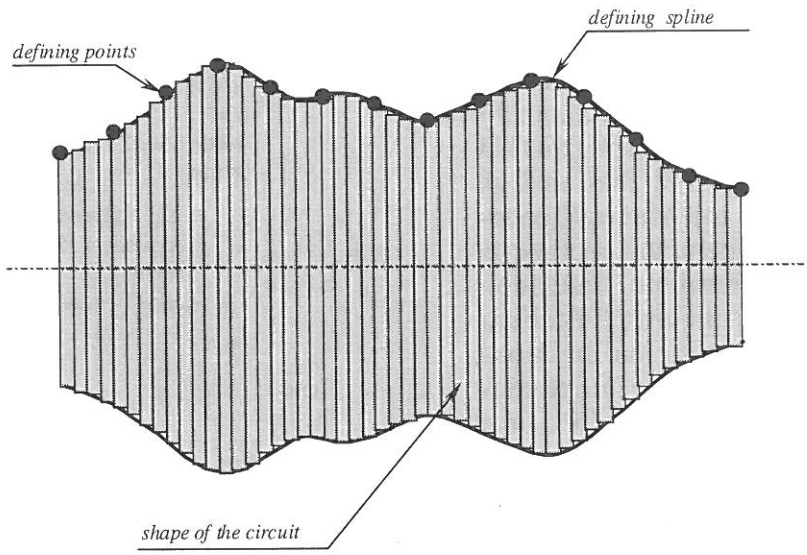

Fig. 6. Chromosome encoding.

at searching through the space of cascaded circuits. From the analysis of the results of experiments we found that for hard problems, the solution is often found on the boundary of the feasible region. Since cascaded circuits are special subclass of tree-shaped ones, we expected that there might exist better solutions, not represented as a cascade. Therefore, we hoped that adding more degrees of freedom might allow us to examine the non-cascaded solutions. We proposed an algorithm with the tree-based encoding and genetic operators, and performed series of experiments that confirmed our expectations.

4. Cascaded Circuits

4.1. Chromosome Structure and Evaluation

In general, we treat the matching circuit as a cascade of elements - transmission line sections, each implemented as a rectangular metallization strip having equal length and variable width. The algorithm manipulates both the number of sections (i.e. the length of the cascade) and width of each section in order to improve the design.

We assume that the metallization shape is symmetrical about the horizontal axis. Its border is defined by the cubic spline. The actual shape of the circuit is obtained by approximating the spline-defined shape by inscribing the cascade of rectangular strips of equal length.

A chromosome contains points to draw the spline through. Their x-coordinates are set along the horizontal axis with equal interval (which is 10 times sparser than the metallization strips of the circuit), and y-coordinates are subject to optimization and are memorized as genes in the chromosome. Each gene is a real number from the range $[W_{\min}..W_{\max}]$; $W_{\min}$ and $W_{\max}$ are the design parameters (and come from the technological restrictions).

The chromosome is evaluated using a multi-step procedure. First, the cubic spline is drawn through the points from the chromosome. After that, an actual shape of the circuit (cascade of stripes) is drawn (see Fig. 6). The cascade (more precisely, width of each strips) is then tuned by the non-smooth optimization algorithm (NOA) [16]. Evaluation of the design yielded by the NOA is returned to the evolutionary algorithm as evaluation of the chromosome.

4.2. Genetic Operators

To allow variable length of the circuit, we used the following specific genetic operators. There are two classes of mutation types (see Fig. 7):

- first one affecting length of the design, namely expansion or contraction of the cascade,
- second one changing the design's elements (perturbation).

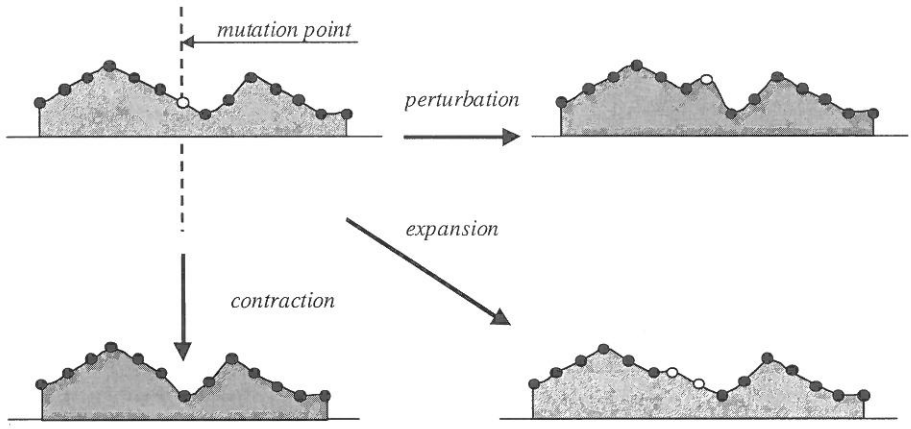

Fig. 7. Mutations in cascaded circuit.

All types of mutation operate on a single, randomly chosen element of the chromosome. *Perturbation* changes the width value of the chromosome element. New value is generated with a uniform distribution from the range $[W_{\min}..W_{\max}]$. During contraction, the chosen element is cut off from the cascade; thus, the chromosome shrinks. On the contrary, expansion inserts single element after the chosen one, and the chromosome expands. The width of the inserted element value is an arithmetic average of the adjacent elements.

We use two types of crossover:

- single-point (Fig. 8),
- two-point (Fig. 9),

affecting only the design topology without changing element values. Both definitions of crossover are very similar to the "classical" ones. In the single-point version, a cut place is chosen randomly in both chromosomes, each chromosome is cut into two pieces, and the remaining parts of chromosomes are exchanged. The same with the two-point crossover, where two cut points are randomly chosen, dividing both chromosomes into three parts, and middle parts are exchanged. Unusually the cut point(s) in both chromosomes are allowed to be completely independent one from another; that is, appropriate parts from both chromosomes can be different in length. Thus, crossover may lead to radical changes of chromosomes' length.

4.3. Experiments and Results

To validate the design method, several circuits were optimized and designed in the microstrip technology. The substrate thickness was 0.635 mm and the relative dielectric permitivity was 9.6. Some examples showing circuits of extremely high level of design complicity (circuits either with a very wide frequency band or with a very high load to source impedance ratio) are presented below.

For the evolutionary algorithm, we assumed the following settings: $p_c = 0.5$ (crossover probability), $p_m = 0.1$ (mutation probability), $|P_t| = 50$ (the number of chromosomes in the base population), $|Q_t| = 50$ (the number of chromosomes in the offspring population). During the execution of EA, several quasi-optimal solutions are produced (see Fig. 10). Since these designs may differ in length, these solutions are, in fact, optimal for a given problem dimension (length of the genotype). In general, the electrical quality of the solution (input reflection coefficient) grows with the increase of the circuit length, contrary to the economical profitability. Therefore, the globally optimal design is a compromise between the electrical and economical factors. The designer's objective is to find the circuit of minimal length for a given maximal admissible reflection coefficient (typically from the range 20 to 40 dB) in the frequency band.

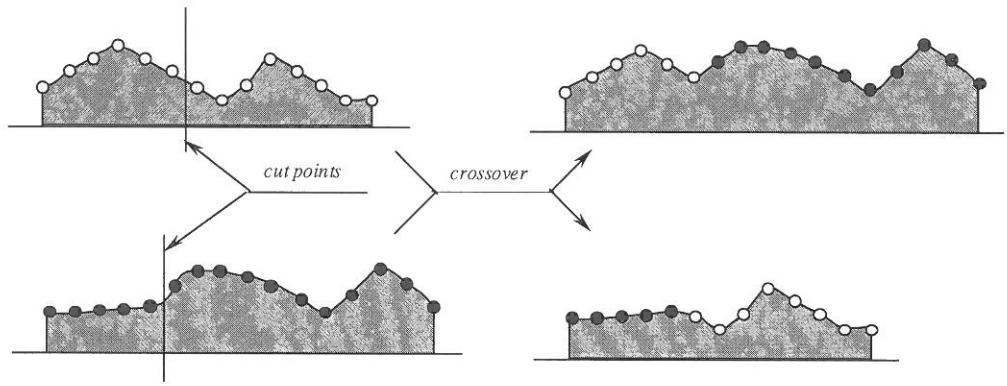

Fig. 8. One-point crossover in cascaded circuits.

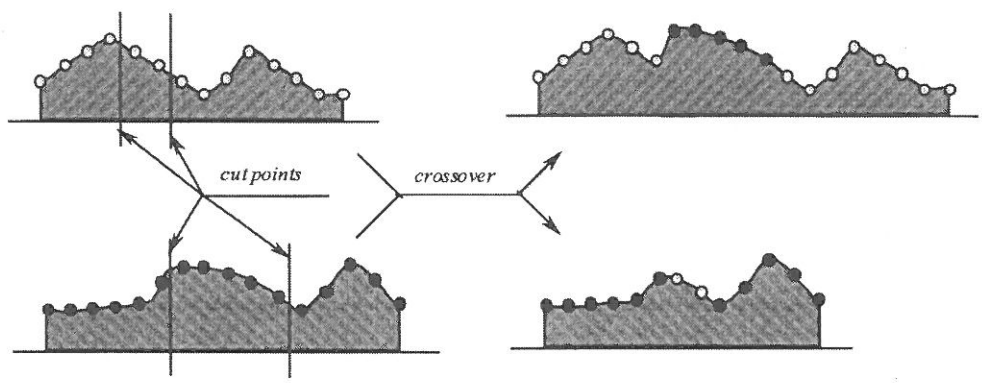

Fig. 9. Example of two-point crossover with cascaded encoding.

4.3.1. Problem 1

The aim was to design a transformer matching the 50Ω source to the 20Ω load. The circuit works in octave frequency band.

The best solution was found by the algorithm after 13th generation and is presented in Fig. 11. Frequency characteristics of the design are presented in Fig. 12. By using the local method it was possible to improve the solution by 4dB. Additionally the final circuit was simulated using Quick Wave Coaxial simulator [5] showing good correlation with the theoretical results.

4.3.2. Problem 2

The hybrid EA optimization method was used to the design of 50Ω to 20Ω impedance transformer in the decade frequency band (0.3 - 3 GHz). The shape of the optimized circuit is shown in Fig. 13. Input reflection coefficient of the circuit is less than 0.05 (26 dB - value typical for many applications). Total circuit length is 167 mm.

4.3.3. Problem 3

Another design example is presented in Fig. 14. The aim of the circuit is to match the 50Ω source to the 2Ω load in the 0.95 - 1.05 GHz band. The maximal input reflection coefficient is 20 dB (excellent for typical applications). Total circuit length is 203 mm.

4.3.4. Problem 4

The EA can be also applied for the design of other devices like amplifiers and filters. An example of low-pass filter is presented in Fig. 15. The filter should have input reflection coefficient better than 0.1 (20dB) in the pass-band (0-15 GHz) and attenuation better than 25dB

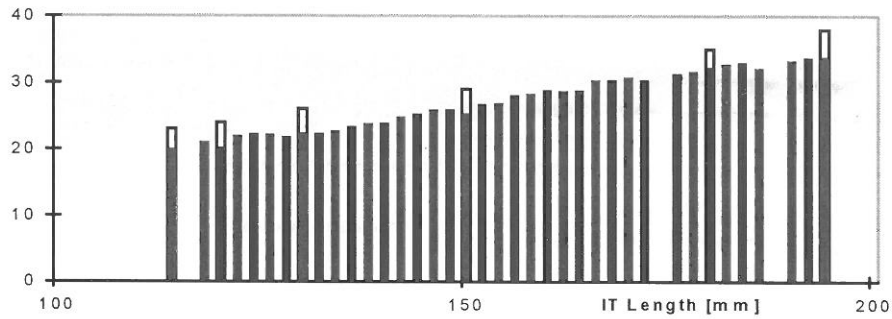

Fig. 10. Variety of solutins generated by Evolutionary Algorithm. Gray bars indicate designs generated by the lone EA, and bars with empty fill represent solutions obtained after tuning by NOA the EA-generated ones.

in the stop-band (20-35 GHz). Optimized frequency characteristics are presented in Fig. 16.

In conclusion we emphasize the following.

- "Local" tuning method is able to end up with a solution dramatically different from the starting point. We observed that (with a fixed number of sections) NOA can be treated as a global rather than a local method.

- We have also observed that the shape of the optimal circuit, although being designed as an arbitrary curve, usually evolves into a stepped impedance cascade with varying section lengths.

These observations encouraged us to step forward and change the chromosome encoding. The chromosome may consist of functional block classes instead of section parameters, since finding appropriate values of the parameters is performed quite efficiently. Thus, the evolutionary algorithm will perform discrete optimization task. Additionally, the considered circuit class can be enlarged to tree-like structures.

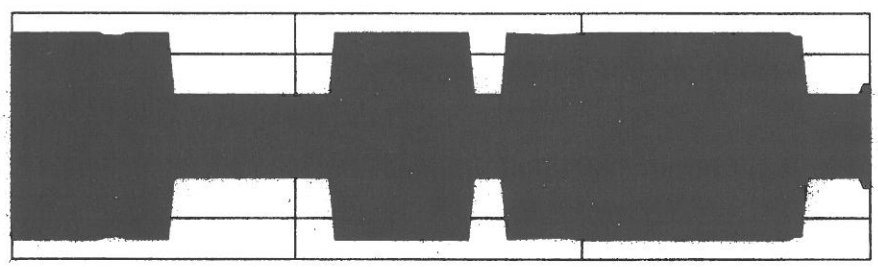

Fig. 11. Shape of the matching circuit (not to scale) after local tuning.

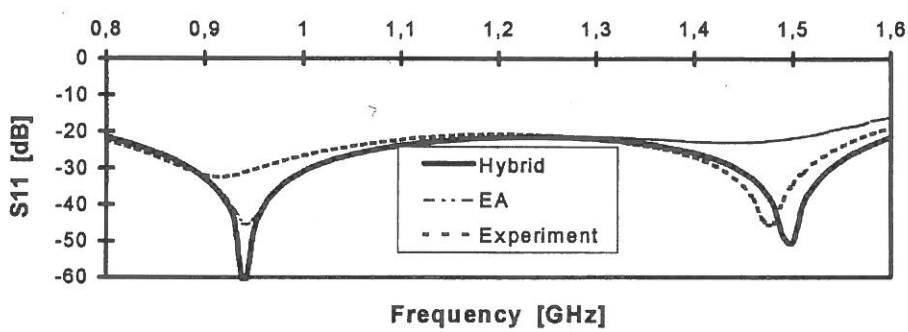

Fig. 12. Frequeny characteristics of the matching circuit. Shaded (EA), solid (Hybrid), and dotted curves denote reflection coefficient (|Γ| or S11) after evolutionary structure optimization, local tuning and simulation by the Quick Wave [5], respectively.

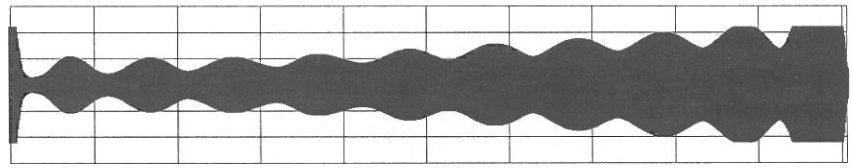

Fig. 13. Shape of the matching circuit 50Ω–20Ω (not to scale) in 0.3–3 GHz band.

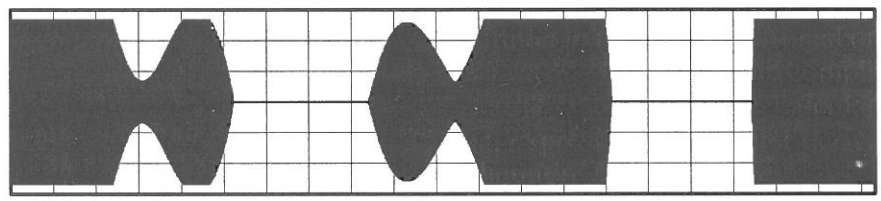

Fig. 14. Shape of the matching circuit 50Ω–2Ω (not to scale) in 0.95–1.05 GHz band.

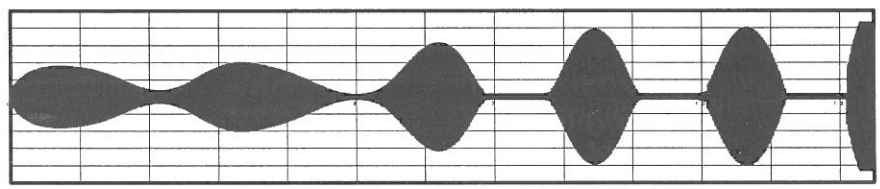

Fig. 15. Shape of the low-pass filter (not to scale) in 0.1–35 GHz band.

5. Tree-shaped Circuits

5.1. Chromosome Structure and Evaluation

In this approach, the aim of the evolutionary algorithm is to optimize circuits in the form of a tree. Each node of the tree is either a connection of links, which are functional blocks (FB), or a special node (*source, load, short circuit, open circuit*).

FB corresponds to a certain circuit class, characterized by the element type and its electrical parameters. It can be, for example, a low impedance transmission line, high capacity capacitor, etc. FB classes (each of them having its electrical parameters) are defined by the designer of the algorithm. A node does not have any particular electrical parameters - it defines only the structure of the tree. In the planar technology, we have constrained ourselves to nodes connecting two, three, or four FBs. Each link (FB) is connected to two nodes. Additionally, there must exist exactly a single load node, likewise with the source. Each terminal node of the tree must be chosen from the set of special nodes.

We stress the difference in meaning between the *stem* of the tree, and its *branches*. A stem is a cascade of connected FBs, connecting source and load. A branch is a sub-tree, with its root connected to the node from the stem. An example of the tree-shape circuit encoding is depicted in Fig. 17.

Similarly to the cascaded encoding, a multi-step procedure is performed to evaluate the chromosome. First, each FB is substituted by its parameters. In our experiments, we assumed that each FB is a transmission line, implemented as a metallization strip of width wi and length l_i. Then, in the same way as for the cascade, the

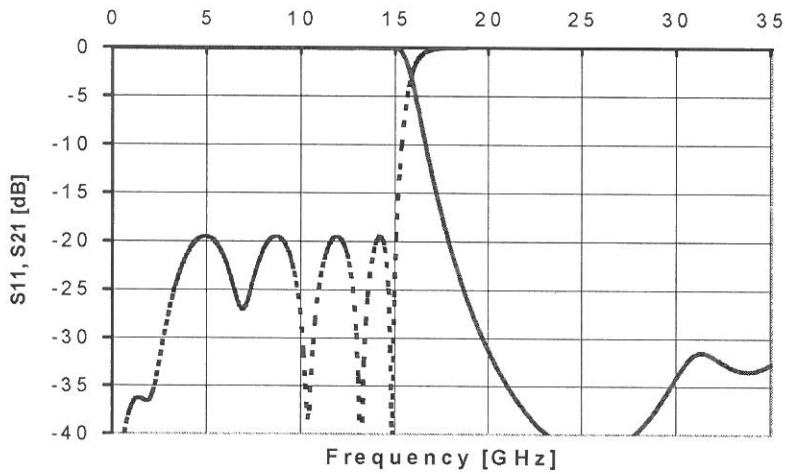

Fig. 16. Frequency characteristics of the optimal low pass filter, obtained by QuickWawe EM Simulator [5]. The dotted line denotes input reflection coefficient $|\Gamma|$ or S11), and the solid line denotes signal attenuation (S21).

tree of strips is passed to the NOA, which produces a new solution whose evaluation is treated as fitness of the chromosome.

5.2. Genetic Operators

We used three types of mutation-type genetic operators: FB perturbation, FB contraction, and FB expansion. A crossover operator is defined in a similar way to one point crossover, however it acts in a different way in tree branches than stem branches.

During *perturbation* (Fig. 18), each FB changes its FB class with the probability p_m. A new value is selected with uniform distribution from the set of all FB classes. *Contraction* consists

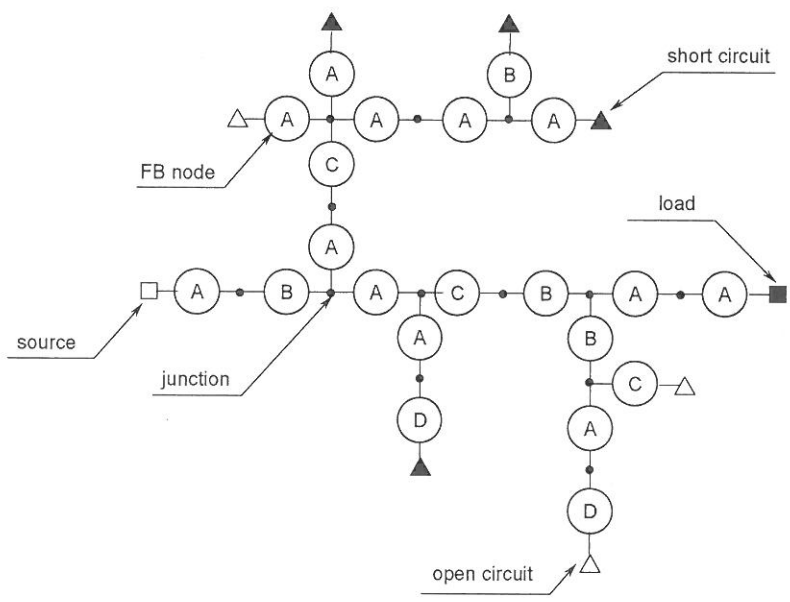

Fig. 17. Example of the three-shaped circuit encoding.

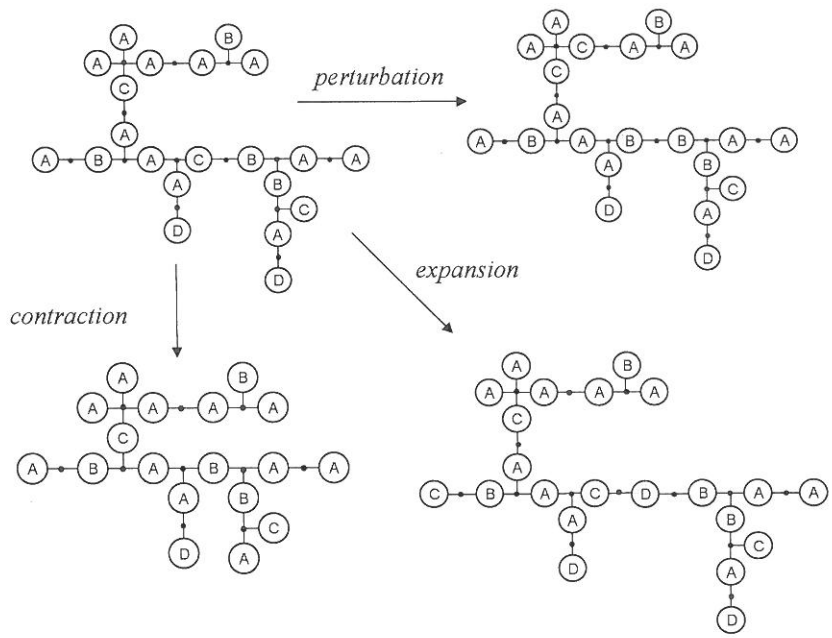

Fig. 18. Example of mutations with tree-shaped encoding. Details (like open- and short-circuits) have been omitted.

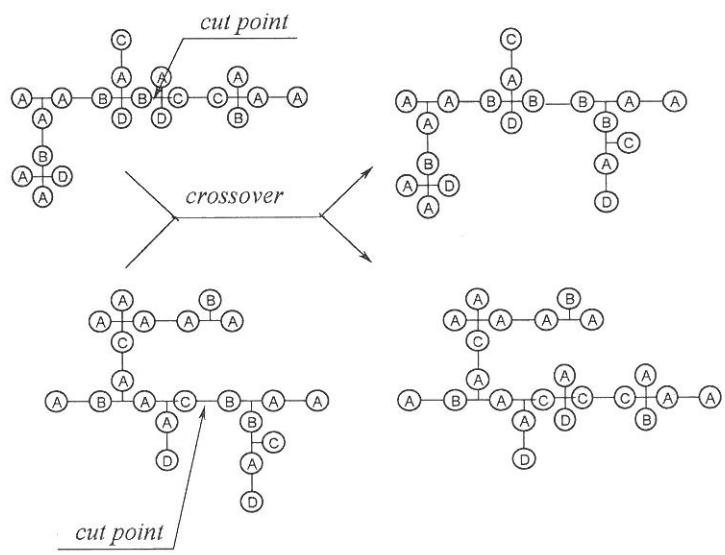

*Fig. 19.*Crossover of a sistem with tree-shaped encoding. Details (like open- and short-circuits) have been omitted.

in shrinking single FB; that is, in replacing a FB with its two nodes by a single node. Therefore, the FB may not be selected freely - otherwise its shrinking might cause unfeasibility of the new tree. A FB can be selected to shrink if at least one of its nodes is connected to exactly two FBs. In the effect of contraction, nodes of the shrunk FB are joined together. During *expansion*, a node is selected with uniform distribution. Then, the node is replaced by a FB (FB class selected randomly) with two nodes. Special nodes do not undergo mutations.

While performing *crossover*, a node is selected for the first parent. If the node belongs to the

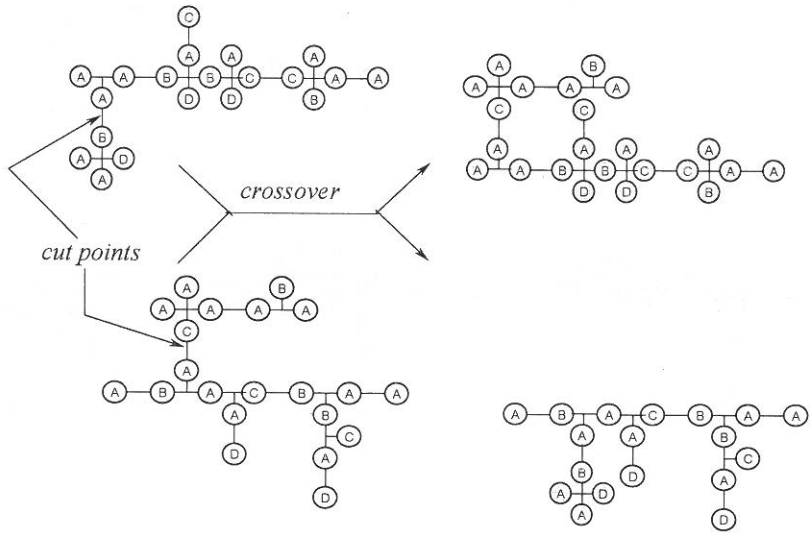

Fig. 20. Crossover of a branch with tree-shaped encoding. Details (like open- and short-circuits) have been omitted.

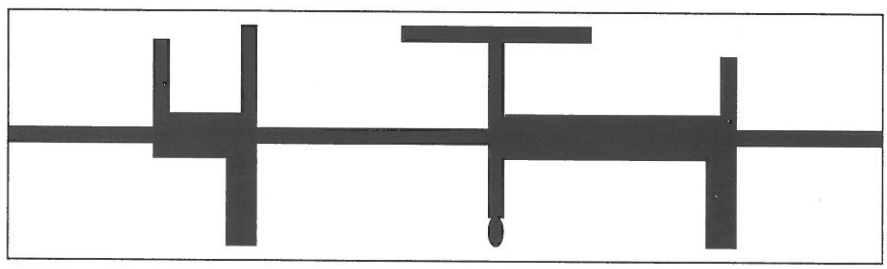

Fig. 21. Shape of the matching circuit 50Ω–20Ω (not to scale) in 0.3–3 GHz band.

stem, then for the second parent another node from the stem is randomly selected (Fig. 19). Otherwise (if a node belongs to a branch), a node from a branch is selected at random for the second parent (Fig. 20). After that, links coming out from the selected nodes towards leafs (load) are cut, and interchanged between chromosomes. As a result, two offspring trees are created.

5.3. Results of the Tree Shape Circuit Optimization

Some problems presented in section 4.3 were solved once again, using the evolutionary algorithm with tree-shaped chromosomes. Settings of the evolutionary algorithm were similar to the cascaded case.

5.3.1. Problem 5

The hybrid EA optimization program was used to the design of 50Ω to 20Ω impedance transformer in the decade frequency band (0.3 - 3 GHz). The shape of the optimized circuit is provided in Fig. 21. Input reflection coefficient of the circuit is better than 0.05 (26 dB). Total circuit length is significantly smaller than for the cascaded circuit and equals 108 mm.

5.3.2. Problem 6

Another design example is presented in Fig. 22. The aim of the circuit is to match the 50Ω source to the 2Ω load in the 0.95 - 1.05 GHz band.

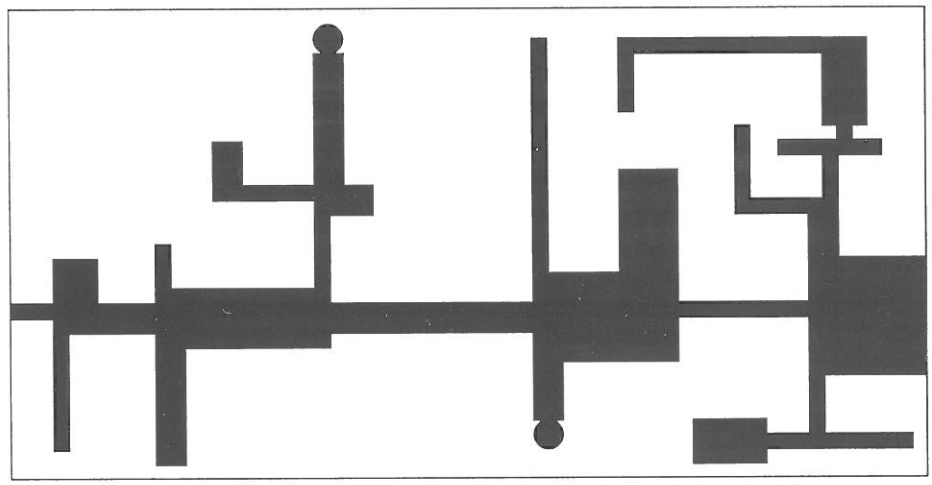

Fig. 22. Shape of the matching circuit 50Ω–2Ω (not to scale) in 0.95–1.05 GHz band.

Input reflection	15 dB	20 dB	30 dB
Quarter-wave transformer	100 x 40 mm 2 sections		150 x 40 mm 3 sections
Non-synchronous transformer		80 x 40 mm 6 sections	120 x 40 mm 8 sections
Evolutionary transformer	50 x 40 mm	73 x 40 mm	144 x 40 mm
Hybrid cascade transformer	44 x 40 mm	58 x 40 mm	102 x 40 mm
Hybrid tree transformer	40 x 48 mm	44 x 48 mm	52 x 48 mm

Table 1. Comparison of dimensions of the transformer for a given reflection coefficients.

The input reflection coefficient is 34 dB. Total circuit length is 126 mm. This result is a significant improvement comparing to the cascaded encoding, since both the circuit and the maximal reflection coefficient are much smaller.

5.4. Comparison of Properties of Design Methods

In the examples given in sections 4.3 and 5.3, transformer matching the 50Ω source to the 20Ω load is chosen as a typical design problem. However, the frequency band should be narrowed to the range where theoretical solution (quarter-wave transformer) [1] is available. In this case, a band from 1 GHz to 2 GHz was chosen. For a given frequency band and maximal admissible reflection coefficient, the quality of the transformer design depends mostly on its occupied surface, which should be minimal in order to reduce manufacturing cost.

In table 1 we compare the results obtained with the evolutionary optimization to those obtained with more conventional methods as detailed below:

- evolutionary transformer - cascaded matching circuit generated by the rough algorithm, without use of the local tuning,
- hybrid cascade transformer - cascaded matching circuit generated by the algorithm with the local tuning,
- hybrid tree transformer - tree-shape matching circuit generated by the algorithm with the local tuning,

and for "classical" designs:

- quarter-wave matching circuit (SIM), consisting of the cascade connection of the equal length transmission line sections; length of each section equals the quarter-wave length for the middle band frequency,
- non-synchronous [15] (SIM); the circuit consists of cascade connection of transmission line sections with varying length; the characteristic impedance of each section can be set either to the high (120Ω) or to the low value (20Ω).

The surface of the circuit's board after applying the evolutionary algorithm can be significantly reduced. The change, for a low performance transformer (15dB), is rather small, but increases with sharpening of the design requirements (better reflection coefficient).

6. Conclusions

In this paper we present original methods for the application of evolutionary computation techniques to the design of a class of planar electronic circuits. This application is one of the first in the field of planar circuit design.

Up until now, existing circuit design methods were based either on a static structure (which was predetermined by the designer), or the designer used to change the topology manually. The importance of the presented approaches rests in the fact that they allow for variable size and (even more important) variable structure of the circuit.

Both methods are hybrid ones, in which the evolutionary algorithm is used to optimize circuit structure, and the circuit parameters are tuned by the local non-smooth method (NOA). In the evolutionary algorithm, we use problem-specific encoding and genetic operators. Genetic operators, which are extensions to the standard ones, use the problem knowledge from the existing engineering design methods. Thus, it is possible to avoid a completely blind search, which might have caused severe increase of the computational effort to find the solution.

The first approach is limited to the class of cascaded circuits. We are able to find designs that are comparable or better than circuit designs by existing methods.

In the second approach, we represent the circuit elements by their classes, instead of their electrical parameters. Thus, the approach is more general, and we can avoid multiple runs of the local tuning method in the attraction basin of the same local optimum. It needs emphasizing that this method generated original topologies of the electronic circuits with improved electrical parameters. It seems questionable (or even impossible) that an engineer could generate such structures using conventional design knowledge and practice.

References

[1] G. MATTHAEI, L. YOUNG, E.M.T. JONES, *Microwave Filters, Impedance Matching Networks and Coupling Structures*, Artech House 1980, pp. 365–372.

[2] WAI–KAI CHEN, *Theory and Design of Broadband Matching Network*, Pergamon Press, 1976.

[3] J.W. BANDLER, S.H. CHEN, "Circuit Optimization: The State of The Art", *IEEE Trans. MTT*, vol. 36, 1988, pp. 424–443.

[4] W.K. GWAREK, "Analysis of an Arbitrarily-Shaped Planar Circuit – a Time Domain Approach", *IEEE Trans. MTT*, vol. 33, No 10, 1985, pp. 1067–1072.

[5] "QuickWave – 3D a general purpose electromagnetic simulator based on conformal finite-difference time-domain method", QWED s.c., http//www.ire.pw.edu.pl/qw3d.

[6] J. ARABAS, P. MIAZGA, "Design of an Impedance Transformer Using Hybrid Approach Based on an Evolutionary Algorithm", *Proc. 15th World Congress on Scientific Computation, Modeling and Applied Mathematics*, IMACS 1997, Berlin, Germany, Aug. 24–29, 1997, pp. 633–638.

[7] N. JAIN, P. ONNO, "Methods of Using Commercial Electromagnetic Simulators for Microwave and Millimeter-Wave Circuit Design and Optimization", *IEEE Trans. MTT*, vol. 45, No. 5, May 1997, pp. 724–746.

[8] P. MIAZGA, W. GWAREK, "Improved Design of Passive Coaxial Components Using Electromagnetic 2–D Solver in an Optimization Loop", *IEEE Trans. MTT*, vol. 45, May 1997, pp. 858–860.

[9] A. JOHN, R.H. JANSEN, "Evolutionary Generation of (M)MIC Component Shapes Using 2.5D EM Simulation and Discrete Genetic Optimization", *Proc. 1996 IEEE MTT International Symposium*, June 20–23, 1996, pp. 745–748.

[10] P. MIAZGA, T. CEGIELSKI, J. POPKOWSKI, "Application of Genetic Algorithm with Adaptive Error Function for the Design of a Class of Planar Circuits", (in Polish) *Proc. 2nd Conference: "Evolutionary Algorithms and Global Optimization"*, Rytro, Poland, Sept. 15–19, 1997, pp. 167–174.

[11] B.M. KAC, W.P. MISHANOV, A.L. FELDSTEIN, *Optimal Synthesis of VHF Devices with TEM Waves*, Radio i Sviaz, Moskva, 1984 (in Russian).

[12] Z. MICHALEWICZ, *Genetic Algorithms + Data Stuctures = Evolution Programs*, Springer, 1995 (3rd ed.).

[13] J.W. BANDLER, Q.J. ZHANG, "An Automatic Decomposition Technique for Device Modeling and Large Circuit Design", *IEEE MTT Symposium Digest*, 1987, pp. 709–712.

[14] P. MIAZGA, A. KOZAK, "Synthesis of Better Microwave Devices Based on Graph Search Methods", *Proc. Mikrowellen und Optoelektronik Symp., MIOP 1995*, Singelfingen, Germany, pp. 229–223.

[15] S. ROSLONIEC, "Algorithms for the Computer-Aided Design of Nonsynchronous, Noncommensurate Transmission-Line Impedance Transformers", *International Journal of Microwave and Millimeter-Wave Computer-Aided Engineering*, vol. 4, No. 3, 1994, pp. 307–314.

[16] K. KIWIEL, A. STACHURSKI, "NOA1: A FORTRAN Package of non-differentiable optimization algorithms Methodological and User's Guide", IIASA Working Paper WP–88–116, December 1988.

[17] H.P. SCHWEFEL, *Optimization of Numerical Model*, Wiley, 1995.

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