

# Development of Robust Discrete controller for Double Frequency Buck converter

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Original scientific paper

A discrete controller is designed for high efficiency double frequency buck converter. This double frequency buck converter is comprised of two buck cells: one works at high frequency, and another works at low frequency. It operates in a way that current in the high frequency switch is diverted through the low frequency switch. Thus, the converter can operate at very high frequency without adding any additional control circuits. Moreover, the switching loss of the converter remains small. The proposed converter exhibits improved steady – state and transient response with low switching loss. A digital compensator further improves the dynamic performance of the closed loop system. Simulation of digitally controlled double frequency buck converter is performed with MATLAB / Simulink. Experimental results are given to demonstrate the effectiveness of the controller using LabVIEW with a Data Acquisition Card (NI - 9221).

**Key words:** Analog to Digital conversion, Digital compensator, Double frequency (DF) buck converter

## Razvoj robusnog diskretnog regulatora za silazni pretvarač s dvostrukom frekvencijom preklapanja.

Diskretni regulator je projektiran za postizanje visoke efikasnosti silaznog pretvarača s dvostrukom frekvencijom preklapanja. Ovaj silazni pretvarač s dvostrukom frekvencijom preklapanja sastoji se od dvaju ćelija: po jedna za rad na visokim i niskim frekvencijama preklapanja. Regulator funkcionira tako da se struja preklapanja na visokim frekvencijama preusmjerava kroz prekidač za preklapanje na niskim frekvencijama. Tako pretvarač može funkcionirati na vrlo visokim frekvencijama bez dodatnih upravljačkih krugova. Štoviše, gubici prekidanja pretvarača ostaju mali. Prikazani pretvarač pokazuje poboljšanja kod odzivu u ustaljenom stanju te u prijelaznim pojavama uz male gubitke prilikom prekidanja. Digitalni kompenzator nadalje poboljšava dinamičke performanse sustava u zatvorenom krugu. Simulacije digitalno upravljano silaznog pretvarača s dvostrukom frekvencijom preklapanja su provedene korištenjem MATLAB / Simulink-a. Eksperimentalni rezultati su prikazani kako bi se demonstrirala efikasnost regulatora korištenjem LabVIEW-a i kartice za prikupljanje podataka (NI - 9221).

**Ključne riječi:** Analogno digitalni pretvarač, Digitalni kompenzator, Silazni pretvarač s dvostrukom frekvencijom preklapanja

## 1 INTRODUCTION

In many applications like switching mode regulator, battery chargers, fuel cell applications and Photo voltaic arrays, dc-dc converters are widely used. DC – DC conversion method is more power efficient which provides an efficiency of 75% to 98%. The efficiency has been increased due to the use of power MOSFETs which are able to switch at high frequency more efficiently than power bipolar transistor. These converters are smaller in size therefore they are used extensively in personal computers, computer peripherals, communication, medical electronics and adaptors of consumer electronic devices to provide different level of DC voltages [2 – 5].

Especially in portable consumer electronics and battery chargers Buck converters play a vital role. In order to im-

prove the transient and steady state performance of power converters and to enhance power density, high switching frequency is an effective method. However, switching frequency rise causes higher switching losses and greater electromagnetic interference. The purpose of double frequency buck converter is to achieve good dynamic response and high efficiency in Buck converters [1]. This topology consists of a high-frequency and low-frequency buck converter operates with a single supply voltage. The current flowing through the high-frequency cell is diverted by the low-frequency one, which also processes the majority of the converter power. This current decreases rapidly so that the high-frequency cell can work at very high frequency to improve the dynamic response. Furthermore, the efficiency is enhanced due to the low-current process-

ing requirement of the high-frequency cell in the DF buck converter. The proposed converter does not incur the circulating current problem like interleaved converter.

The main challenge in the field of Power Electronics is emphasized more on the control aspects of the DC-DC converter. The control approach requires effective modeling and a thorough analysis of the converters. The switching power converters in general are non-linear and time invariant. The major disadvantages of the double Frequency Buck converter are its dependence on large passive components.

In conventional analog controller design approaches, difficulty in control, lack of flexibility to higher functions and system alteration, and low reliability. The design of digital controller offers many advantages over their analog counterpart. Some of its advantages are i) Digital components are less susceptible to aging and environmental variations ii) less sensitive to noise, iii) changing a controller does not require an alteration in the hardware iv) improved sensitivity to parameter variations v) flexibility of its modifying controller characteristics vi) ease of operation. Digital controller provides stability, faster response and minimal overshoot in its dynamic response.

In digital approach the three areas which find significance in the research are 1) Analog to Digital Conversion (ADC) used to sample the error voltage 2) the digital compensator which compensate the error signal 3) Digital Pulse Width Modulation (DPWM) signals are generated with highest resolution in order to obtain high accuracy in required output voltage. In this paper, high resolution DPWM signals are generated keeping the system switching frequency high to provide the compensator. The control objective in the design of controller is to drive the double frequency buck converter switch with a duty cycle so that the dc component of the output voltage is equal to the reference voltage. The regulation should be maintained constant despite variations in the input voltage or in the load. Furthermore, the constraints in the design of controller results due to the duty cycle which is bounded between zero and one. This problem can be solved by modeling the dc-dc converters using state space averaging technique. By using this technique, the converter can be described by a single equation approximately over a number of switching cycles. The averaged model makes the simulation and control design much faster [6].

The foremost objective of this work is to design a robust compensator based on discrete PID, which overcomes the above mentioned problems. The design is based on time domain in which the converter specifications such as rise time, settling time, maximum peak overshoot and steady state error are met. The double frequency buck converters are modeled using state space averaging technique and the digital compensator is designed by discrete PID

technique. Switching losses across the power converters are found using PSIM Software. MATLAB / Simulink is used to perform simulation.

## 2 OVERALL BLOCK DIAGRAM

The overall block diagram of the double frequency buck converter with the entire set up is shown in Figure.1. The output voltage of the double frequency buck converter is compared against the desired value of the reference voltage using the comparator circuit (Operational Amplifier IC 741). The Digital compensator is designed for the double frequency buck converter using digital compensation technique. The error output thus obtained is fed into the inbuilt block diagram section of the LabVIEW through the Data Acquisition Card, DAQ NI 9221.

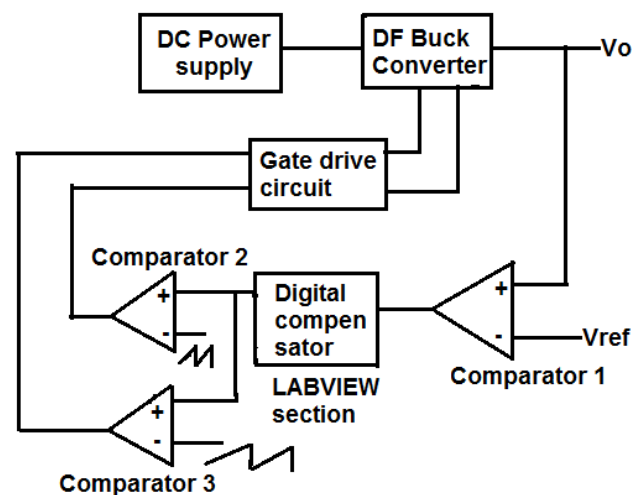


Fig. 1. Overall Block diagram

The LabVIEW section consists of Analog to Digital conversion, discrete transfer function and Digital to Analog conversion blocks. Inside the block diagram of LabVIEW section Analog to digital conversion takes place and thus processed signal is fed into the discrete transfer function block in which the designed controller value is entered. The output of the controller is acquired back by DAQ card and fed into the comparator 2 and comparator 3 also designed using operational amplifiers (IC 741). This signal is compared against different ramp signals with desired switching frequencies obtained from signal generator. The resulting PWM switching pulses are fed to the switches of the DF buck converter through the gate drive circuits.

## 3 DESIGN OF DF BUCK CONVERTER

For buck converter of Figure.2 operates in Continuous Conduction Mode (CCM), the relationship between the input voltage ( $V_s$ ) and the output voltage  $V_o$  is given as [7].

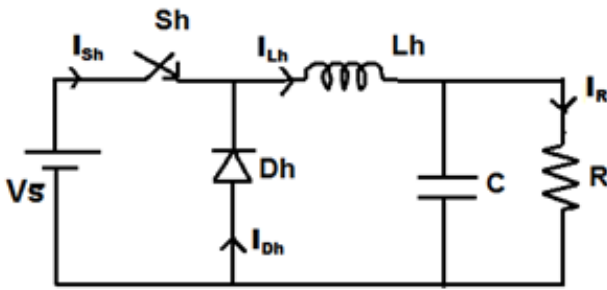


Fig. 2. Conventional Buck converter

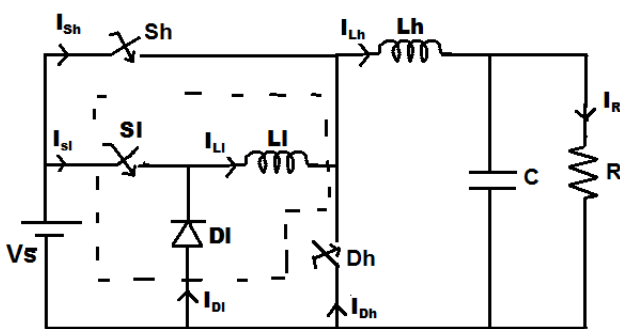


Fig. 3. Proposed DF Buck converter

$$d = \frac{V_o}{V_s} \tag{1}$$

where  $d = \frac{T_{ON}}{T_h}$  is the duty cycle,  $T_h$  is the switching period of the high frequency and  $T_{ON}$  is the conducting time of switch  $S_h$ . The boundary conduction of Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) of the buck converter is the critical value of the inductor  $L_c$ , and is given by

$$L_c = \frac{(1 - d \lll) R}{2f_h} \tag{2}$$

where  $R$  is the load resistance and  $f_h$  is the high switching frequency. The selected inductance  $L_h$  should be greater than  $L_c$  for CCM. However, the inductor value determines the magnitude of ripple current in the output capacitance as well as the load current at which the converter enters into DCM.

Normally 30% ripple of the average output current is considered for design. The  $L_h$  can be determined by

$$d(V_s - V_o) = f_h L_h \Delta I \tag{3}$$

where  $\Delta I$  is the ripple current. The capacitor  $C$  is then determined by the allowed voltage ripple  $\Delta V_C$ , which is

typically 2% of the output voltage. The capacitor value is determined by

$$\Delta V_C = \frac{\Delta I}{8Cf_h} \tag{4}$$

The proposed DF buck converter is shown in Figure. 3. The buck cells work at two different frequencies. The cell containing  $L_h$ ,  $S_h$  and  $D_h$  works at higher switching frequency, and is called the high-frequency buck cell. Another cell containing  $L_l$ ,  $S_l$  and  $D_l$  works at lower switching frequency, and is called the low-frequency buck cell. The low-frequency buck cell is to improve the converter efficiency and the high-frequency buck cell is used to enhance the output performance. An active switch, instead of a diode as in the conventional buck converter, is employed to realize the  $D_h$  in the high frequency buck cell. This active switch transfers the energy stored in the low-frequency cell, it works complementary with high-frequency cell switch  $S_h$ , and improves the transient response [1]. The inner cell inductor  $L_l$  is determined by

$$L_l = \frac{d(V_s - V_o)}{\Delta I f_l} \tag{5}$$

where  $f_l$  - low switching frequency. The following are the parameters considered for the design of DF buck converter:  $V_s = 48$  V,  $V_o = 10$  V,  $f_h = 100$  KHZ,  $f_l = 10$  KHZ,  $L_l = 1$  mH,  $L_h = 100$   $\mu$ H,  $C = 470$   $\mu$ F and  $R = 4$   $\Omega$ . Figure 4 shows the simulation result of open loop DF buck converter, it comprises of voltage across inner cell inductor and outer cell inductor and current through inner cell inductor and outer cell inductor respectively.

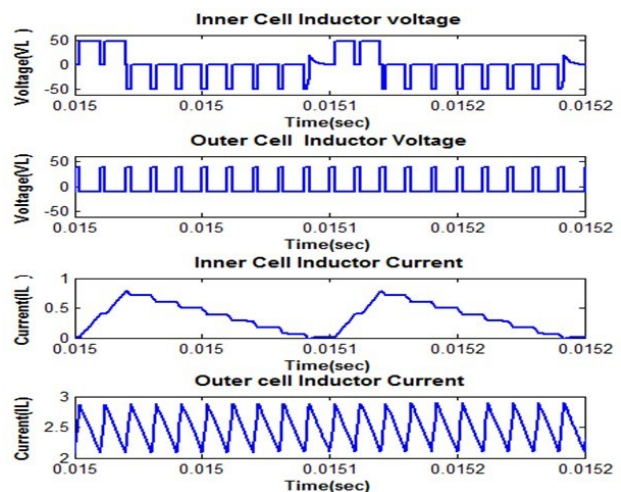


Fig. 4. Waveforms are voltage across the Inner cell inductor, outer cell inductor and current through the inner cell inductor, outer cell inductor for DF buck converter

#### 4 EFFICIENCY ANALYSIS

In order to analyze the efficiency improvement of the double frequency buck converter, the efficiency expression is discussed in the section. The analysis is also applied to the single high-frequency buck and low-frequency buck converters. A simple loss model is adopted here in that we just want to show the efficiency relationship between DF buck, single low-frequency buck and single high-frequency buck converter. The conduction losses of active switch and diode are found according to their conduction voltage  $V_{on}$  and  $V_f$ . Where  $V_{on}$  is ON state voltage and  $V_f$  is the forward voltage of the switches. Since the switching losses usually dominates the total loss [1].

##### 4.1 Single frequency buck converter

In a single-frequency buck converter, the total loss consists of four parts, the conduction loss  $P_{dcon}$  and switching loss  $P_{sd}$  of the diode and the conduction loss  $P_{scon}$  and switching loss  $P_{ss}$  of the active switch. When the input voltage is  $V_s$ , duty ratio is  $d$ , and the current through the inductor is  $I_{Lh}$ .  $t_{on}$  - ON time of the switch or diode,  $t_{off}$  - OFF time of the switch or diode and the switching frequency is  $f_s$ . The losses can be estimated according to the following equations and Figure 5c and Figure 5d.

$$P_{Scon}(MOSFET) = dv_{on}I_{Lh} \quad (6)$$

$$P_{dcon}(Diode) = (1 - d)V_f I_{Dh} \quad (7)$$

$$P_{ss}(MOSFET) = \frac{1}{2}f_s V_S I_{Lh}(t_{on} + t_{off}) \quad (8)$$

$$P_{sd}(Diode) = \frac{1}{2}f_s V_S I_{Dh}(t_{on} + t_{off}) \quad (9)$$

##### 4.2 DF buck converter

The losses comprise of two portions: Outer cell losses and inner cell losses.  $i_{Lh}$  is the outer cell inductor current,  $t_{on}$  is the conducting time of the switch,  $t_{off}$  is the OFF time of the switch,  $i_{Ll}$  is the inner cell inductor current,  $i_{Lh}$  is the outer cell inductor current,  $f_h$  is the high switching frequency and  $f_l$  is the low switching frequency [1]. The losses across the outer cell switch and inner cell switch are shown in Figure 5a and Figure 5b respectively. The losses in the outer cell are

$$P_{Scon}(MOSFET) = dv_{on}i_{Lh} \quad (10)$$

$$P_{dcon}(MOSFET) = (1 - d)V_f I_{Lh} \quad (11)$$

$$P_{ss}(MOSFET) = \frac{1}{2}f_h V_S I_{Lh}(t_{on} + t_{off}) \quad (12)$$

$$P_{sd}(MOSFET) = \frac{1}{2}f_h V_S I_{Lh}(t_{on} + t_{off}) \quad (13)$$

Table 1. Comparison of the losses occur in the types of Buck converter

Types of Buck converter	Losses (watts)	Output power (watts)	Efficiency (%)
Single Low Frequency Buck converter	1.516	21.57	93.43
Single High Frequency Buck converter	2.205	24.58	91.77
DF Buck Converter	1.6726	24.62	93.64

The losses in the inner cell are

$$P_{Scon}(MOSFET) = dv_{on}i_{Ll} \quad (14)$$

$$P_{dcon}(MOSFET) = (1 - d)V_f I_{Ll} \quad (15)$$

$$P_{ss}(MOSFET) = \frac{1}{2}f_l V_S I_{Ll}(t_{on} + t_{off}) \quad (16)$$

$$P_{sd}(MOSFET) = \frac{1}{2}f_l V_S I_{Ll}(t_{on} + t_{off}) \quad (17)$$

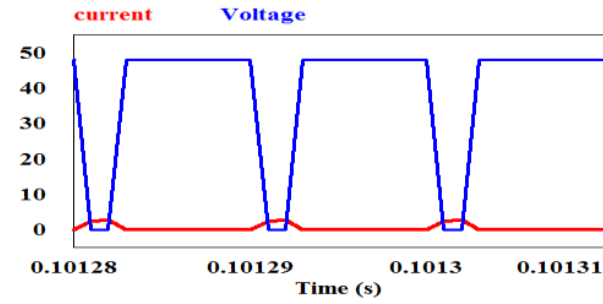
$$Efficiency = \frac{\text{output power}}{\text{output power} + \text{losses}} \quad (18)$$

With the help of Figure 5 and equations (6) to (18), switching losses and conduction losses of single frequency buck converters and double frequency buck converter are found. Table 2 shows the total losses, output power and efficiency of various buck converters. Table 1 proves that the Double frequency buck converter has higher efficiency than all other single frequency buck converter. Outer cell of the DF buck converter is operated by high switching frequency; hence the performance of the converter is also good as shown in the below section of this paper.

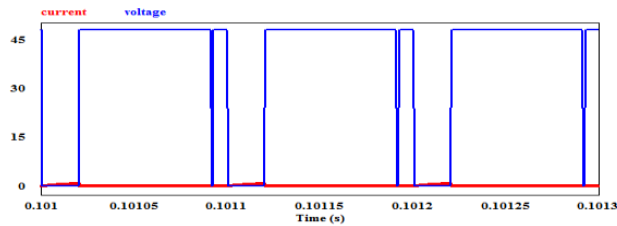
#### 5 MODELLING OF DF BUCK CONVERTER

After the design of DF buck converter, may be simulated using state space averaging technique. The unique feature of this method is that the design can be carried out for a class of inputs such as step, ramp or impulse function in which the initial conditions are also incorporated. This technique is convenient to use for low frequency approximation of the true dynamics where the discontinuous effect introduced by the switching is ignored [7]. The Simulink requires the system equations of the power converter circuit. The state space analysis is discussed now.

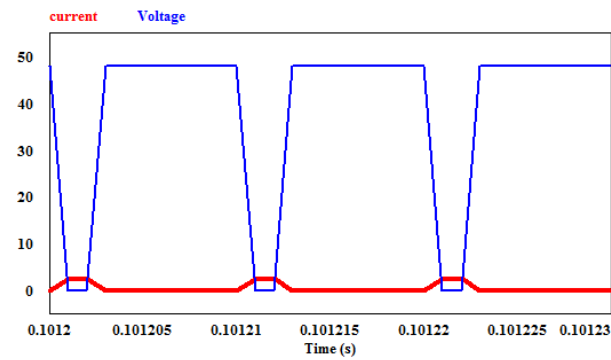
The switches  $S_h$  and  $S_l$  are driven by a pulse sequence with a constant switching frequency  $f_h$ , and  $f_l$  respectively. The state vector for the DF buck converter is defined



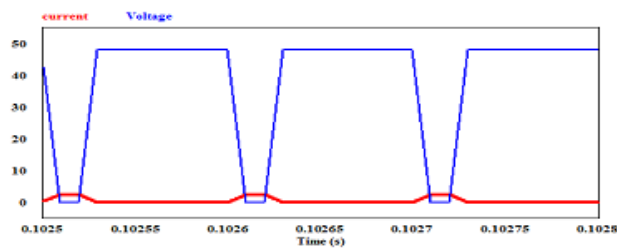
(a) Switching losses at Outer cell switch of double frequency buck converter



(b) Switching losses at Inner cell switch of double frequency buck converter



(c) Switching losses at High frequency buck converter



(d) Switching losses at Low frequency buck converter

Fig. 5. Switching losses for different buck converters

as  $x(t) = \begin{bmatrix} i_{Ll} \\ i_{Lh} \\ V_c \end{bmatrix}$ , where  $i_{Ll}$ ,  $i_{Lh}$  are current through an inner cell inductor and the outer cell inductor respectively and  $V_c$  is the voltage across the capacitor. The system is de-

scribed by the following set of continuous time state space equations:

$$\begin{aligned} \dot{x}(t) &= Ax(t) + BV_s(t) \\ y(t) &= Cx(t) + DV_s(t) \end{aligned} \quad (19)$$

where  $x$  is a state vector,  $V_s$  is a source vector,  $A$ ,  $B$ ,  $C$ ,  $D$  is the state coefficient matrices.

High power densities are possible only for continuous conduction mode (CCM) of operation. Diode  $D_l$  and MOSFET  $D_h$  are always in a complementary state with the switches  $S_l$  and  $S_h$  respectively. When  $S_l$  – ON,  $D_l$  – OFF and vice versa and  $S_h$  – ON,  $D_h$  – OFF vice versa. Four modes of operations are possible, corresponding state equations are

Mode 1:  $S_l$  is ON and  $S_h$  is ON

$$\dot{x}(t) = A_1x(t) + B_1V_s(t) \quad (20)$$

Mode 2:  $S_l$  is ON and  $S_h$  is OFF

$$\dot{x}(t) = A_2x(t) + B_2V_s(t) \quad (21)$$

Mode 3:  $S_l$  is OFF and  $S_h$  is ON

$$\dot{x}(t) = A_3x(t) + B_3V_s(t) \quad (22)$$

Mode 4:  $S_l$  is OFF and  $S_h$  is OFF

$$\dot{x}(t) = A_4x(t) + B_4V_s(t) \quad (23)$$

where

$$A_1 = A_2 = A_3 = A_4 = \begin{bmatrix} 0 & 0 & \frac{-1}{Lh} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} \quad (24)$$

$$B_1 = \begin{bmatrix} \frac{1}{Lh} \\ 0 \\ 0 \end{bmatrix} \quad (25)$$

$$B_2 = \begin{bmatrix} \frac{1}{Ll} \\ 0 \\ 0 \end{bmatrix} \quad (26)$$

$$B_3 = \begin{bmatrix} \frac{1}{Lh} \\ \frac{1}{Ll} \\ 0 \end{bmatrix} \quad (27)$$

$$B_4 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \quad (28)$$

The state space model takes the form described as follows:

$$\dot{x}(t) = [A] [x] + [B] [u] \quad (29)$$

Where  $d$  is the duty cycle ratio.  $d_1, d_2, d_3$  &  $d_4$  are the duty cycle of Mode 1, Mode 2, Mode 3 & Mode 4 respectively [1]

$$[A] = A_1d_1 + A_2d_2 + A_3d_3 + A_4d_4 \quad (30)$$

$$[B] = B_1d_1 + B_2d_2 + B_3d_3 + B_4d_4 \quad (31)$$

$$[u] = V_s \quad (32)$$

We have

$$d_1 + d_2 + d_3 + d_4 = 1 \quad (33)$$

$$d_1 + d_2 + d_3 = d \quad (34)$$

$$d_1 = d_3 \quad (35)$$

$$d_2 = d_4 \quad (36)$$

Hence

$$[A] = \begin{bmatrix} 0 & 0 & \frac{-1}{Lh} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & \frac{-1}{RC} \end{bmatrix} \quad (37)$$

$$B = \begin{bmatrix} \frac{d_1+d_3}{Lh} \\ \frac{d_2-d_4}{Ll} \\ 0 \end{bmatrix} \quad (38)$$

$$Y = [0 \ 0 \ 1] \begin{bmatrix} i_{Ll} \\ i_{Lh} \\ V_c \end{bmatrix} + [0]Vs(t) \quad (39)$$

The state space equations (29) and (39) can be converted into transfer function. The transfer function of the DF buck converter is

$$G(s) = \frac{-1.592 \cdot 10^{-12} s^2 + 3.31 \cdot 10^6 s + 1.015 \cdot 10^{-9}}{s^3 + 572.6s^2 + 6.331 \cdot 10^6 s} \quad (40)$$

The continuous state equations are discretized for the design of discrete PID controller. It is considered that the discrete system is same as that of the continuous system except that the system is sampled with a sampling time, which is assumed as  $1 \mu S$ . The state space solution (40) is evaluated and finds an analog PID controller equation using Ziegler – Nichols method [2].

### 6 CLOSED LOOP CONTROL SYSTEM OF A DF BUCK CONVERTER

Figure 6 shows the closed loop control system of the DF buck converter with Discrete PID – based feedback. The goal is to minimize the error between  $V_{ref}$  and  $V_o$  and to make the system to track the reference signal which is considered as a step input. The output is regulated by using the feedback. The feedback ensures that the output must be insensitive to load disturbances, stable and provides good transient response thereby improving the dynamic performances. The error voltage  $V_e$  (difference between  $V_{ref}$

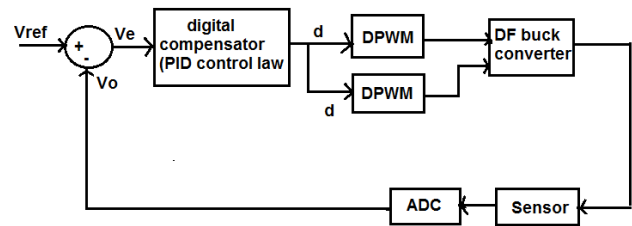


Fig. 6. Closed loop system using discrete controller

and  $V_o$ ) is fed to Analog to Digital converter which samples them at a sampling rate equal to  $1 \mu S$ . The function of the digital compensator is for generating the control signal by compensating the error ( $V_e$ ).

The error is processed by digital compensator block with PID algorithm to generate control signal. For the digital control of DF buck converter switching, discrete PID control can be realized by its compensation block. The control signal from the compensator will affect the converter characteristics significantly, so it is important to find a suitable compensation way by making good use of discrete controller to provide the better converter performance. The output samples control the switch by generating gating pulses when it is processed through Digital Pulse Width Modulation (DPWM) block. The DPWM is nothing but a demodulator which consists of sample and hold block. It includes the delay time ( $t_d$ ), A/D conversion time, switch transition time, computational delay and modulator delay.

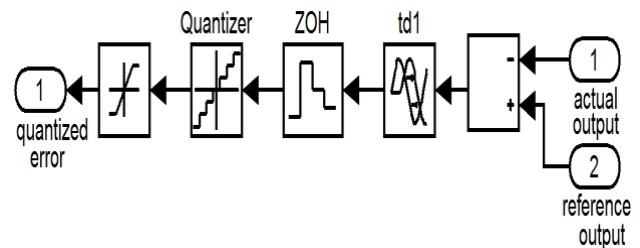


Fig. 7. Analog to Digital converter

Figure 7 shows the block diagram of Analog to digital converter block. It is a device that converts a continuous time signal to a discrete time signal by using sampling. The converter block consists of delay, zero order hold, quantizer and saturation. The delay block carried out the total time between sampling the error signal and updating the duty cycle command at the beginning of the next switching period. The zero order hold is mainly for modeling the sampling effect. Quantizer is mainly used for rounding off or truncating the signal that is to map a larger set of input values to a smaller set such as rounding values to some unit

of precision.

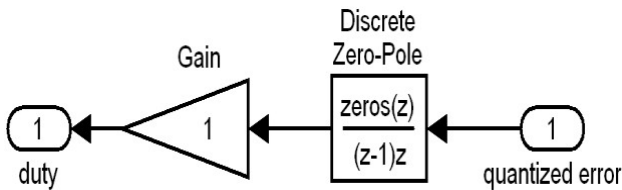


Fig. 8. Discrete Time compensation

The discrete time Compensation block is shown in Figure 8. The output of the A/D converter fed to the discrete zero - pole block which in turn is converted into PWM Pulses using DPWM blocks [8] shown in Figure 9. The discrete time integral compensator thus designed minimizes the error and send the command signal to the switches in the form of pulses in order that the output tracks the reference signal. The output of the compensator is compared against one low frequency ramp signal and one high frequency ramp signal in order that the duty cycles command for the switches are obtained.

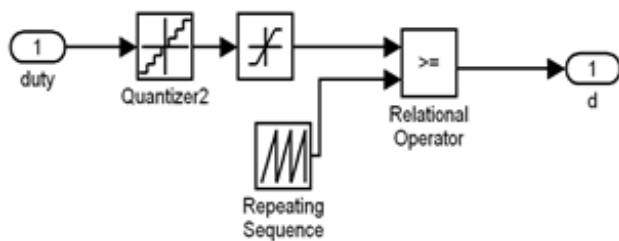


Fig. 9. Digital Pulse Width Modulation

**7 DESIGN OF DIGITAL CONTROLLER**

A closed loop system using a discrete controller is shown in Figure.6. The PID controller block provides the compensation in the feedback control of the DF buck converter. PID controller has the advantages of both PD & PI controller. PD controller improving system stability and increasing system bandwidth, it is a special case of phase-lead controller. PI controller reduces steady - state error is a special case of the phase - lag controller. Hence PID controller is also called as phase lag - lead controller [9 - 10].

The continuous time PID controller can be expressed as [13]:

$$u(t) = K_p[e(t) + \frac{1}{T_i} \int_0^t e(t) dt + T_d \frac{de(t)}{dt}] \quad (41)$$

where  $u(t)$  is the control output,  $K_p$  is the proportional gain constant,  $T_d$  is the derivative time or rate time constant,  $T_i$  is the integral time or reset time constant and  $e$

Table 2. Ziegler – Nichols Tuning Formulae

Type of Controller	$K_p$	$T_I$	$T_D$
P	$0.5K_{cr}$	$\infty$	0
PI	$0.45K_{cr}$	$\frac{1}{1.2P_{cr}}$	0
PID	$0.6K_{cr}$	$0.5P_{cr}$	$0.125P_{cr}$

is the error (difference between reference  $V_{ref}$  and output  $V_o$ ). The role of proportional depends on the present error,  $I$  on the accumulation of past error and  $D$  on prediction of future error [12].

The Laplace transfer function of the corresponding PID controller is given as:

$$U(s) = K_p \left( 1 + \frac{1+T_I T_D s^2}{T_I s} \right) E(s) \quad (42)$$

$$= K_p \left( 1 + \frac{1}{T_I s} + T_D s \right) E(s)$$

Proportional term provides an overall control action proportional to the error signal. Integral term reduces steady state errors through low frequency compensation by an integrator. Derivative term improves transient response through the high frequency compensation by a differentiator.

By proper choice of these tuning parameters a controller can be adapted for a specific converter to obtain a good behavior of the controller system. By using routh – array technique one can find the range of  $K_p$ . The values of  $T_d$  and  $T_i$  are obtained using Ziegler – Nichols tuning rule method. Table 2 shows Ziegler – Nichols tuning formulae. Where  $K_{cr}$  is the critical gain and  $P_{cr}$  is the critical period. By solving characteristic equation,

$$1 + G(s)H(s) = 0 \quad (A)$$

where  $G(s)$  is the transfer function of open loop double frequency buck converter and  $H(s)$  is the unity feedback gain. Hence

$$s^3 + 572.6s^2 + 9.641 \times 10^6 s + 1.015 \times 10^{-9} + K = 0 \quad (B)$$

where,  $K$  is the range of stability. By using routh-array technique, find the value of  $K$ . Fix  $K_{cr}$  within the range of  $K$ . In equation (A) substitute  $s = j\omega$ , find the value of  $j\omega$  then  $P_{cr} = \frac{2\pi}{\omega}$ . The value of  $K_p$ ,  $T_I$  and  $T_D$  can be obtained from Table 2.

The transfer function of the PID controller is

$$U(s) = \frac{G(s)}{d(s)} \quad (43)$$

$$U(s) = K_p + \frac{K_I}{s} + K_D s = \frac{K_D s^2 + K_p s + K_I}{s} \quad (44)$$

where  $K_p$  is the proportional gain,  $K_I = K_p/T_I$  is the integral gain, and  $K_D = K_p T_D$  is the derivative gain of the controller. Pole – zero cancellation technique is the most suitable one to remove unstable poles in the transfer function. In order to use pole – zero cancellation technique, the analog PID controller equation can be re-written in the form as:

$$G(s) = \frac{K_D \left( S^2 + \frac{K_p}{K_d} s + \frac{K_i}{K_d} \right)}{s} \tag{45}$$

This form is easy to determine the closed loop transfer function.

$$H(s) = \frac{1}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{46}$$

$$\frac{K_i}{K_d} = \omega_o^2 \tag{47}$$

$$\frac{K_p}{K_d} = 2\xi\omega_o \tag{48}$$

Then

$$G(s) H(s) = \frac{K_d}{s} \tag{49}$$

Where  $\xi$  the damping ratio and  $\omega_o$  is is the natural frequency of oscillation of the system. The DF buck converter under consideration is of third order and the desired poles can be easily placed by assuming the following converter specifications,

$$\text{Settling time} \approx \frac{4}{\xi\omega_o} \leq 1ms \tag{50}$$

$$\text{Max. Peak Overshoot} \approx 100e^{-\xi\pi\sqrt{1-\xi^2}} \leq 1\% \tag{51}$$

For the system to be stable, the closed – loop poles or roots of the characteristic equation must lie within the unit circle. The  $K_p$ ,  $K_I$  and  $K_D$  values are satisfying the above the condition then the poles and zeros of the function should be placed within the unit circle and the system is said to be in stable condition.

By following the above equation and conditions, the value of  $K_p = 0.09$ ,  $K_I = 189$  and  $K_D = 6.6528 \times 10^{-6}$ ,  $\omega_o = 5331$  rad/sec and  $\xi = 0.9$ . Then the analog PID controller equation is

$$U(s) = \frac{V_o(s)}{d(s)} = \frac{6.6528 \times 10^{-6} (s^2 + 13528s + 28409)}{s} \tag{52}$$

The continuous-time domain controller of (52) is transformed into the discrete-time domain using Trapezoidal method is called as Tustin method or Bilinear – Transformation method. This Tustin method tracks the analog controller output more accurately at the sample times and approximate to the analog integration are better than

other methods. Let us discuss Trapezoidal approximation method now.

Let  $n(t)$  be the integral of  $e(t)$ , then the value of the integral of  $t = (K + 1)T$  is equal to the value at  $KT$  plus the area added from  $KT$  to  $(K + 1)T$ .

$$N[(K + 1)T] = u(KT) + \int_{KT}^{(K+1)T} e(\tau) d \tag{53}$$

Using Trapezoidal rule,  $e(t)$  is the area curve from  $t = KT$  to  $t = (K + 1)T$  is approximated as

$$\frac{e[(K + 1)T] + e(KT)}{2} x T \tag{54}$$

Therefore

$$N\{(K + 1)T = n(KT) + \frac{T}{2} \{e[(K + 1)T] + e(KT)\} \tag{55}$$

Taking the z-transform of (55) then

$$zN(z) = N(z) + \frac{1}{2} [zE(z) + E(z)] \tag{56}$$

Thus

$$\frac{N(z)}{E(z)} = \frac{T}{2} \left[ \frac{z + 1}{z - 1} \right] \tag{57}$$

Hence equation (57) is the transfer function of a discrete Integrator. Trapezoidal approximation to differentiation. Derivative of  $e(t)$  at  $t = KT$  is  $n(KT)$ , then

$$n(KT) \cong \frac{e(KT) - e[(K - 1)T]}{T} \tag{58}$$

Taking z – transform of (58). Thus

$$\frac{N(z)}{E(z)} = \frac{(z - 1)}{Tz} \tag{59}$$

The discrete PID controller block diagram is shown in Figure.10. Now discrete PID controller transfer function be-

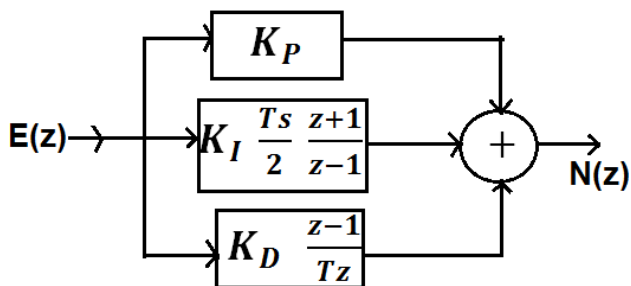


Fig. 10. Discrete PID Controller

comes

$$G(z) = \frac{U(z)}{E(z)} = \left[ K_p + K_I \frac{T_s}{2} \frac{z + 1}{z - 1} + K_D \frac{z - 1}{Tz} \right] \tag{60}$$



Table 3. Performance parameters of the closed loop DF buck converter

Controller	Settling Time (ms)	Peak Over-shoot (%)	Rise Time (ms)	Steady State Error (V)	Output Ripple Voltage (V)
Discrete PID	8	0	6	0.001	0
Discrete PI	10	10	2	0.02	Less
Analog PID	18	0	18	0.01	More
Analog PI	20	0	20	0.03	More

$$U(z) = \left[ \frac{(K_P + K_I \frac{T_s}{2} + \frac{2K_d}{T_s})z^2 + (K_I T_s + \frac{4K_D}{T_s})}{z(z-1)} \right] E(z) \quad (61)$$

In the designed DF buck converter the discrete PID controller equation becomes

$$U(z) = \frac{V_o(z)}{d(z)} = \frac{(z - 0.9929)(z - 0.9928)}{z(z - 1)} \quad (62)$$

The response of the discrete PID controller in DF buck converter is explained below.

## 8 SIMULATION RESULTS

The proposed closed loop response of the DF buck converter is simulated using MATLAB / SIMULINK is shown in Figure 11. Simulation has been carried out using the values same as that of the experimental values. The aim of this paper is to achieve robust controller in spite of variations in load and uncertainty. Table 3 shows the performance of the various controllers using the same DF buck converter. The table shows that the output voltage obtained using digital controller settles down at 0.008 S with a rise time of 0.006 S. The controller specifications under considerations are settling time, Peak overshoot, rise time, steady state error and output ripple voltage are shown compared against its Discrete PI and analog PI & PID controllers are designed for the same DF buck converter.

Steady state error observed for load variations is much lesser than 2% and no overshoot or undershoots are evident. The performance specifications for the DF buck converter with discrete PID controller are better than with PI and analog controller. The results are thus obtained with digital controller for DF buck converter is in concurrence with the mathematical calculations. It is proved that the digital system shows improved results than the analog controller.

The simulation is carried out by varying the input voltage, load resistance and the corresponding output voltage, output current, current through inner cell inductor and

Table 4. Output response with variable DF buck converter parameters

$L_l$ (mH)	$L_h$ ( $\mu$ H)	$C$ ( $\mu$ F)	$R$ ( $\Omega$ )	Reference voltage ( $V_{ref}$ )	Output Voltage ( $V_o$ )
0.8	100	470	4	10	10.005
0.8	75	470	4	10	10.005
0.8	75	400	4	10	10.004
1.5	150	500	8	10	10.015
0.6	80	450	2	10	10.002

outer cell inductor are shown in Figure 12 respectively. The input voltage is first set as 48 V until 0.01 S and then varied from 48 V to 44 V and again at 0.02 S, 44 V is varied to 48 V. 48 V is changed to 52 V at 0.03 S and finally 48 V is set at 0.04 S. Similarly the load resistance is first set as 6 $\Omega$  until 0.015 S and then varied from 6 $\Omega$  to 4 $\Omega$  and again at 0.03 S, 4 $\Omega$  is varied to 2 $\Omega$  and finally 4 $\Omega$  is set at 0.04 S. The corresponding output response of the double frequency buck converter shows fixed output voltage regulation. Undershoots or overshoots are not seen and the steady state error is also not apparent. The load current, outer cell inductor current and inner cell inductor current are also shown in Figure 12. In order to check the dynamic performance of the controller, the  $L_h$ ,  $L_l$ ,  $C$  and  $R$  values are varied and the output response of the system is shown in Table 4.

Table 4 proves that the system is very much dynamic in tracking the reference voltages in spite of the variations in the inductance  $L_l$  and  $L_h$ , capacitance  $C$  and Load resistance  $R$  values. The system does not show any steady state error, overshoots or undershoots and it settles down fast with a settling time of about 0.009 S for all the values. In order to confirm the better performance of Discrete controller over its analog counter parts, the output response of the DF buck converter is compared against the response produced by an analog controller and its graph is shown in Figure.13. Here both analog and discrete controller for DF buck converter is activated by  $V_s = 48$  V,  $V_{ref} = 10$  V and the corresponding output voltage response are shown below. From the output waveforms, one can understand that the discrete PID controller has less rise time and settling than analog PID controller. In analog PID controller, filter is used to get such kind of response, whereas in discrete controller filter is not required.

## 9 HARDWARE IMPLEMENTATION

### 9.1 LabVIEW package

The DF buck converter with discrete controller has been implemented using LabVIEW as a controller platform. LabVIEW (Laboratory Virtual Instrumentation Engineering Work Bench) is a system design platform and

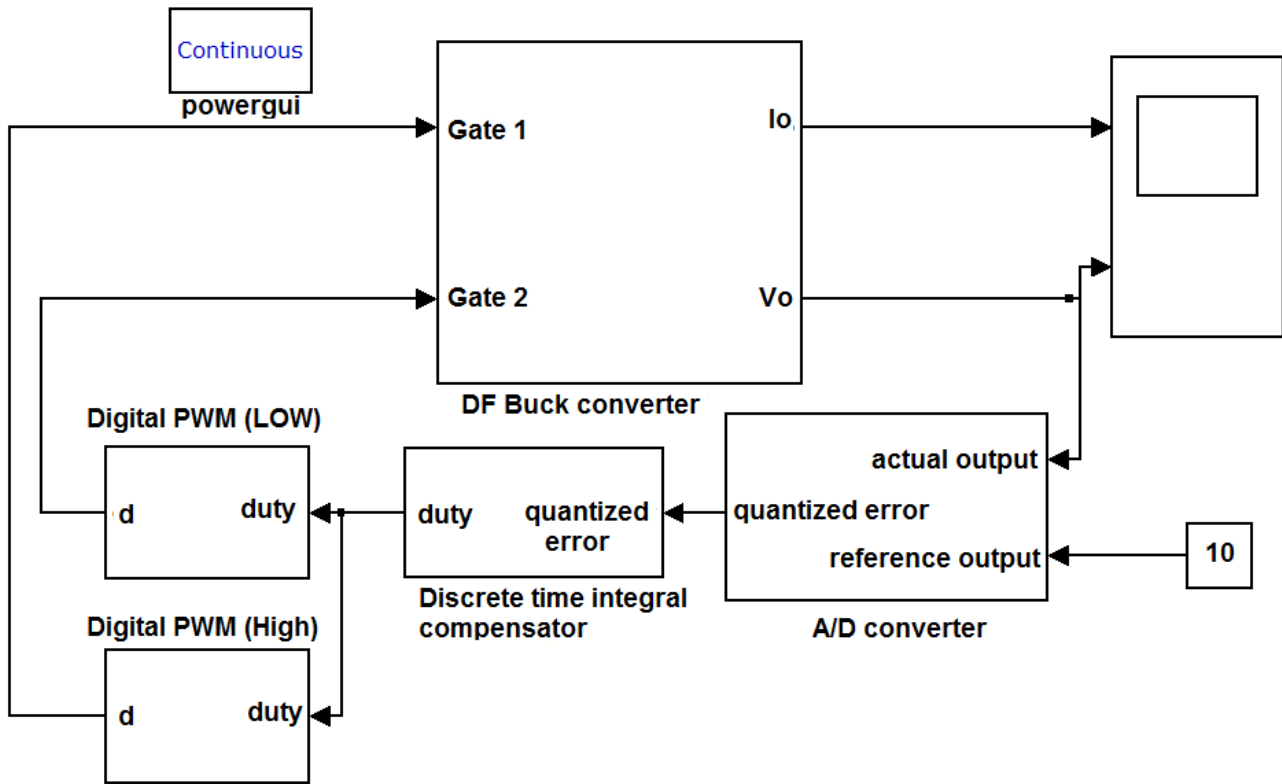


Fig. 11. Matlab diagram for discrete controller based feedback control of DF buck converter

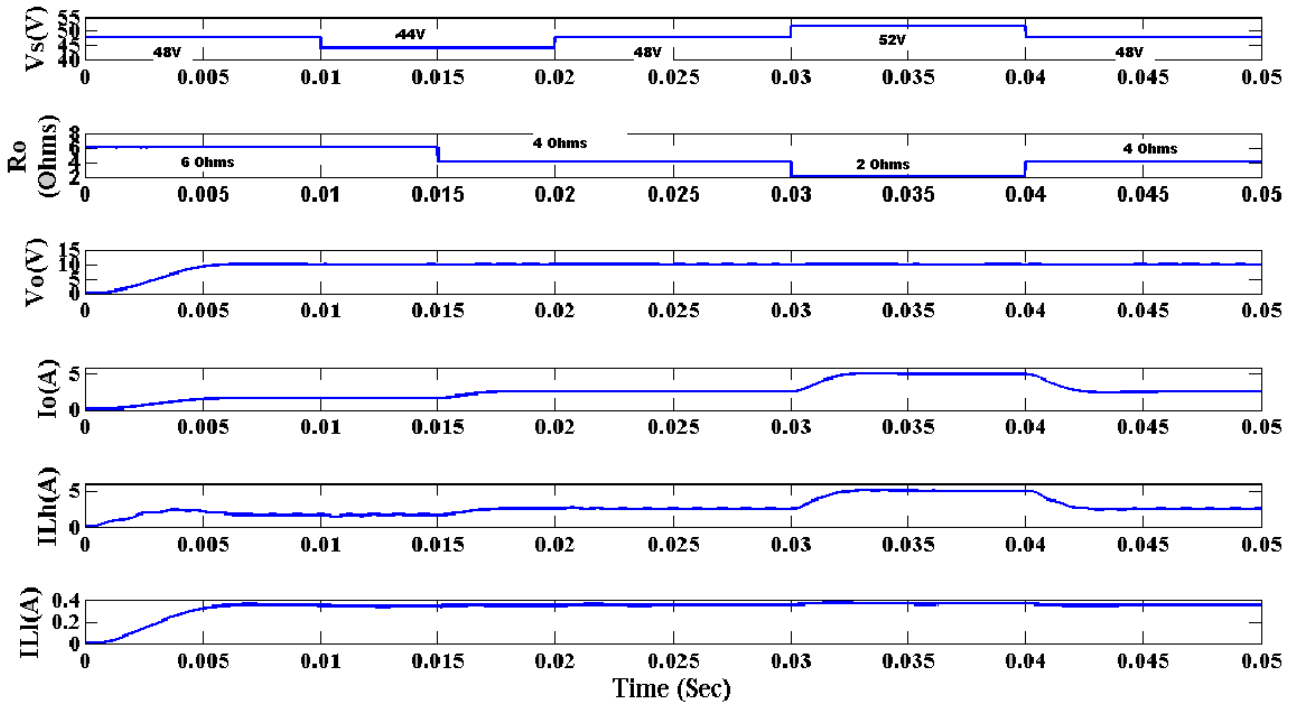


Fig. 12. Output response of the DF buck converter ( $V_s$  – Input voltage,  $R_o$  – Load resistance,  $V_o$  – Output voltage,  $I_o$  – Output current,  $I_{Lh}$  – Outer cell inductor current,  $I_{Ll}$  – Inner cell inductor current)

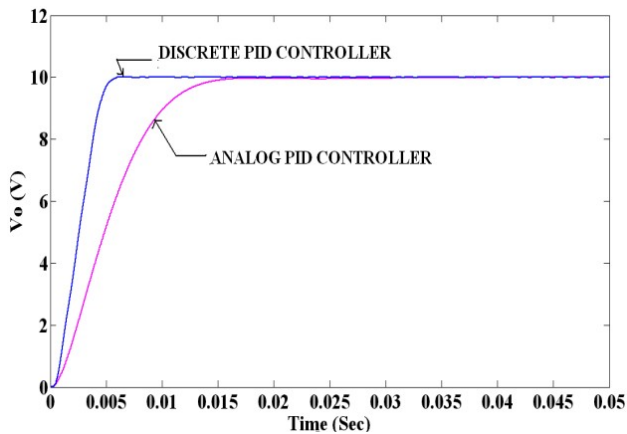


Fig. 13. Comparison between Digital and Analog PID controller responses

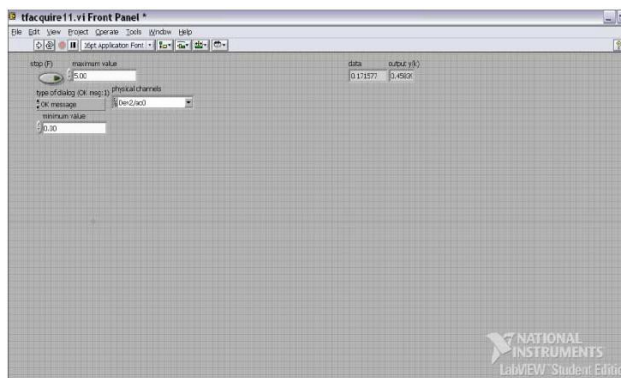


Fig. 14. Front panel

development environment for a visual programming language from National Instruments. LabVIEW programs are called virtual instruments (Vis). This has three main parts: the block diagram, the front panel, and the icon/connector. Vi's have an interactive user interface – known as the front panel – and the source code – represented in graphical form on the block diagram. The front panel is the interactive user interface of a VI – a window through which the user interacts with the source code. The front panel opens through which we pass inputs to the executing program and receive outputs when we run a VI. The front panel is necessary for viewing the program outputs [11].

The control circuit associated with the front panel is shown in Figure 14. The block diagram consists of executable icons (called nodes) connected (or wired) together. The block diagram is the source code for the VI. Figure.15 is mainly used for user interactions. It is through the front panel the desired transfer function of the discrete controller is entered and the corresponding parameters of the controlled process and hence the updated status of the system

Table 5. Experimental values

Description	Experimental values
$f_h$	100 KHZ
$f_l$	10 KHZ
$V_s$	48 V
$L_l$	1 mH
$L_h$	100 $\mu$ H
$C$	470 $\mu$ F
$R$	4 $\Omega$
$S_l, S_h, D_h$	IRF840
$D_l$	1N4001
DAQ	NI 9221

is obtained. The block diagram, data acquisition, transfer function and signal generation are built using the functional block diagram as shown in Figure. 15. The analog output voltage from the external circuit is acquired by Data Acquisition card and it gets converted into discrete PID controller H(z) block. Since this type of DAQ card supports a maximum sampling rate of about 48 k samples/sec, such low frequency is assumed.

## 9.2 Interfacing circuit

The NI 9221 with screw terminal has a 63-terminal, detachable connector. The NI 9221 with DSUB has a 25-pin DSUB connector. Each channel has an AI (Analog Input) terminal or pin to which we can connect a voltage signal. The NI DAQ 9221 multifunction data acquisition (DAQ) devices provide plug and play connectivity via USB for acquiring, generating and data logging in a variety of portable applications. It comprises of 8 analog inputs with referenced single ended signal coupling or 4 inputs with differential coupling, 2 analog outputs, 12 bits A/D and D/A converters and 32 bits counters. There are 12 channels of digital Input/output lines which can be used either as input or output. It eventually provides an excellent platform for the proposed discrete PID controller.

The prototype model of the Double Frequency Buck converter with discrete PID controller is shown in Figure 16. It is obviously understood that the Discrete controller works well and the LabVIEW provides the most feasible solution for the controller platform. To evaluate the performance, the reference value of 10 V is set for which the output is obtained as 10.01 V. The steady state error thus observed is very minimum of the order of 0.01 V and the system settles down fast. The acquisition of the error signal from the hardware takes place instantaneous, when the program is run and at the same time the controlled signal from the LabVIEW package is also generated within a very shorter duration of time without any delay or time lag. The experimental results thus obtained are in concurrence with

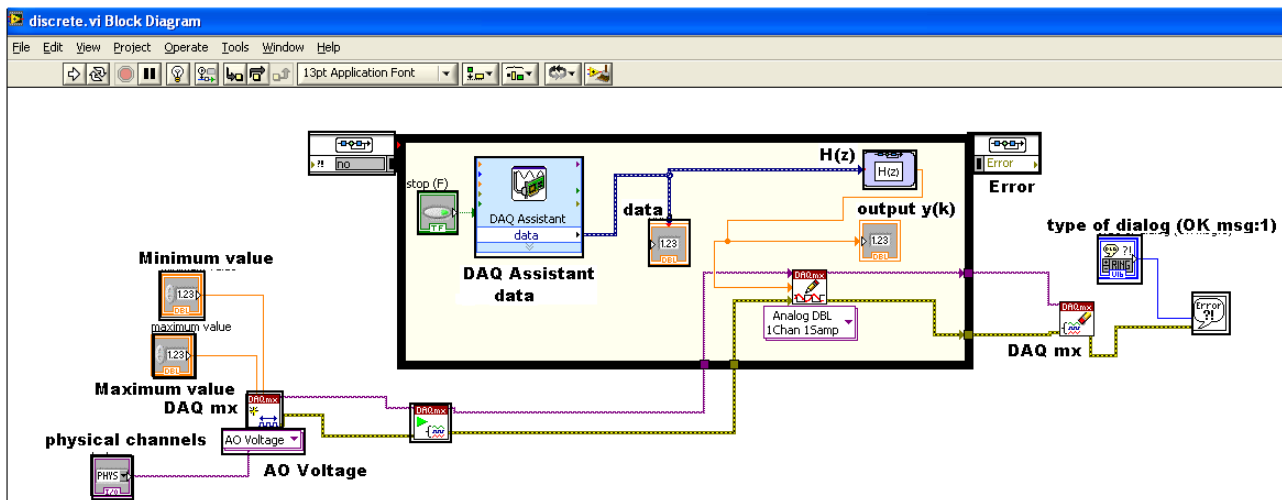


Fig. 15. Functional block diagram

the simulation results and mathematical calculations. Prototype model is developed using the values shown in Table 5.

The input voltage has been varied as 44 V, 48 V and 52 V and the corresponding output voltage is measured as 10.01 V, 10.0 V and 10.03 V respectively for the reference of 10 V and it is illustrated as shown in Figures 17, 18 and 19 respectively. In these figures channel 1 indicate the input voltage such as 44.06 V, 48.03 V and 52.05 V respectively and Channel 2 indicates the corresponding output voltages. The results prove that there are no undershoots or overshoots and steady state error is of very minimum order. Similarly the output voltages for the references of 10 V & 15 V along with their switching pulses are shown in Figure 20 and 21 respectively. From the output waveforms, one can be very well understood that the output thus observed shows better performance thereby providing that the controller is more enough to track the references in spite of the change in input voltage.

## 10 CONCLUSION

In this paper, discrete controller for double frequency buck converter has been presented. Simulation results are demonstrated that the DF buck converter not only exhibits the steady state and transient performance but also improves the efficiency of conventional buck converters. The design of time domain based discrete PID controller for DF buck converter whose duty cycle varies with the variations in the error signal and the implementation includes an ADC and discrete pulse width modulator. The discrete controller is thus designed for the DF Buck converter is implemented using LabVIEW as a control platform and the results are illustrated. The mathematical analysis, simulation study and the experimental results show that the

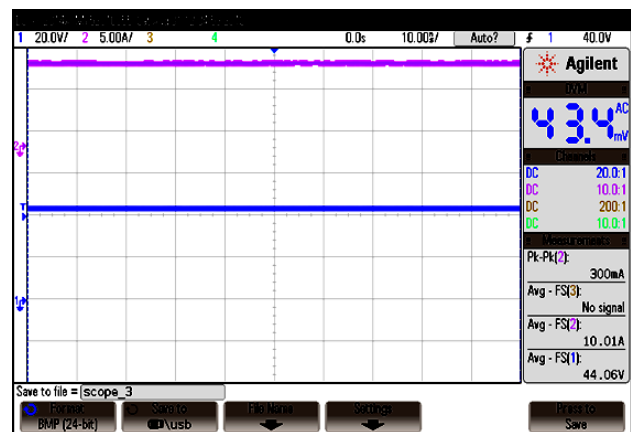


Fig. 17. Output Voltage obtained for 44V input

controller thus designed achieves tight output voltage regulation, good dynamic performances and higher efficiency. This topology is independent and also can be extended for any of the applications such as speed control, photo voltaic cell and medical electronics.

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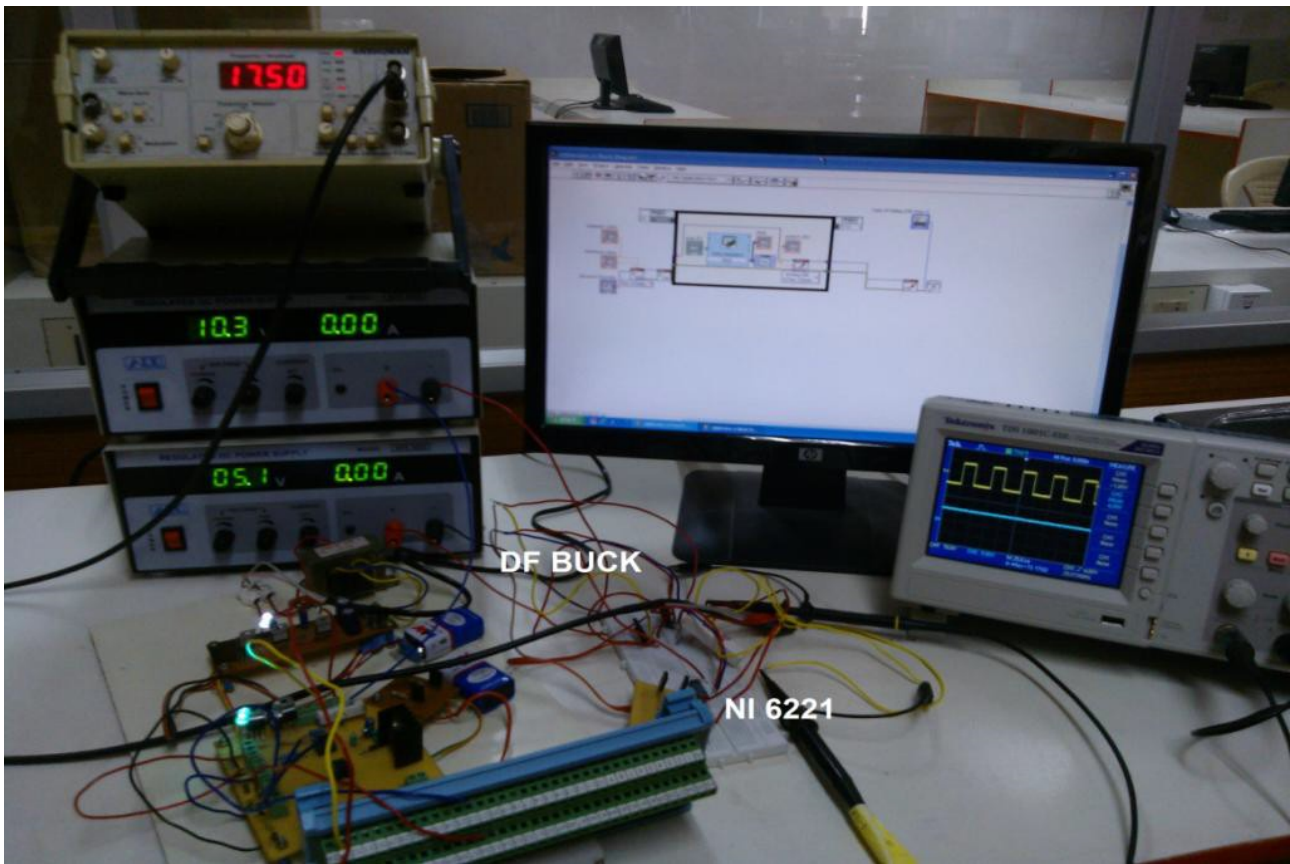


Fig. 16. Experimental set up

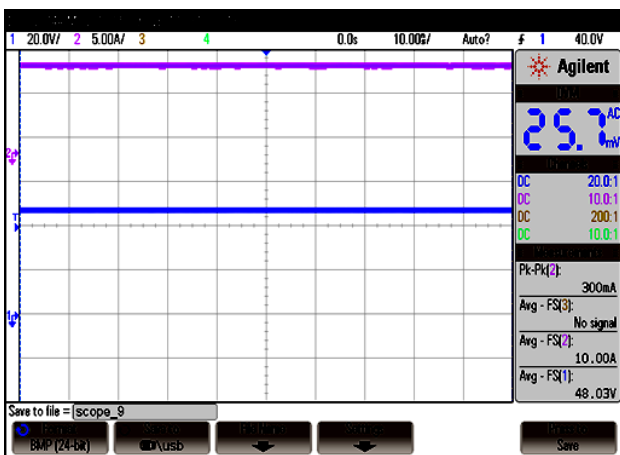


Fig. 18. Output voltage obtained for 48V input

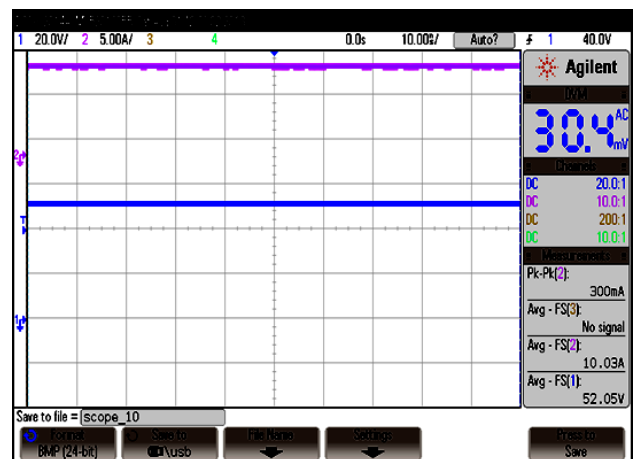


Fig. 19. output voltage obtained for 52V input

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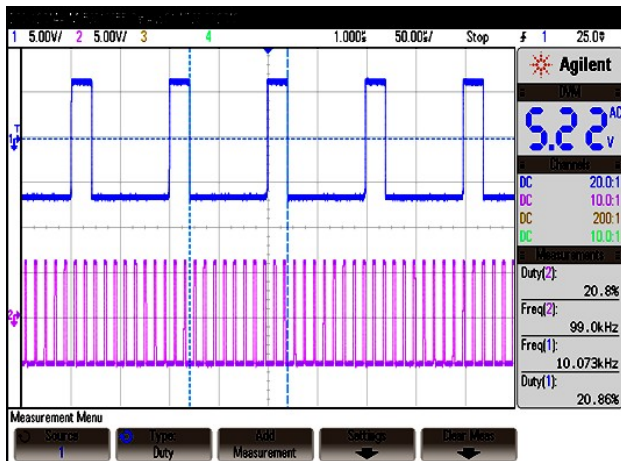


Fig. 20. Duty Cycle Obtained for 10V reference

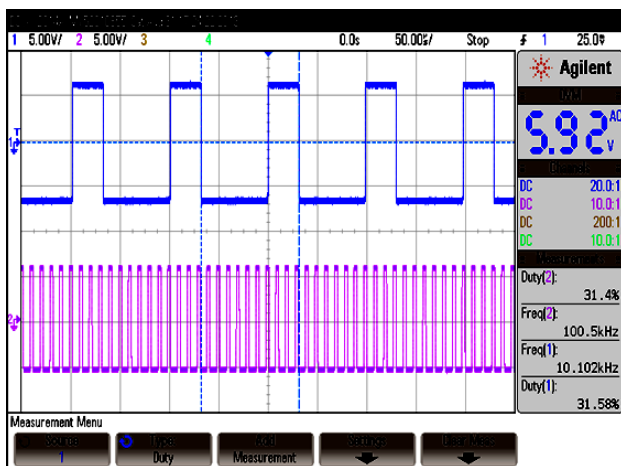


Fig. 21. Duty Cycle obtained for 15V reference

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**Subramanian Vijayalakshmi** received AMIE degree in Electronics & Communication Engineering from Institution of Engineers (India), Kolkatta in 1992, Master of Science degree in Information Technology from Bharathidasan University, Tiruchirapalli, and Master of degree in Power Electronics and drives from Anna University, Chennai in 2007 and Ph.D from Anna University, Chennai in 2015. Her research interests are Discrete controller for DC-DC converters and renewable energy.



**Thangasamy Sree Renga Raja** is working as an Assistant Professor in the Department of Electrical and Electronics Engineering, Anna University, BIT Campus, Tiruchirapalli, Tamil Nadu, India. He obtained B.E (Electrical and Electronics Engineering) degree from Manonmaniam Sundaranar University, Tirunelveli in 1998, M. E (Power Systems) from Annamalai University, Chidambaram in 1999 and Ph.D from Anna University, Chennai in 2007. He has published many papers in the field of Power System Engineering. His area of interest includes Power system optimization, Renewable Energy Applications, Energy Conservation Management and Insulation Engineering.

**AUTHORS' ADDRESSES**

**Asst.Prof. Subramanian Vijayalakshmi, Ph. D.**  
**Department of Electrical and Electronics Engineering,**  
**Saranathan College of Engineering,**  
**Panchapur, Tiruchirappalli 600 012, India,**  
**email: bksviji@gmail.com**

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**Asst. Prof. Thangasamy Sree Renga Raja, Ph.D.**  
**Department of Electrical and Electronics Engineering,**  
**Anna University, BIT Campus,**  
**Tiruchirappalli, Tamil Nadu 600024, India,**  
**email: renga\_raj@rediffmail.com**