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Design of low-power voltage/current references and supply voltage for 9-bit fully differential ADC

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This paper presents the design of a low-power voltage reference, bias current and the supply voltage for a 9-bit fully differential ADC. The references, power supply circuits and the ADC are integrated in one circuit, i.e. chip. The proposed chip is implemented in the UMC 0.18 μm CMOS process and occupies 800×700 μm^2. The circuit supply voltage VDD is obtained from the external RF signal. When the circuit is active VDD is used as a supply for the rest of the circuitry. The circuit generates supply, reference voltages and currents when VDD exceeds the upper voltage level V_{HIGH} ≈1.82 V. When VDD is lower than the lower voltage level V_{LOW} ≈1.35 V, the circuit is off. When the circuit is active, the current consumption is 22 μA. The presented results are based on measurements.

Key words: Low-power, voltage references, current references, voltage regulator, analogue-to-digital converter

Projektiranje izvora stabilnog napona/struje i napona napajanja niske potrošnje za 9-bitovni AD pretvornik sa simetričnim ulazima. U ovom radu opisano je projektiranje izvora stabilnog napona, stabilnih struja i napona napajanja za 9-bitovni AD pretvornik sa simetričnim ulazima. Izvori stabilnih napona, struja i AD pretvornik integrirani su u jedan čip. Opisani čip je projektiran u 0,18 μm CMOS procesu tvrtke UMC i zauzima 800×700 μm^2. Napon napajanja čipa VDD je dobiven iz vanjskog RF signala. Kad je čip aktivan VDD se koristi kao napajanje za ostale dijelove čipa. Stabilni napon, struja i napon napajanja uključuju se kad VDD prijeđe gornju naponsku granicu V_{HIGH} ≈1.82 V. Kada je VDD niži od donje naponske razine V_{LOW} ≈1.35 V, čip je isključen. Kad je čip uključen, potrošnja struje je 22 μA. Rezultati predstavljeni u ovom radu temelje se na mjerenjima.

Ključne riječi: Niska potrošnja, izvor stabilnog napona, izvor stabilne struje, naponski regulator, analogno-digitalni pretvornik

1 INTRODUCTION

Integration of radio frequency identification (RFID) systems with sensors has potential usage in infrastructure and object monitoring, identification of harmful agents and implantable biomedical devices [1]. Also, wirelessly powered healthcare sensors enable continuous health monitoring [2, 3]. In such systems available power is limited because the energy is very often extracted from environment and used to supply chip (tag). One way of energy harvesting is harvesting from electromagnetic waves.

The key component in intelligent RFID systems is an analogue-to-digital converter (ADC) because it has to provide high resolution and low-power consumption [1]. The designers of such ADCs are focused on lowering power consumption and increasing the ADC speed. The examples of a low-power ADCs are presented in [1–9]. Very often generation and stability of the reference voltages for ADCs is an equally challenging task because classic bandgap voltage references are not used in the tags because of low supply voltage of the tags. The papers [1,6] present ADCs but without the reference and supply voltage, while the papers [2, 3] present the whole chip with on-chip voltage references, but it is not clear how the references are designed. This paper focuses on the design of supply voltage and fully differential reference voltages (presented in [10]) for the fully differential 9-bit ADC implemented in 0.18 μ CMOS process. The ADC is presented in [11].

2 SYSTEM DESCRIPTION

Fig. 1 shows the block diagram of the proposed chip. The ADC voltage reference, bias current and the supply voltage from regulators are generated for the 9-bit ADC. The powering strategy, which reduces required input power, is adopted from [12].

The RF/DC converter converts harvested RF energy to DC voltage VDD. The charge needed to produce the

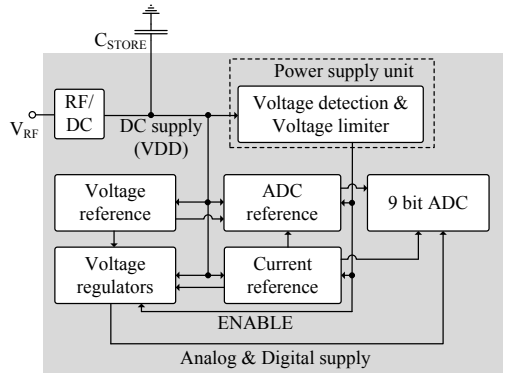


Fig. 1. Block schematic of implemented solution.

voltage VDD is stored in the external capacitor C_{STORE} and when the proposed circuit is active, VDD is used as a supply for the ADC voltage reference circuit, bias current circuit and the voltage regulators. When VDD is low, only voltage references are enabled so that the proposed circuit consumes the minimum power. When VDD exceeds targeted upper voltage limit V_{HIGH}, the voltage detection unit will enable the rest of the circuitry (the circuit is active). When the circuit is active, the harvested energy stored in the capacitor is decreasing as the capacitor is discharging, which reduces the supply voltage.

At the low voltage limit V_{LOW} the voltage detection circuit will turn off the circuitry so power consumption is minimum and the supply voltage will rise again. V_{HIGH} is the maximum allowed supply voltage in given technology and V_{LOW} is the minimum supply voltage of the ADC. The proposed circuit operates in the voltage range $V_{HIGH} - V_{LOW}$ and the system has to be insensitive to supply voltage variations. The value of the capacitor C_{STRORE} can be calculated as

$$C_{STORE} = \frac{I_{act} \cdot t_{act}}{V_{HIGH} - V_{LOW}} \tag{1}$$

where I_{act} is the current consumption of the circuit and t_{act} is the time window in which the circuit is enabled. The duration of t_{act} depends on the ADC conversion time and settling time of the circuitry, especially ADC references.

2.1 Voltage detection and voltage limiter

Fig. 2 shows the voltage reference circuit, the voltage detection and voltage limiter circuit presented in [12]. A low-power voltage and temperature compensated voltage reference is presented in [13]. The circuit in Fig. 2 generates two 485 mV reference voltages which are insensitive to voltage and temperature variations. One is for the ADC ($VADC_{REF}$) and the other is for the voltage detector, voltage limiter and for voltage regulators (VDD_{REF}). The reference generation for the ADC and for the supply is separated in order to avoid possible propagation of interferences generated by the voltage regulators. Also the 2 pF capacitor is added to VDD_{REF}. The expression for the reference voltage is given in [13]

$$VADC_{REF} = V_{th} + \left[\frac{1}{\sqrt{k_8}}\left(\sqrt{\frac{W_5/L_5}{W_7/L_7}}\right) - \frac{1}{\sqrt{k_6}}\right]\sqrt{2I_0} \tag{2}$$

$$I_0 = \frac{m^2 V_T^2 k_2}{2}\left(\frac{N}{N-1}\right)^2 \ln^2\left(\frac{W_4/L_4}{W_3/L_3}\right) \tag{3}$$

where $N = \sqrt{k_1/k_2}, (k = k_n' W/L)$, k_n' is the nMOS transconductance parameter in saturation, V_{th} is the threshold voltage of the nMOS transistor, V_T is the thermal voltage and *m* is the subthreshold swing parameter. The stability of the reference voltage depends on process parameters (2) and it was checked by Monte Carlo mismatch analysis. The mean value of the reference voltage is 485.8 mV and the standard deviation is σ = 7 mV. The mean temperature coefficient (TC) is 7 ppm/°C and the standard deviation is σ_{TC} = 30 ppm/°C. The temperature coefficient is calculated in the range from -10 °C to 70 °C. Fig. 3 presents the simulated stability of the reference voltage as a function of temperature.

Due to the parasitic gate-source capacitance C_{par} of the transistors M_{p1} and M_{p2} a part of the voltage VDD will be coupled to the reference voltages $VADC_{REF}$ and VDD_{REF}. When the voltage VDD rises or decreases, it causes the parasitic current I_0' through the parasitic capacitance. The additional parasitic current I_0' will be added to the current I_0 causing error in the voltages $VADC_{REF}$ and VDD_{REF}. The parasitic current $I_0' = C_{par}(\Delta VDD/\Delta t)$ is proportional to the slope $(\Delta VDD/\Delta t)$. The slope $(\Delta VDD/\Delta t)$ depends on the charging capacitor C_{STORE}, i.e. the slope is lower if C_{STORE} is larger. Since the current I_0 is in the order of 40 nA even small parasitic capacitance will cause the parasitic current I_0' of few nA, which means that the only way to reduce I_0' is to have low $(\Delta VDD/\Delta t)$.

The voltage detector is a low-power comparator with the hysteresis. Since the power consumption must be low, four pMOS transistors are used as a voltage divider instead of using large resistors. The transistors bulk and source terminals are shorted and each transistor has the same threshold voltage (i.e. same characteristics) and they can be considered as resistor with equal resistance. When VDD exceeds the level V_{HIGH}=4·VDD_{REF}= 1.94 V (1.94 V is obtained from simulations), the comparator digital output ENB is set low. This signal enables the rest of

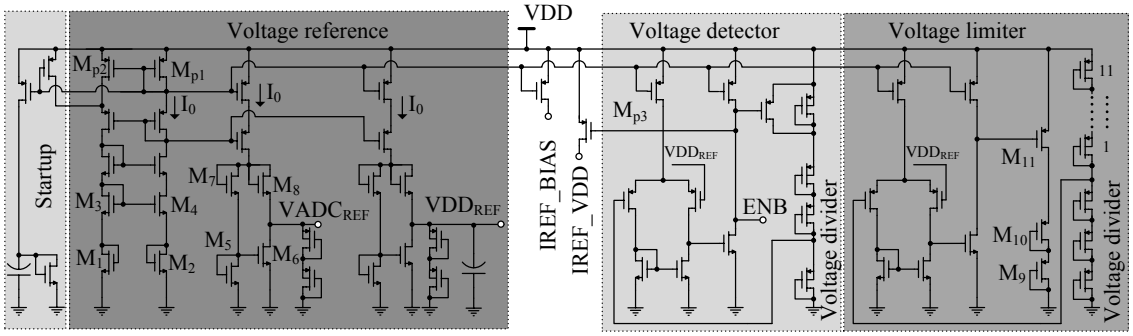


Fig. 2. Schematic of the voltage reference, voltage detection and voltage limiter.

the circuitry and the supply voltage $IREF\_VDD$ for the current references; and C_{STORE} discharges and the voltage VDD decreases. When the voltage reaches the level V_{LOW}=3·VDD_{REF}= 1.455 V (1.455 V is obtained from simulations), ENB is set high and the circuit is turned off; and C_{STORE} voltage rises. When VDD is in the range 1.455 V to 1.94 V, the circuit is active and the voltage hysteresis is 485 mV.

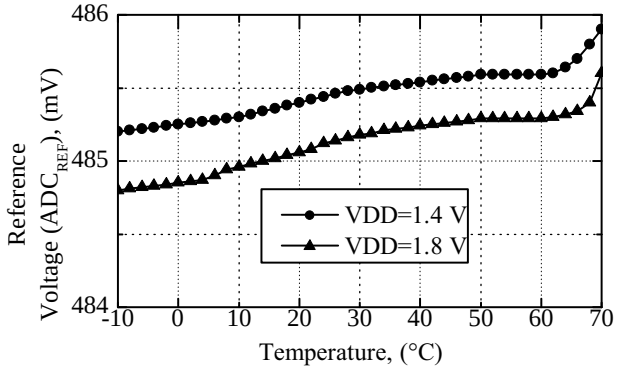


Fig. 3. Simulated stability of the reference voltage over temperature simulated in Spectre.

The voltage limiter detects if VDD exceeds the breakdown voltage (2.2 V). When the voltage is too high, the limiter will quickly turn on the transistor M_{11} and pull large current which will discharge the capacitor C_{STORE} and decrease VDD. In order to prevent a short circuit VDD – ground, two pMOS-based resistors are added (M_9 and M_{10}).

The consumption of the circuit from Fig. 2 must be as low as possible. The simulated overall current consumption in the voltage range from 1.4 V to 2 V is 60 nA in a typical case. The voltage reference circuit consumes 41 nA while the voltage detection and voltage limiter consumes 12 nA and 7 nA respectively. The worst case consumption is 100 nA (fast corner, 70 °C).

As very low current flows (15 nA) into the transistors $M_5 - M_8$ and the parasitic capacitances of the transistor gates are large, the reference voltages reaches 485 mV very slowly; the settling time is ≈500 µs. On the other hand $VADC_{REF}$ must be stable before the comparator enables the circuitry. This can be achieved if $VADC_{REF}$ is generated at the same time as VDD_{REF}. When the circuit is enabled (ENB is low), $VADC_{REF}$ has already settled at 485 mV.

2.2 Current references

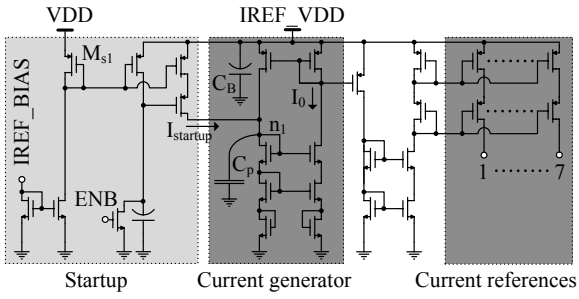


Fig. 4. Current references.

Fig. 4 shows the current reference circuit. The circuit is designed to generate six current references of ∼100 nA for the voltage regulators and for the ADC references and one reference current of ∼150 nA for the ADC ($IREF\_ADC$). The current I_0 can be calculated by using (3). The simulated overall current consumption of the circuit is 1.2 µA. The stability of the reference current over temperature and voltage variations is not crucial because the generated currents are used as the reference currents for the operational amplifiers used in the proposed circuit. It is only important that these currents are as low as possible

due to the power consumption restriction. The simulated current variations over temperature and voltage variations are shown in Fig. 5.

In order to minimize the current consumption the reference supply voltage $IREF\_VDD$ is disconnected from the supply voltage VDD and the circuit is turned off when ENB is high because the start-up circuit is disabled i.e. the transistor M_{p3} from Fig. 2 is off. After ENB is set low, $IREF\_VDD$ is connected to the voltage VDD (i.e. $IREF\_VDD = VDD$). The start-up circuit is modified to ensure fast turn on. The parasitic capacitance C_p slows down the start-up process because it takes time to charge the capacitance. Therefore, the current $I_{startup}$ charges the parasitic capacitance C_p before the current reference circuit is enabled. $I_{startup}$ is the mirrored current $IREF\_BIAS$ which is generated by the voltage reference circuit. The transistor M_{S3} is always on because it is connected to VDD and the current $I_{startup}$ will charge C_p before the current reference circuit is enabled.

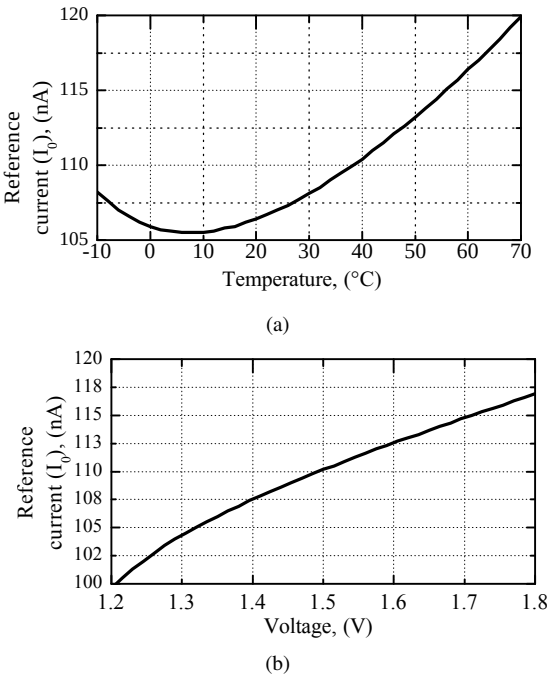


Fig. 5. Reference current variations as a function of temperature and supply voltage obtained by simulations in Spectre. (a) Reference current variation as a function of temperature, (b) Reference current variation as a function of the supply voltage $IREF\_VDD$.

2.3 ADC references

The ADC reference circuit is shown in Fig. 6. The input voltage $VADC_{REF}$ from the voltage reference subcircuit (Fig. 2) is sampled on the capacitor C_{SH}= 4.5 pF in

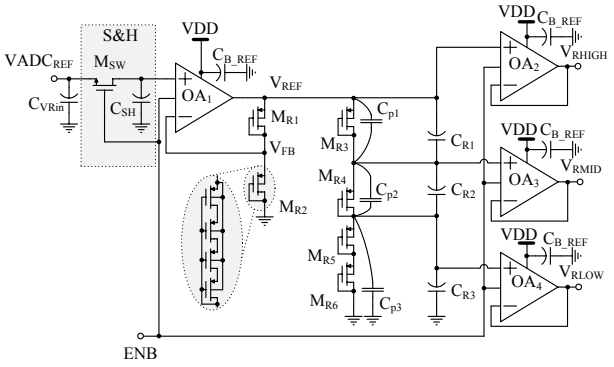


Fig. 6. ADC reference circuit.

order to avoid the issues related with the parasitic current I_0' which are described in Section 2.1. The capacitor value is large due to charge injection of the transistor M_{SW}. The capacitor C_{VRin}=2 pF is used for filtering any interference which might occur. The outputs are three voltages V_{RHIGH}, V_{RMID} and V_{RLOW}. Three voltages are necessary because the ADC is fully differential. V_{RHIGH} and V_{RLOW} are high and low voltage references while V_{RMID} is the common-mode voltage. The voltage $VADC_{REF}$ is first amplified two times to obtain the voltage V_{REF} = 970 mV. V_{REF} is divided and then three reference voltages are generated. To reduce current consumption the feedback resistors M_{R1} and M_{R2} should be large. The area is reduced by using the pMOS transistors M_{R1} and M_{R2} instead of resistors. In order to enable good matching both transistors, M_{R1} and M_{R2}, are implemented as four segments, i.e. as four transistors connected in series with the gates tied together as in Fig. 6. Each segment has a (W/L)=1µm/2µm and the overall (W/L) ratio of the transistors M_{R1} and M_{R2} is 1µm/8µm. The source and bulk terminals of the transistors M_{R1} and M_{R2} are shorted so the transistors have the same threshold voltage and resistance R_{DSon}. According to [14] the voltage V_{REF} is

$$V_{REF} = VREF_{ADC}\left(1 + \frac{m}{n}\right) \tag{4}$$

where m is the number of transistors between the nodes V_{REF} and V_{FB} and n is the number of transistors between the nodes V_{FB} and ground. Since m=n=1 (M_{R1}=M_{R2}) the voltage V_{REF}= 970 mV.

The high reference voltage V_{RHIGH} = V_{REF}= 970 mV. The transistors $M_{R3} - M_{R6}$ are the resistive divider used to generate the low reference voltage V_{RLOW} and the common-mode voltage V_{RMID}. The (W/L) ratio of $M_{R3} - M_{R6}$ is 4µm/1µm and to ensure good matching the transistors consist of parallel units. Because the transistors $M_{R3} - M_{R6}$ have the same size V_{RLOW}= 485 mV and $V_{RMID} \approx$ 730 mV. For

better matching the transistors consist of multiple devices. The capacitors C_{R1}, C_{R2} and C_{R3} are the blocking capacitors. Their task is to filter any interference which could couple from the power supply VDD. Also, the buffers $OA_2 - OA_4$ prevents switching noise from the ADC during AD conversion.

The power consumption of the circuit is crucial. In order to reduce power consumption, the operational amplifiers $OA_1 - OA_4$ are directly connected to VDD without voltage regulators. This means that the amplifiers must have good power supply rejection ratio (PSRR). The decoupling capacitors are connected to VDD to improve PSRR.

Besides PSRR the reference buffers $OA_2 - OA_4$ also must be capable driving capacitive loads since the ADC inputs are purely capacitive loads. Because the ADC has 9-bit resolution the buffers open-loop gain is A_{V0} = 60 dB. With 60 dB open-loop gain the voltage error at the output of the buffers is less than 1/2 of differential nonlinearity (DNL) for the ADC, e.g. $V_{RHIGH} - V_{REF} \approx$0.95 mV. During the AD conversion for each bit the buffers must charge or discharge the ADC input capacitors (the DAC capacitors) very fast and the reference voltages must settle before the conversion of the next bit starts. The settling time accuracy S is defined as $S = 2^{-b}$ where b is the number of bits [15]. Under the assumption that the buffers are modelled as a single-pole system the unity-gain bandwidth (GBW) is given in [15]

$$GBW = -\frac{\ln S}{\beta T_S} \tag{5}$$

where β is the feedback factor of the closed-loop system (for buffers β=1) and T_S is the settling time. The setting time is defined by the speed of the ADC. The output voltage of the ADC, presented in [11], settles within 1.5 µs so the buffers must settle much faster and T_S is chosen to be 0.5 µs. According to (5) for the 9-bit resolution and T_S=0.5 µs, the GBW is ≈2 MHz.

The classic Miller compensated amplifier has very low gain bandwidth (GBW) which depends on compensation capacitor C_C and it is not suitable for this application. Also the speed is limited by the slew rate. The amplifier presented in Fig. 7 is capable to source and sink large currents so the slew rate is not an issue although quiescent current of the amplifier is only 1 µA. The GBW can be improved if the amplifier is load compensated as the amplifier in Fig. 7.

Because of the small dimensions the amplifier offset is σ= ±2.6 mV. Since the proposed ADC is fully differential circuit the buffers OA_2 and OA_4 from Fig. 6 are layouted close to each other. In this way the differential offset can be reduced.

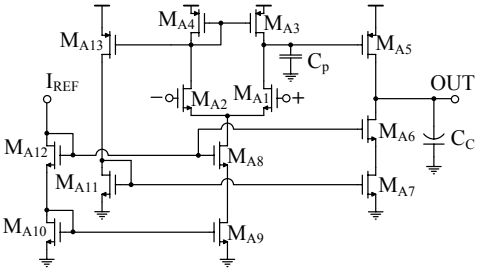


Fig. 7. Operational amplifier.

Table 1. Simulated performance of the amplifier

Parameter	Value
A_{vo} (dB)	61
GBW (MHz)	2.34
Phase margin (°)	54
PSRR@900 MHz (dB)	-70
Quiescent current (µA)	1

Table 1 presents the performance of the amplifier from Fig. 7 when C_C = 4 pF. The transient simulations confirmed that, when PM is 54 °C, the buffer amplifier has no overshoots. Fig. 8 shows simulated transient behaviour of the differential reference voltage $V_{REF\_DIFF} = V_{RHIGH} - V_{RLOW}$ during the AD conversion. During the conversion the buffers OA_2 and OA_4 charge the ADC input capacitors and the voltage V_{REF_DIFF} drops. The voltage settles to its nominal value of 485 mV within 0.5 µs which is enough for the ADC maximum conversion rate of 10 kS/s.

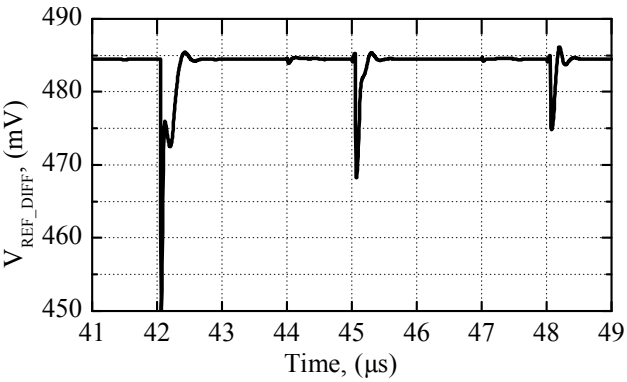


Fig. 8. Transient simulation of the ADC references simulated in Spectre.

2.4 Voltage regulators

The ADC does not need state of the art regulators so the regulators, used in this design, are actually non-inverting

amplifiers shown in Fig. 9. The amplifier gain is 3 and the targeted output voltage voltage ($AVDD$ or $DVDD$) is $AVDD = 3VDD_{REF}$ ≈1.45 V. The operational amplifier used in the voltage regulators is the same amplifier which is used for the ADC reference generation (Fig. 7). The pass element is the transistor M_{A5} (Fig. 7). To save the area a pMOS transistors $M_{d1} - M_{d3}$ are used instead of resistors. The transistors have the same (W/L) ratio, but each transistor consists of two parallel devices to improve matching. In order to track fast transition on $AVDD$ and $DVDD$ pins the feedback loop, which is formed by $M_{d1}-M_{d3}$, must have fast response time. The parasitic capacitance C_{pFB} slows loop performance and it must be reduced. This can be done by reducing (W/L) of $M_{d1}-M_{d3}$ and the transistor ratio is chosen to be 2µm/2µm. It is estimated that the capacitance $C_{pFB} \approx 20$ fF. The value of the blocking capacitors are C_{B1}= 33 pF C_{B2}= 34 pF and they are implemented as an nMOS capacitor (MOSCAP). The capacitor C_{B3} value is 3.6 pF.

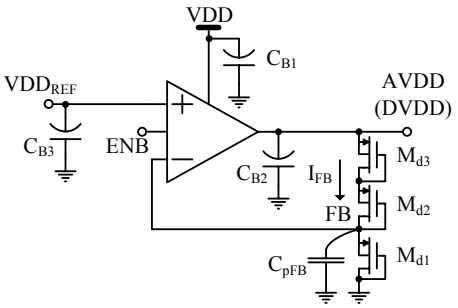


Fig. 9. Schematic of voltage regulators.

2.5 RF/DC converter

The schematic of the RF/DC converter is shown in Fig. 10. The transistors are low threshold voltage nMOS transistors with the typical threshold voltage of 220 mV. The capacitors are metal–insulator–metal (MIM) capacitors. The converter must be able to deliver at least the DC output voltage of 1.94 V for the load current of 100 nA with a minimum input amplitude. The load is the circuitry for voltage detection and voltage limiter. The optimal number of half-voltage rectifier stages (*N*), transistor size and capacitor values are obtained by simulations. The simulations have shown that the optimum circuit parameters are $W/L = 35$µm/0.24µm (all transistors have the same dimensions), $C = 0.6$ pF (all capacitors have the same dimensions) and *N*=24. The simulations confirmed that the requirements can be reached if the RF signal amplitude is only 150 mV which is less than the threshold voltage of the transistors.

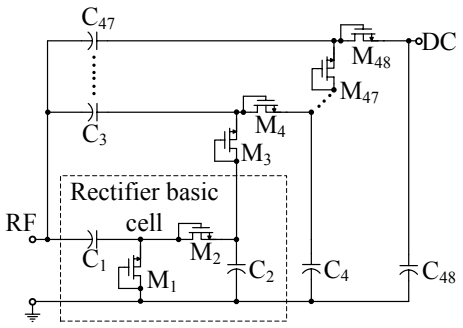


Fig. 10. RF/DC converter schematic.

3 CIRCUIT POWER-UP SIMULATIONS

Fig. 11 shows the simulated start-up behaviour of the whole circuit from Fig. 1 except the ADC. The storage capacitor C_{STORE}=11 nF and the input RF signal amplitude is 200 mV (i.e. 400 mV_{pp}). The capacitor value is relatively small because the transistor level transient simulations of the whole circuit are very slow (typically few days).

The digital signal ENB, after being set to low, enables voltage regulators and voltage reference circuits and the differential reference voltage V_{REF_DIFF}, voltages $AVDD$ and $DVDD$ from analogue and digital voltage regulators are settled to final value after 40 µs (Fig. 11). The supply voltages vary when the circuit is active. This is caused by slight changes of VDD_{REF}, as described in Section 2.1. In the simulated case the slope is $\Delta VDD/\Delta t$ ≈323 V/s.

The transistor level simulations are very slow when the RF/DC converter is included. This is because the incoming RF frequency is 900 MHz and the amplitude is very low (on the order of 200 mV, i.e. 400 mV_{pp}) while the start-up time is typically few ms and increases when the storage capacitor C_{STORE} increases. Therefore, for the optimization of the circuit start-up and performance, the RF/DC time domain model is used. The model is presented in [16].

4 EXPERIMENTAL RESULTS

The fabricated prototype in Fig. 12 occupies 800×700 μm^2. The measurement setup is shown in Fig. 13. The regulator power-up and the ADC reference power-up is shown in Fig. 14 for the case when the storage capacitor is C_{STORE}= 47 µF. The RF voltage from the signal generator HP E4421B is applied to the input RF_IN on the chip package (Fig. 13). The signal power is 8.5 dBm and the reflected power is 5.5 dBm meaning that 3 dBm are delivered to RF_IN. This input is connected by a bondwire to the input RF from Fig. 1.

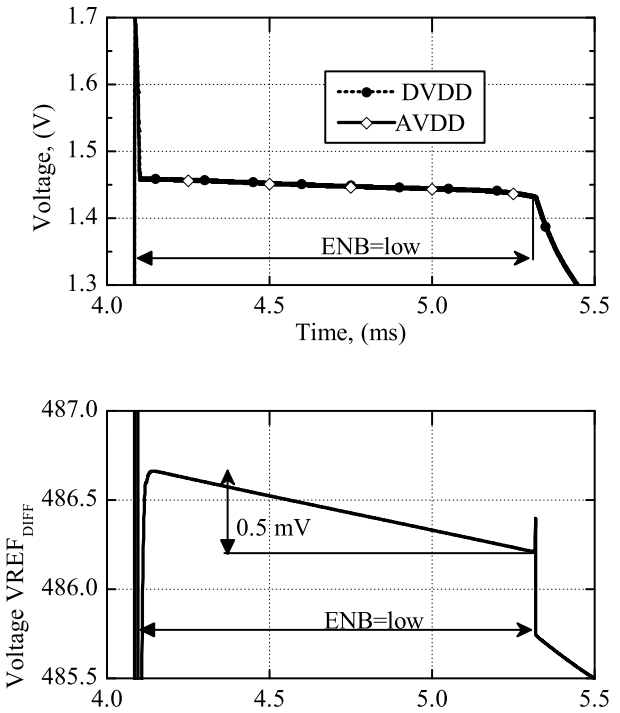


Fig. 11. The generated voltages $AVDD$, $DVDD$ and $VREF_{DIFF}$ simulated in Spectre

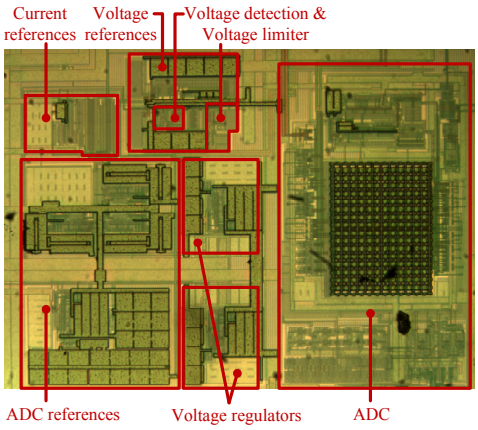


Fig. 12. Die micro-photograph of the chip (the RF/DC converter is not shown).

Because of the bondwire impedance, it is possible that even less than 3 dBm is delivered to the proposed circuit.

When the voltage VDD exceeds the upper voltage limit V_{HIGH} the circuit from Fig. 1 is enabled (ENB is low) and the voltage regulators (digital and analogue) and reference circuit are on. After VDD drops below the low voltage limit V_{LOW}, the circuit is off (ENB is high) and the regulators and reference circuit are off.

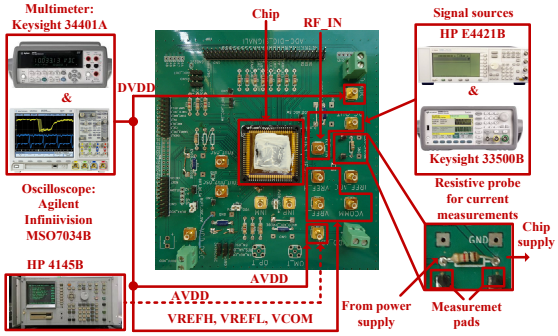


Fig. 13. Measurement setup.

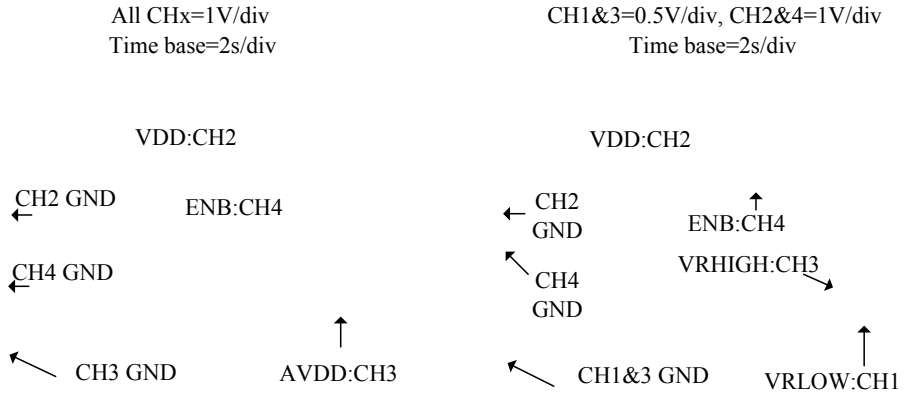
In Table 2 the reference voltages (V_{RHIGH}, V_{RMID} and V_{RLOW}), regulator voltages ($AVDD$ and $DVDD$) and the ADC reference current $IREF\_ADC$ are measured when the chip supply voltage VDD=1.8 V is a stable external voltage.

The overall current consumption I_{act} is measured when the chip is active. The voltage drop V_{Rprobe} is measured on the 1 kΩ resistor probe and the current consumption is V_{Rprobe}/1 kΩ. The digital 6 1/2 digit multimeter Keysight 34410A is used for the measurements.

4.1 Measurements of the analogue voltage regulator

The proposed circuit has two identical voltage regulators. One of them is for the analogue supply and the other one is for the digital supply. The results, presented in this section, are for the analogue regulator.

Fig. 15 presents the measured power supply rejection ratio (PSRR) of the voltage regulator from Fig. 9. The regulator PSRR is -38.1 dB@10Hz and the maximum value is -15.15 dB@200MHz. This values are not state-of-the-art but the ADC is immune to the power supply variations and this level of PSRR is sufficient. For the PSRR measurements the 100 mV_{pp} sine AC signal is applied to the input VDD of the circuit (Fig. 1) and the DC voltage is set to 1.8 V. The AC voltage is swept in the range from 10 Hz to 200 MHz. The AC signal is generated by Keysight 33500B in the range from 10 Hz to 30 MHz (30 MHz is the instrument maximum frequency). The RF source HP E4421B generates signals in the range from 250 kHz to 1 GHz and it is used in the frequency range from 30 MHz to 200 MHz. The three points are measured for each decade. The oscilloscope Agilent Infiniivision MSO7034B is used for the measurement of the AC voltage at the regulator output. The oscilloscope bandwidth is 350 MHz and that is the reason why the AC signal is swept to 200 MHz instead of 900 MHz, which is the harvesting frequency. One of the oscilloscope channels is used for the measurements of the



a) The regulator power-up. b) The voltage reference power-up.

Fig. 14. Chip power-up.

Table 2. Measured performance of the chip (C_{STORE}= 47 μF)

Parameter	Value	Description
V_{HIGH}, (V)	1.82	High switching point
V_{LOW}, (V)	1.35	Low switching point
AVDD, (V)	1.472	Analogue regulator output
DVDD, (V)	1.4	Digital regulator output
V_{RLOW}, (V)	499.5m	Low reference for the ADC
V_{RMID}, (V)	723.7m	Common-mode reference for the ADC
V_{RHIGH}, (V)	971.7m	High reference for the ADC
IREF_ADC, (A)	284n	Bias current reference for the ADC
I_{act} (A)	22μ	The overall current consumption (including the ADC) when the chip is active

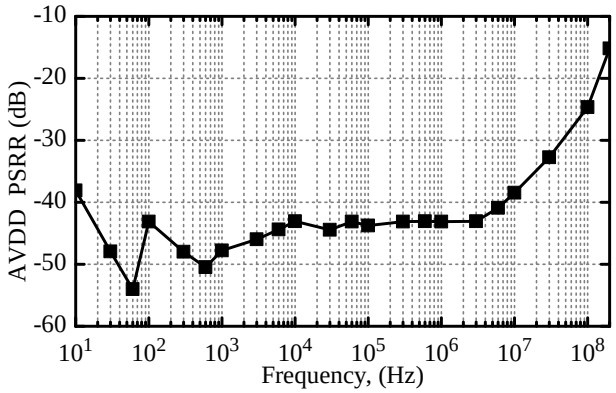


Fig. 15. Measured voltage regulator PSRR.

peak-to-peak AC voltage at the input VDD and the other one is used for the peak-to-peak voltage measurements of the regulator output. In order to avoid the measurement error, which could be caused by the oscilloscope channel mismatch, the 20 mV_{pp}, 30 MHz sine signal from the reference source Keysight 33500B is measured and it is found that both channels measure the same AC voltage, which means that there is no mismatch in the channels. For a better accuracy the oscilloscope averaging is set to 4096 counts.

Fig. 16 presents the measured DC performance of the regulator. The regulator line regulation is 122 mV/V (Fig. 16(a)). The line regulation is measured for the load current I_L=10 μA. This is the maximum current consumed by the analogue part of the ADC. The load current is set by the instrument HP 4145B which is used as a current source. The worst case load regulation in Fig. 16(b) is measured for VDD=1.6 V, which is the minimum regulator output voltage. The load regulation is 4.22 mV/μA.

Fig. 17 presents the regulator transient response when the load current changes from 0 to 10 μA for VDD=1.6 V. The measured falling edge settling time is 360 μs for the load current step from 0 to 10 μA and the rising edge settling time is 484 μs for the step from 10 μA to 0. The settling time is measured from the moment when the load current reaches 5 μA to the moment when the regulator

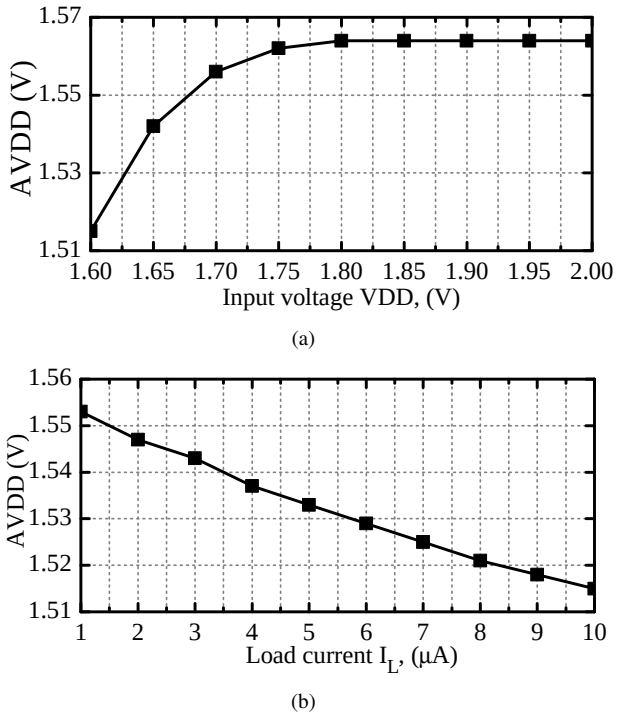


Fig. 16. Measured regulator DC response. (a) The regulator output voltage $AVDD$ as a function of the circuit voltage VDD when I_L=10 μA (b) The regulator output voltage $AVDD$ as a function of the load current I_L.

Table 3. Voltage regulator performance

Parameter	Value
Line regulation (mV/V)	122
Load regulation (mV/μA)	4.22
PSRR@10Hz (dB)	-38.1
PSRR@200MHz (dB)	-15.15
Load transient response - rising edge (μs)	2.93
Load transient response - falling edge (μs)	2.18

output voltage settles within 0.1% of the final value. The settling time is long because of the parasitic capacitance of the oscilloscope probes, PCB and probes of the current source HP 4145B. The measured parasitic capacitance is 5.46 nF. The regulator is internally loaded with the 34 pF capacitor which is 165 times smaller capacitor than the parasitic capacitance of the measurement setup. Therefore, the estimated falling edge settling time is 2.18 μs and the estimated rising edge settling time is 2.93 μs. Table 3 summarizes the regulator measured parameters.

4.2 Measurements of the voltage references

Fig. 18 presents the differential voltage reference $VREF_{DIFF} = V_{RHIGH} - V_{RLOW}$ over supply voltage variations and temperature variations measured by the 6 1/2 digit multimeter Keysight 34410A. The voltage $VREF_{DIFF}$ varies 1.6 mV for the input voltage range VDD= 1.6 to 2.1 V (Fig. 18(a)). The $VREF_{DIFF}$ stability in the temperature range from 25 °C to 70 °C is presented in Fig. 18(b) for VDD=1.6 V and VDD=2.1 V. The $VREF_{DIFF}$ variation is 10.8 mV in both cases which is 2% compared to the the voltage $VREF_{DIFF}$ at room temperature (25 °C). As it can be seen, the voltage $VREF_{DIFF}$ decreases as the temperature increases. The reason for this could be lower gain of the buffers from Fig. 7 at higher temperatures.

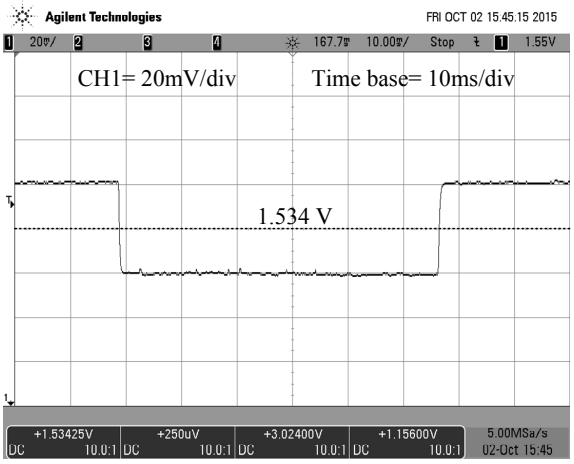


Fig. 17. Measured regulator transient response for the current load jump from 0 μA to 10 μA.

The temperature of the chip was controlled by the custom made heater which was glued by the thermal paste on the chip. The heater can change temperature in the range room temperature to 100 °C.

As described in Section 2.1, because of the parasitic gate-source capacitances of the transistors M_{p1} and M_{p2} in Fig. 6 the changes of the supply voltage VDD affect the reference voltage. Therefore the triangular voltage ($V_{\rm AC}$=400 $\rm mV_{pp}$, $V_{\rm DC}$=1.8 V, f=1 kHz) from the voltage source Keysight 33500B is applied to the input VDD. The frequency is set to 1 kHz, which means that the slope is $\Delta VDD/\Delta t$=800 V/s. The slope of 800 V/s is the worst case slope, i.e. the slope is much larger than in case when the large storage capacitor C_{STORE}= 47 μF is connected to the circuit input VDD. When C_{STORE}= 47 μF the slope is ≈0.47 V/s. The slope is calculated by using (1) for I_{act}= 22 μA (Table 2).

The storage capacitor of 47 μF is chosen because the ADC measurement (presented in section 4.3) requires a lots of samples.

Fig. 19 presents the measured results. The variation of

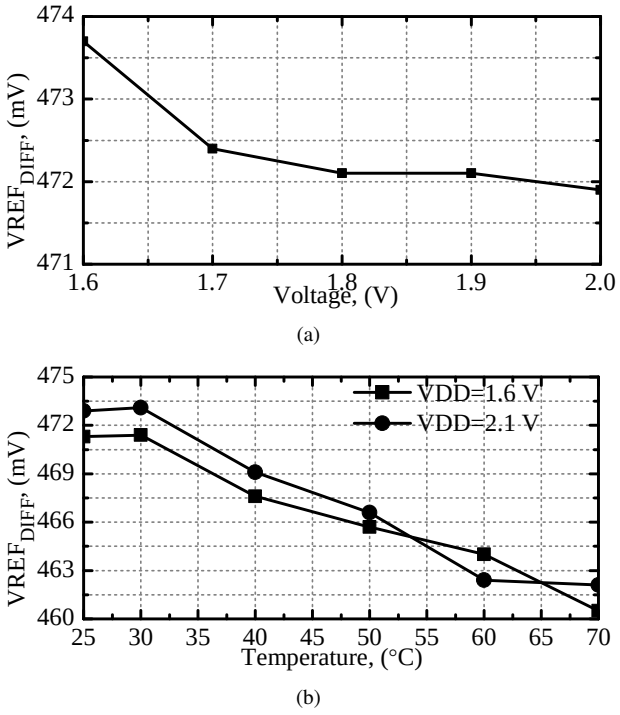


Fig. 18. Measured stability of the differential reference voltage $VREF_{DIFF} = V_{RHIGH} - V_{RLOW}$ over supply and temperature variations: (a) $VREF_{DIFF}$ over supply variations, (b) $VREF_{DIFF}$ over temperature variations .

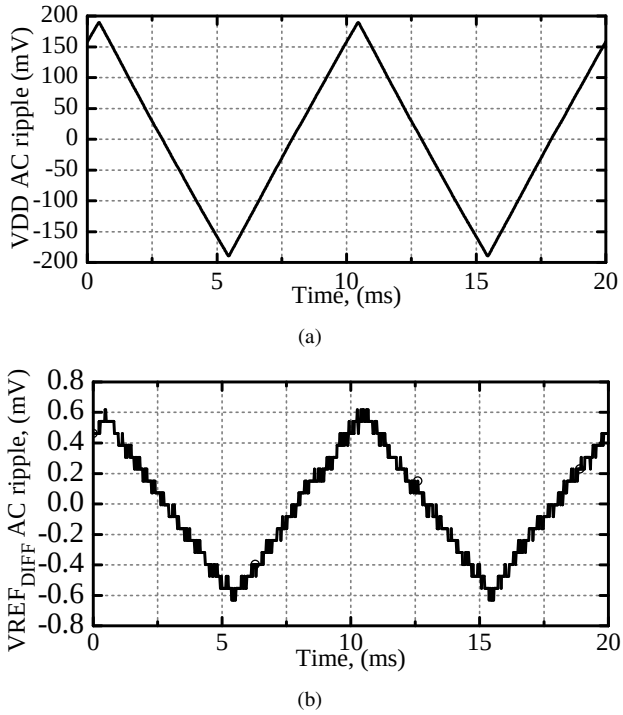


Fig. 19. Measured AC ripple. (a) AC input voltage (b) Differential reference voltage ripple.

the voltage is $VREF_{DIFF} = \pm 0.8$ mV. For the designed ADC $VREF_{DIFF} = \pm 0.8$ mV is less than 1/2 LSB.

The PSRR measurements of the voltage reference is measured by the same setup and instruments as the voltage regulator PSRR. Fig 20 presents the PSRR of the differential reference voltage $VREF_{DIFF} = V_{RHIGH} - V_{RLOW}$. The PSRR is measured at the outputs of the buffers from Fig. 6. The measured PSRR is -41.6 dB@10Hz and the worst case is -16.17 dB@200MHz.

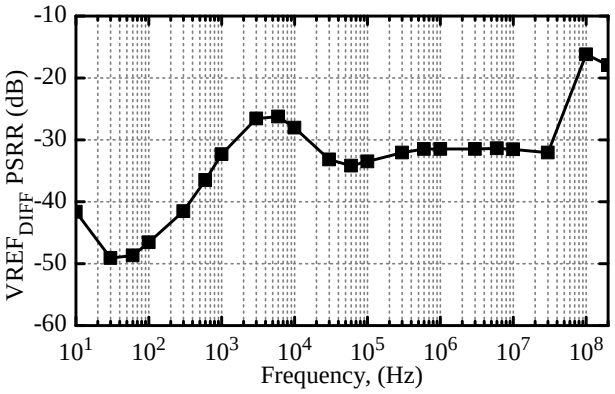


Fig. 20. PSRR of the differential reference voltage $VREF_{DIFF} = V_{RHIGH} - V_{RLOW}$.

4.3 ADC measurements

In order to test the designed voltage reference and voltage regulators they are connected to the ADC and measured together. Because the ADC digital signals are generated externally the voltage regulator for the digital part of the ADC is not used.

The designed chip is active from the moment when the supply voltage reaches V_{HIGH} till the moment the supply voltage decreases to V_{LOW}, as described by (1). As mentioned earlier, the reference voltage $VADC_{REF}$ is sampled and stored in the capacitor C_{SH}= 4.5 pF in the sample-and-hold circuit from Fig. 6 when the chip is active. This voltage is used to generate the ADC references (V_{RLOW}, V_{RMID} and V_{RHIGH}). If we would decide to measure static characteristics (DNL and INL), the chip would be active all the time and the leakage current would discharge the capacitor C_{SH} and reduce the value of the ADC references V_{RLOW}, V_{RMID} and V_{RHIGH}. That means that the ADC static characteristics (DNL and INL) can not be measured because the measurement lasts too long. For a good accuracy in case of histogram method, the input voltage must be sampled, i.e. very often more than 100k times. On the other hand the dynamic measurements are not so time consuming because they require few

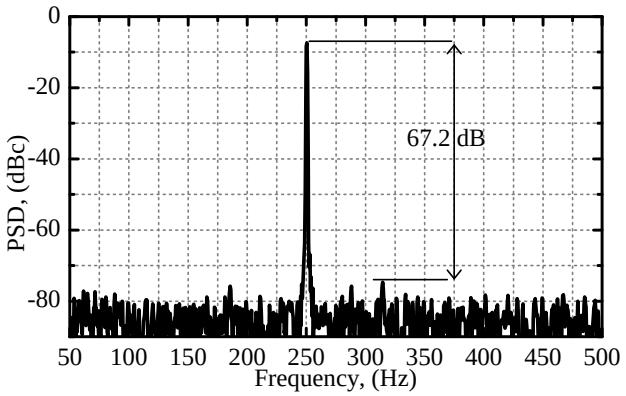


Fig. 21. Measured 2048-point FFT spectrum at 1 kS/s.

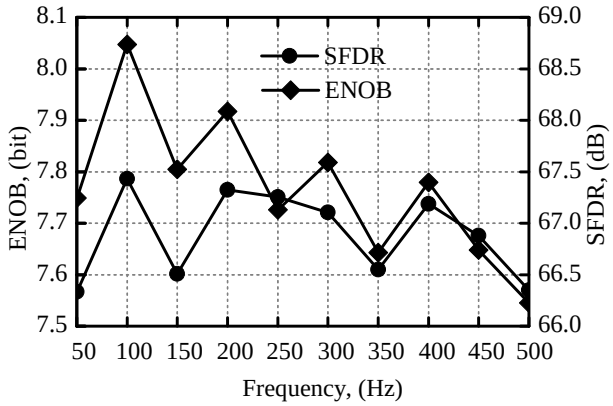


Fig. 22. ENOB and SFDR of the ADC as a function of input frequency.

thousands of samples, in this case the input sine signal is sampled 2048 times. The input sine signal amplitude is set to 940 mV_{pp} what is close to full scale range. The measured signal frequency is varied from 50 Hz to 500 Hz and the signal is sampled with 1 kS/s.

During the measurement, the chip was supplied by the DC voltage connected to the node VDD in Fig. 1. The chip is enabled only when the supply voltage exceeds upper switching point V_{HIGH}=1.82 V. Therefore, before the dynamic measurement started, the DC voltage is set to 2 V and then reduced to 1.7 V. After this procedure, the ADC dynamic performance is measured.

Fig. 21 shows measured 2048-point Fast Fourier Transform (FFT) of a 250 Hz sine signal. The measured spurious free dynamic range is SFDR=67.2 dB, signal to noise and distortion ratio SNDR=58.6 dB and the equivalent number of bits is ENOB=7.72. Fig. 22 shows the measured ENOB and SFDR with respect to the input frequency. At 500 Hz (Nyquist frequency) ENOB drops 0.5 bit compared to maximum value of 8.05 bits (100 Hz).

5 CONCLUSION

This paper presents the design of a low-power voltage reference, bias current and the supply voltage for the fully differential cyclic ADC. The references, power supply circuits and ADC are integrated into one circuit, i.e. the final chip. The proposed circuit is implemented in the UMC 0.18 μm CMOS process and occupies 800×700 μm^2. The circuit supply voltage VDD is obtained from the external RF signal of 900 MHz. When the circuit is active, VDD is used as the supply voltage for the rest of the tag circuitry. The circuit generates supply and reference voltages and currents when VDD exceeds the upper voltage level V_{HIGH} ≈1.82 V. When VDD is lower than the lower voltage level V_{LOW} ≈1.35 V the circuit is disabled. When the circuit is active, the overall current consumption including the ADC is 22 μA.

The measured differential reference voltage $VREF_{DIFF}$ is 472.1 mV which is close to the targeted 485.8 mV. The variation of the differential voltage $VREF_{DIFF}$ is 1.8 mV when the voltage VDD varies from 1.6 V to 2 V. The measured power supply rejection ratio is -41.6 dB@10Hz.

The voltage regulator line regulation is 122 mV/V and the load regulation is 4.22 mV/μA. The measured PSRR is -38.1 dB@10Hz.

The designed voltage regulator as well as the ADC current and voltage references are connected to the ADC and the ADC dynamic performance is measured. The ADC sampling rate is 1 kS/s. At 500 Hz (Nyquist frequency) the effective number of bits is 7.5 bits, spurious free dynamic range 66.35 dB and signal to noise and distortion ratio 47.8 dB.

Measurements confirmed that the designed circuit can provide stable voltage references and power supply for the 9-bit ADC.

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