A NEW DFT ARCHITECTURE TO REDUCE TEST DATA VOLUME AND TEST APPLICATION TIME

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Abstract:

This paper proposes a new DFT Architecture that contains three test scan modes. The test data could be interval broadcast to scan chains whenever the data in corresponding locations are compatible. Compared with the conventional broadcast scan architecture, the proposed architecture achieves better compression ratio in all cases, and the test application time is also induced. The hardware overhead is very low. Both theoretical and experimental results prove efficacy and versatility of the proposed scheme.

1 Introduction

The scan-based design-for-testability (DFT) is widely used in industry. For conventional single scan chain, all test vectors have to be shifted in a serial scan path, and the long time to shift test data is due to the large number of internal flip-flops [1]. To reduce scan-shift operations, the multiple scan chains architecture was proposed [2]. It divides a serial scan chain into a number of shorter scan chain segments and thus reduces the time needed to shift input/output vectors. However, the test time reduction is achieved by using more test pins, while the test data volume remains unchanged. Many test data compression schemes have been proposed to reduce the test data volume and tester channel requirements [3-4]. The Illinois Scan Architecture (ILS)[5], as shown in Fig. 1, is one of the most useful and efficient architectures to reduce test application time and test data volume for testing today's high density VLSI circuits.

As shown in Fig. 1, a single scan chain is partitioned into multiple scan chain segments, which are fed by the same set of data whenever the data in segments are compatible. It has two operation modes: broadcast scan mode and serial scan mode. It is accomplished by using an ATPG to generate vectors in broadcast scan mode, the scan-in pin feeds into each of the scan chain segments, and each segment will be shifted into the same parallel loaded test data. Since broadcast scan mode imposes constraints on test patterns, many faults become untestable. To cover these untestable faults, an ATPG is used to generate test vectors under serial scan mode. Additional hardware required for this includes multiplexers (MUXs) for each scan chain segment to switch between the two modes of operation. In addition, a MISR or combinational compactor is needed.

To enhance the fault coverage in broadcast scan mode and improve test compression efficiency, many techniques have been developed by using scan cells rearranging scheme [6-9]. These schemes gain better compression results. However, as/since this may increase the wiring complexity and cost of the scan chain, the physical locations of the flip-flops on silicon are determined at an early design stage before scan insertion. There are also some other ILS

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optimization schemes to reduce test pins or test power. A low pin test for ILS is proposed in paper [10]. MILT [11] uses multiple test modes to reduce test pins and test data volume. Paper [12] presents a new functional Illinois scan at the register-transfer (RTL) level where test data compression is similar or even better than the gate level counterpart. Some other works also focus on reducing test power of the ILS scan [13-14]. There are some other testing schemes to check reliability of other systems [15-16].

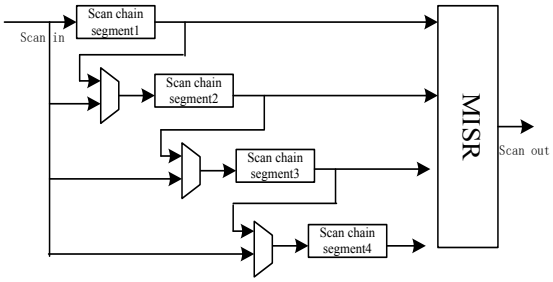

Figure 1. Illinois Scan Architecture.

To reduce test data volume and test application time, the paper proposes a new DFT scheme with multiple scan chains which can make the full use of compatible scan cells. It uses interval broadcast scan mode and new serial scan mode as a replacement of the ILS's serial scan mode. The proposed architecture has the same hardware cost as ILS's, and is compatible with some prior optimization techniques on ILS, such as scan chain reconfiguration schemes, test generation for Illinois scan, etc.

2 Proposed DFT Architecture

As shown in Fig. 1, if all test vectors can operate in the broadcast mode, the ILS architecture can achieve its best results, and consequently both test application time and test data volume can be very much reduced.. However, there are several hard-to-detect faults whose test vectors could not work in broadcast mode. These vectors must operate in serial mode (called *S_Vector*), which requires big test data volume and long test application time.

Since/ As an *S_Vector* is applied to the ILS architecture, and providing that test data in one scan cell is not compatible with any others in the same depth, the vector has to be shifted serially, and ILS broadcast architecture scan simply becomes a single scan chain. An *S_Vector* example is shown in Fig. 2, for all six scan chains segments, and as obviously only the first bit of test data in the same depth is incompatible, it also has to be operated in serial test mode in ILS architecture, and 60 bits must be stored for the *S_Vector*. The large volume of *S_Vectors* would reduce the effectiveness of the data compression scheme, which is the inefficiency of the ILS architecture stem form.

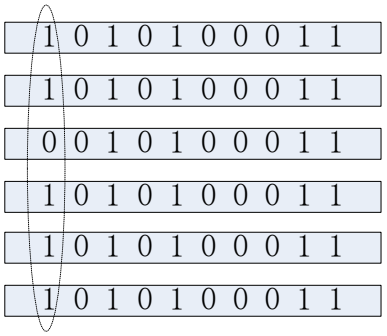

Figure 2. An S Vector example.

To make the full use of the compatible test set, a better approach would be allowing broadcasting identical data to scan segments whenever test data in the same depth scan cells are compatible (scan cells in the same column in Fig. 3). Thus, in this new approach, even an *S_Vector* in ILS Architecture may partly broadcast data.

An architecture example of the proposed DFT architecture is given in Fig. 3. The architecture has *m* scan segments and *n* scan cells each. The hardware required includes multiplexers (MUX) for each scan chain segment, a MISR or combinational compactor to check the signatures. Except these, the proposed architecture inserts a MUX in the front of the first scan cell for each scan chain segment. Three test modes exist in the new architecture, the first mode is *broadcast scan mode* where test data are broadcast to multiple scan chains. The second test mode is *interval broadcast mode* which allows interval broadcast compatible test data to multiple scan chain. The last test mode is *serial test mode* where test data must be shifted serially into scan chains.

The test pattern generation (TPG) is first generated for the broadcast scan mode, the corresponding test vectors are presented as *B_vectors*. Then, for all

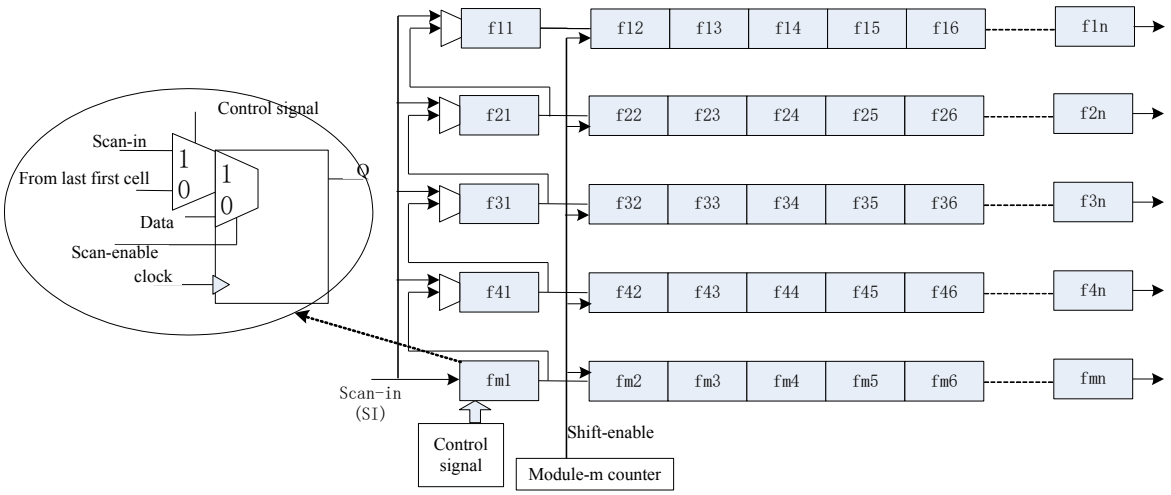

Figure 3. The proposed architecture example.

remaining undetected faults, a non-filling TPG is used to produce a partially specified test set *BS_vectors*. The three operation phases of the test generation begin with the first phase of a broadcast operation that is the same as traditional ILS using broadcast test set *B_vectors*. Two test set parts divided from the *BS_vectors* are then applied to the interval broadcast mode and new serial scan mode, respectively.

For the proposed DFT scheme, scan cells in the same depth share the same test data if they receive compatible test logic value. Otherwise, the incompatible data will be shifted serially through a shift register composed of the first scan cell of all scan segments. These MUXs are used to choose data from scan-in (SI) and the first scan cell of its adjacent scan chain segment. If the MUX-select signal is high, SI feeds all the scan chains with the same data. Otherwise, only the first scan chain receives the new scan-in data from SI, and the shift-enable is inactive to prevent all scan chain segments from shifting, the module-m counter(m is the number of scan segments) controls the operation of shifting data to the first scan cell of each scan chain segment. The signal of *shift-enable* is enabled when the *mode-m counter* is zero. The output of each scan chain is connected to a multiple input signature analyzer (MISR).

The broadcast scan mode and the new serial scan mode are used to broadcast test data and shift test data respectively, seriallyin the new architecture, and they can be easily controlled by the signals of the MUXs. The MUX-select signals are set to high in broadcast test mode, and are set to low in serial test mode. However, for interval broadcast mode, the MUX-select signals are decided by the compatible of the corresponding same depth test data, and these corresponding MUX-select signals must be stored.

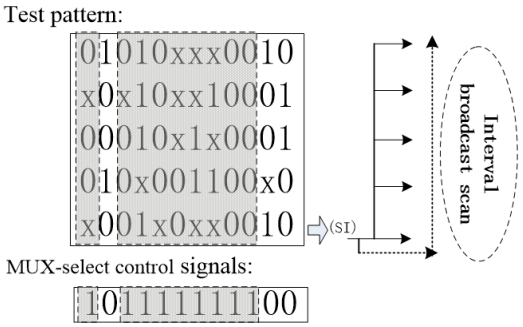

Figure 4. Getting the MUX-select signals for interval broadcast scan mode.

Whether the same depth scan cells are compatible or not is simply determined by nothing but an absence of logic value conflicts. An example of MUX-select signal computation is given in Fig. 4, test data shown in the shade box illustrates that the data in the same-depth scan cells are compatible, the corresponding MUX-select control signals are set to high, and the shared data are broadcast to shared scan chain segments. Otherwise, the control signal is set as low; the corresponding different test logic values are serially shifted to the first scan cells of all shared scan chain segments.

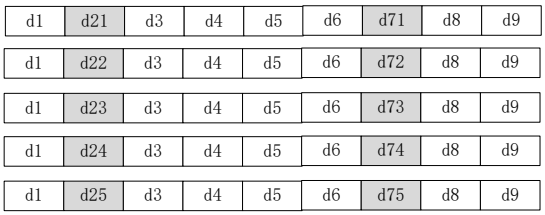

Figure 5. A vector operating in interval broadcast scan mode.

Algorithm1:

dividing *BS_vectors* set into two parts for interval broadcast scan and new serial scan

Input:

BS_vectors: ILS serial test set;

V_i: each *BS_vectors*;

x_i: The number of conflict depths for each vector V_i;

m: the number of scan chain segment in OILS;

n: the number of scan cells that each scan segment contains in OILS.

Output:

S1: test set for interval broadcast scan;

S2: test set for new serial scan.

Begin:

For each V_i in *S*

The storing bits is computed as $m \times n$ under ILS architecture;

The storing bits is $m \times x_i + (n - x_i) + n$ if using interval scan mode;

If x_i meets the inequation ($m \times n > m \times x_i + (n - x_i) + n$), the V_i is put into *S1* which will be applied to interval broadcast scan mode. Otherwise, the V_i belongs to *S2* that would be applied to new serial scan mode.

End.

An example vector that operates in interval broadcast scan mode is given in Fig. 5. The architecture has 5 scan segments with 9 scan cells each. A vector in *S* is applied to the proposed architecture and has compatible data in all depths except depth 2 and depth 7. Thus, the data of d1, d3, d4, d5, d6, d8 and a9 are broadcast, while the data of depth 2(d21, d22…d25) and depth 7(d71, d72…d75) are serially shifted through the shift register composed of the first scan cell of each scan segments. The bits need to be stored consist of three parts: 2×5 bits serially shift conflict data; (9-2) bits broadcast compatible data; 9 bits MUX-select signals, totally 26 bits. It is assumed that the vector applied to the ILS architecture must be operated in serial scan mode for/as there are conflicts appearing in d2 and d7. The bits need to be stored are 5×9=45 bits, and 45-26=19bits are saved.

To achieve best compression result, if a *BS_vector* has no or very little compatible same depth test data, it should operate in serial scan mode since/as lots of MUX-select signals must be stored in interval broadcast scan mode. Otherwise, the *BS_vector* should be applied in interval broadcast mode.

The orders of the vectors have no Impact on fault coverage, so a simple algorithm is used to divide *S* into two parts here, the first parts operate in interval broadcast scan mode and the second parts operate in serial scan mode. The algorithm is given in Algorithm1. For the *BS_vector Vi* , it needs $m \times n$ bits to store it if it applied in serial scan mode. The storing bits needed are $m \times xi + (n - xi) + n$ bits if it operated in interval broadcast scan mode. The algorithm checks for each vector *Vi* in *S*, and puts *Vi* into the proper part for storing smaller test data volume. Take an example as Fig. 4, $m=5, n=9$, take *m* and *n* in the inequation of ($m \times n > m \times xi + (n - xi) + n$), we get that $xi < (27/4)$. Thus, if $xi \leq 6$, Vi operates in interval broadcast mode, otherwise, it operates in new serial scan mode. Then *S* is divided into *S*1 for interval broadcast scan mode and *S*2 for serial scan mode.

3 Experimental results

A default order of scan cells is assumed in the experiments. Test pattern generation with random-fill was performed by using a modified Atalanta for broadcast scan mode, while generation without random-fill was accomplished to generate for the corresponding serial scan mode. The serial test patterns are divided into two parts using Algorithm1 for interval broadcast mode and serial mode. Since/As there are many ILS optimization schemes which use scan chain modification, these schemes could also be applied to the OILS. So, we only compare the proposed scheme with the conventional ILS in the same situation. The experimental results are given in Table 1 and Table 2.

Table 1 presents the test data volume comparison

results for conventional ILS and the proposed DFT scheme. *M* is the number of scan chain segments. *Bn* and *Sn* are the number of test vectors of broadcast scan mode and serial scan mode, respectively. *IB* and *IS* are the number of test patterns for interval broadcast scan mode and serial scan mode, respectively. *TV*1 is the test volume of the ILS. TV2 is test volume of the proposed scheme. *Vsav* is test data volume savings, and it is computed as expression (1).

Table 1. Test volume comparison results

circuit	m(#)	Bn(#)	Conventional ILS		Proposed interval broadcast scan			
			Sn(#)	TV1	IB(#)	IS(#)	TV2	Vsav(%)
S5378	6	221	43	18263	15	28	16293	10.79
S9234	6	349	150	24973	116	34	19254	22.90
S13207	8	326	383	290920	296	87	122978	57.72
S15850	9	356	96	88916	65	31	58507	34.59
S35932	9	61	10	20253	3	7	18312	9.58
S38417	16	856	90	132512	78	12	59485	55.11
S38584	16	606	102	182052	56	46	131901	27.55

Table 2. Test application time comparison results

circuit	m(#)	Bn(#)	Conventional ILS		Proposed interval broadcast scan			
			Sn(#)	TPT1 (cycles)	IB(#)	IS(#)	TPT2	Tsav(%)
S5378	6	221	43	14808	15	28	13071	11.73
S9234	6	349	150	44968	116	34	36783	18.20
S13207	8	326	383	258791	296	87	105043	59.41
S15850	9	356	96	60829	65	31	36923	39.30
S35932	9	61	10	25786	3	7	23563	8.62
S38417	16	856	90	238111	78	12	121341	49.04
S38584	16	606	102	202234	56	46	155194	23.26

Table 2 gives the test application time comparison results. *TPT1* is the test application time of ILS's, and it is computed as expression (2) where *scsL* is the number of scan cells in the longest scan chain segment. *TPT2* is the test application time of the proposal. It is computed as expression (3) where *ci* and *ici* are the number of compatible locations with same depths and the incompatible locations with same depths for vector *i*, respectively. *Tsav* is test application time saving that

$$(TV1\text{-}TV2)*100/TV1 \quad (1)$$

$$1+scsL+(1+scsL)\times Bn+m+1+FA+(1+FA)\times Sn \quad (2)$$

$$1+scsL+(1+scsL)\times Bn+m+\sum_{i=1}^{IB}(m\times c_i+ic_i)+1+FA+(1+FA)\times IS \quad (3)$$

$$(TPT1\text{-}TPT2)*100/TP \quad (4)$$

computed as expression (4). *FA* is the number of scan cells in circuit. These two tables prove that the proposed interval broadcast scan better compression efficiency, and the test application time is also very reduced.

Through scan chains reconfiguration without routing constraints, ILS architecture could achieve high Fault coverage in broadcast mode for ISCAS 89 circuits [5]. However, as the physical locations of the flip-flops on silicon are determined at an early design stage before scan insertion, scan chains reconfiguration may increase the wiring complexity and cost of the scan chain, and therefore some reconfiguration methods without routing constraints

are not practical. The proposed DFT architecture achieves better compression results under default scan cells order, and consequently has the same compression results as ILS's in the worst theoretical case.

4 Conclusion

The paper proposes a new DFT scheme with multiple scan chains, which can make a full use of the compatible scan chains. It has three test modes: broadcast scan mode, interval broadcast scan mode and serial scan mode. It is worth noting that undoubtedly, the proposed architecture has not only the same hardware cost as ILS architecture but it is also compatible with some prior optimization techniques on multiple scan chain architecture.

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References

[1] Tsai, B.-J., Wang, S.-J.: *Multi-mode segmented scan architecture with layout-aware scan chain routing for test data and test time reduction*, IET Computer & Digital Techniques, 2(2008), 5, 434–444.

[2] Wang, L., Wang, Z., Wen, X.: *VirtualScan: Test compression technology using combinational logic and one-pass ATPG*, IEEE Design & Test of Computers, 25(2008), 5, 122-129.

[3] Tyszer, J., Filipek, M., Mukherjee G.: *New test compression scheme based on low power BIST*, Pro. in IEEE European Test Symposium, Avignon, 2013, 1-6.

[4] Dongsoo, L., Kaushik, R.: *Vitebi-based efficient test data compression*, IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems, 31(2012), 4, 610-619.

[5] Pandey, A.R., Patel, J. H.: *Reconfiguration technique for reducing test time and test data volume in Illinois scan architecture based designs*, Proc. IEEE VLSI Test Symposium, Monterey, CA, USA, 2002, 9-15.

[6] Gupta, P., Kahng, A.B., Mantik, S.: *Routing-aware scan chain ordering*, Proc. Asia and South Pacific Design Automation Conference, Kitakyushu, Japan, 2003, 857 – 862.

[7] Wang, S., Peng, K., Li, K.: *Layout-aware scan chain reorder for skewed-load transition test coverage*, Proc. Asian Test Symposium, Fukuoka, 2006, 169-174.

[8] Donglikar, S., Banga, M., Chandrasekar, M., Hsiao, M.S.: *Fast circuit topology based methods to configure the scan chains in Illinois scan architecture,* International Test Conference, Austin, TX, 2009, 1 - 10.

[9] Banerjee, S., Mathew, J., Pradhan, D. K. Mohanty, S. P.: *Layout-aware Illinois scan design for high fault coverage*, 11th International Symposium on Quality Electronic Design, San Jose, CA, 2010, 683-688.

[10] Shah, M.A., Patel, J. H.: *Enhancement of the Illinois scan architecture for use with multiple scan inputs*, Proc IEEE Computer society Annual Symposium on VLSI, TX, USA, 2004.

[11] Chandra, A., Yan, H., Kapur, R.: *Multimode Illinois scan architecture for test application time and test data volume reduction*, Proc. IEEE VLSI Test Symposium, Berkeley, CA, 2004.

[12] Ko, H.F, Nicolic, N.: *Functional Illinois scan design at RTL*, Proc. IEEE International Conference on Computer Design: VLSI in Computers and Processors, Hamilton, Ont., Canada, 2004, 78-81.

[13] AlQuraishi, E., AlTeenan, R.: *Average power reduction in compression-based scan designs*, 15th IEEE Mediterranean Electrotechnical Conference, Valletta, 2010, 504-509.

[14] Czysz, D., Kassab, M., Lin, X., Mrugalski, G.: *Low-Power scan operation in test compression environment*, IEEE Trans. Comput.-Aided Design Integr. Circuits Syst, 28 (2010), 11.

[15] Wan, B., Fu, G., Pei, C., Dong, Y.: *Storage degradation mechanism analysis and storage life prediction of the optoelectronic coupler based on multi-channel degradation testing data*, Engineering Review, 3 (2014), 34.

[16] Gašparini, K., Nasser, A., Sladić, S.: *The fault tolerant led power converter design for more efficient and durable lighting*, Engineering Review, 3 (2014), 4, 189-195.