Online ISSN 1848-3380, Print ISSN 0005-1144
ATKAFF 57(2), 506–513(2016)

Jong-Ryul Yang

Gate Driver Integrated Circuit with Breakdown Protection for Switch-mode Power Amplifiers

DOI 10.7305/automatika.2016.10.1005
UDK 621.375.4.026.051

Original scientific paper

This paper proposes a gate driver integrated circuit to prevent breakdown of switching power amplifiers. The proposed circuit consists of a dead-time generator, level shifters, and a breakdown blocker. The dead-time generator makes non-overlapped input signals and the breakdown blocker detects instantaneous turned-on input signals and resets them to the off-state before the switching power cells are damaged. The circuit is designed using TowerJazz's $0.18\,\mu$m BCD process for a tightly coupled wireless power transfer system. The protecting operation is verified using circuit simulation including layout-dependent characteristics.

Key words: Breakdown blocker, dead-time generator, gate driver circuit, switching power amplifiers

Pobudni sklop sa zaštitom od kvarnog stanja za pojačalo snage. U ovom radu prikazan je pobudni sklop za sprječavanje kvarnog stanja pojačala snage. Predloženi krug sastoji se od generatora mrtvog vremena, translator razine i sklopa za sprječavanje kvarnog stanja. Generator mrtvog vremena tvori neprekloplјene ulazne signale, a sklop za sprječavanje kvarnog stanja prepoznaje trenutno paljenje ulaznog signala i resetira ih prije nego su ćelije pojačala snage oštećene. Krug je dizajniran koristeći TowerJazz's $0.18\,\mu$m BCD postupak za povezani sustav bežičnog prijenosa snage. Zaštita je verificirana koristeći simulaciju kruga uključujući karakteristike povezane s izgledom.

Ključne riječi: sklop za sprječavanje kvarnog stanja, generator mrtvog vremena, pobudni sklop, pojačalo snage

1 INTRODUCTION

Class D half-bridge voltage-switching power amplifiers have been widely used in power applications; two transistors in the power amplifier are operated as switches [1]. The large-signal channel resistance of the transistors in on-state switch mode, which is called R_{ON}, makes the conduction loss of the amplifier [1]. To reduce the loss and improve the conversion efficiency, transistors with low R_{ON} are used in the amplifier [2]. The gate driver controls the signals to operate each power cell transistor alternately. If both power cells are simultaneously turned on because of the transition characteristics of the switches, mismatching of the two driving signal paths, inflow noises, or power supply vibration, the drain-source current of the transistor increases in an extreme fashion and the amplifier cannot transmit the output power to the load, as shown in Fig. 1 [3]. The increased current can generate a breakdown of the transistors or of the metal interconnections in the amplifier [3]. For stable operation of the amplifier, the gate driver should protect the switching power cells from breakdown.

The dead time, which is the time when both switches are turned off, is a general solution to prevent breakdown [3,4]. However, the dead time induced by the gate driver should be optimized within a certain range to obtain both stability of the switching operation and efficiency of the amplifier [5-8]. The harmonic distortion is increased and the efficiency is degraded as the dead time increases [5–8]. Because the transmission efficiency is the most important

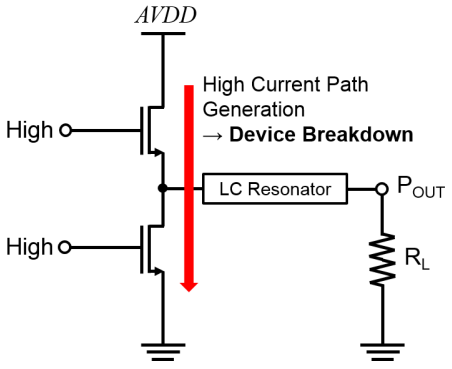

Fig. 1. Breakdown of Switching Transistors

factor in the transmitter of a wireless power transfer system [9-11], a controllable dead-time generator and an additional protection circuit are required in the driver circuit to increase both the stability and the efficiency.

This paper presents the gate driver integrated circuit (IC) to generate a controllable dead time and enhance the stability of the amplifier. Level shifters are included in the driver to adjust the gate input levels and adequately drive the switching power cell N-type transistors. For a tightly coupled wireless power transfer system [12,13], the circuit is designed using TowerJazz's $0.18\,\mu$m BCD process. A simulation, including layout-dependent characteristics, is used to demonstrate the overall operation.

2 SCHEMATIC OF THE PROPOSED GATE DRIVER IC

Figure 2 provides a schematic of the half-bridge power amplifier with the proposed gate driver IC. N-type transistors are used on both sides of the switching power cell because the R_{ON} of an N-type transistor is smaller than that of a P-type transistor [14] and the optimum size of the device layout is obtained with the same transistors. The dead-time generator makes non-overlapping differential signals using a pulse-width modulated (PWM) input signal. The level shifter converts the differential signals from standard logic levels to target logic levels for each switching power cell N-type transistor. When delay mismatching of signal paths in two level shifters is increased, or the dead-time is not adequately generated, the on-state signals can be concurrently transmitted to both gates of the switching transistors, as shown in Fig. 1. And then, a breakdown blocker rapidly changes the two gate inputs to the off-state before the switching power cells are turned on by the on-state signals. The minimum dead time can be achieved by controlling the parameters of the dead-time generator; the stability of the amplifier can also be improved by using the breakdown blocker. The layout size of the power amplifier with the gate driver IC, as shown in Fig. 3, is $0.6\,\text{mm} \times 0.55\,\text{mm}$, including I/O pads.

2.1 Dead-time generator

The proposed dead-time generator, as shown in Fig. 2, uses a circuit topology of a D flip-flop, including inverter buffers and RC filters in the feedback paths. When it is assumed that the operation time of the D flip-flop is negligible, the dead time t_D generated by the proposed circuit can be expressed as

$$t_D = 2 \times t_{INV} + t_{RC}\,, \tag{1}$$

where t_{INV} is the time delay of the inverter buffer, and t_{RC} is the time delay of the RC filter. The time delay t_{RC} is a dominant factor of the dead time because minimum-size inverters are used. The dead time can be controlled to vary the capacitance of a capacitor bank in the filters. High-frequency glitches in the output signal of the generator can be decreased using the RC filters, which reduce harmonics in the feedback path. Additional inverter buffers can be used in the outputs of the generator to decrease the rise and fall times of the output signals.

2.2 Level shifter

Differential signals from the dead-time generator are adjusted by the level shifters, as shown in Fig. 4. Common source amplifiers are used to increase the on-state voltage, but the supply voltages are different in each amplifier because the required on-state voltages are different in each power cell N-type transistor. Because the maximum gate-source voltage of the N-type transistors is $5\,\text{V}$, the level shifter is designed such that the on-state voltages are set at 5 V for the low-side switching transistor and at the analog supply voltage *AVDD* for the high-side transistor. The off-state voltage is set at $0\,\text{V}$ for the low-side and at *AVDD*-$5\,\text{V}$ for the high-side, so that the two switching transistors have the same voltage differences between on and off states. The analog supply voltage is set at $19\,\text{V}$ in the design of the level shifters. Because the widths of the transistors are nearly equal, the voltage differences lead to similarly transient performances due to the rise and fall times and output swing levels of each power cell. Therefore, harmonic distortion in the output of the amplifier can be decreased by using the same voltage differences.

2.3 Breakdown blocker

When on-state signals abnormally occur at the gate nodes of both switching transistors, the breakdown blocker, as shown in Fig. 2, changes the inputs of the level shifter to the off-state; the dead time is additionally generated to prevent the breakdown of the switching power cells. The breakdown blocker consists of a logic state detector and a comparator with an output inverter buffer. The maximum current I_{DMAX} through *RD* and the maximum output voltage V_{DMAX} at the detector shown in Fig. 5 are generated when both gate inputs are on. The reference voltage V_{REF} is fixed in the voltage range between V_{DMAX} and the normal output voltage V_{DN}, which is shown when either of the transistors is on. The transistors in the detector are of the same types as the switching transistors, but they can operate faster than the switching power cells due to their small size. The comparator outputs the off-state signal on the input of AND gates when the detector output voltage V_D is larger than V_{REF}; the AND gates reset the logic state at the inputs of the level shifter. The digital supply voltage *DVDD* is set at $1.8\,\text{V}$ in the design of the gate driver. For

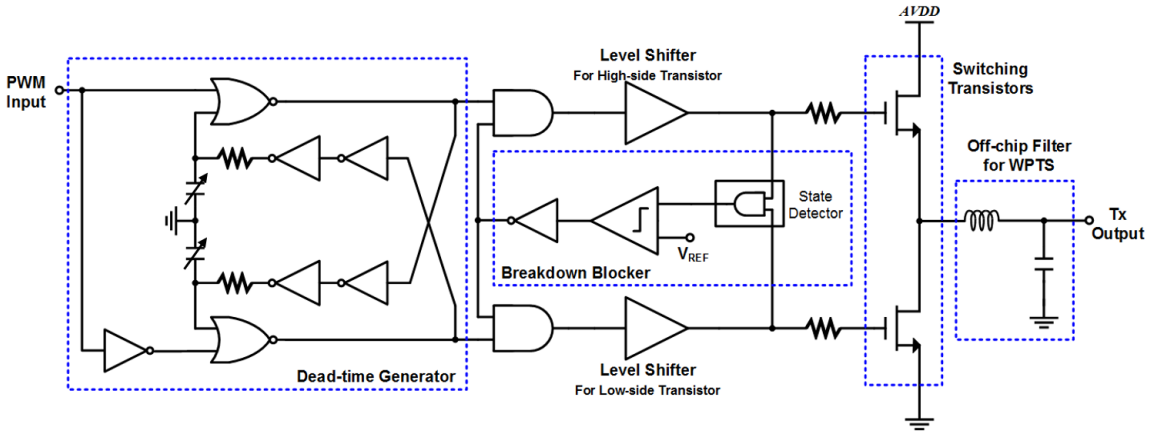

Fig. 2. Block diagram of the gate driver integrated circuit and the half-bridge power amplifier for the tightly-coupled wireless power transfer system (WPTS).

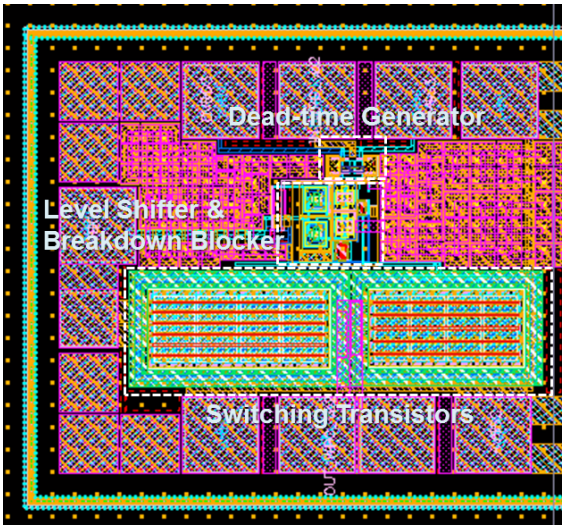

Fig. 3. Layout of the power amplifier with the proposed gate driver IC using TowerJazz's 0.18 *µm BCD process.*

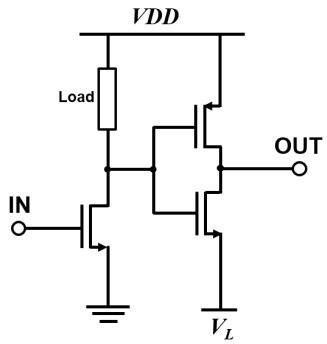

Fig. 4. Schematic diagram of the level shifter. The VDD is 5 *V for the low-side switching transistor and AVDD for the high-side transistor. The VL is* 0 *V for the low-side and AVDD-*5 *V for the high-side.*

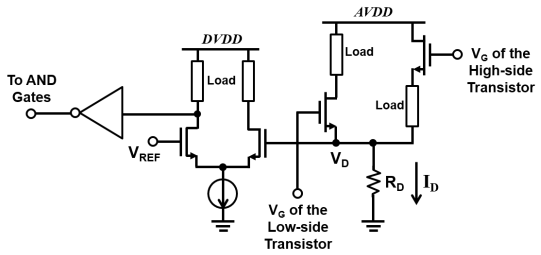

Fig. 5. Schematic diagrams of the breakdown blocker. The DVDD is the supply voltage of the digital logic circuits.

stability enhancement of the blocker, a small sized capacitor, such as several pF, should be used at the output of the detector and the comparator.

3 DEMONSTRATION RESULTS

Figure 6 shows simulation voltage waveforms in each node of the power amplifier with the gate driver IC shown in Fig. 2 under normal conditions. Depending on the layout, the simulation is performed to consider the effects of the parasitic factors, such as the metal resistance and the parasitic capacitance in the devices and interconnections. Referring to WPC [12] and PMA [13] specifications, the analog supply voltage is set at 19 V with 1 V variation. The driver IC can operate within a frequency range from 100 KHz to 300 KHz for application to both standards of wireless power transfer systems [12,13]. The dead times induced by the generator are shown in the insets of Fig. 6 and Fig. 7. The dead time can be controlled by the capacitance of the RC filter at the feedback path of the generator.

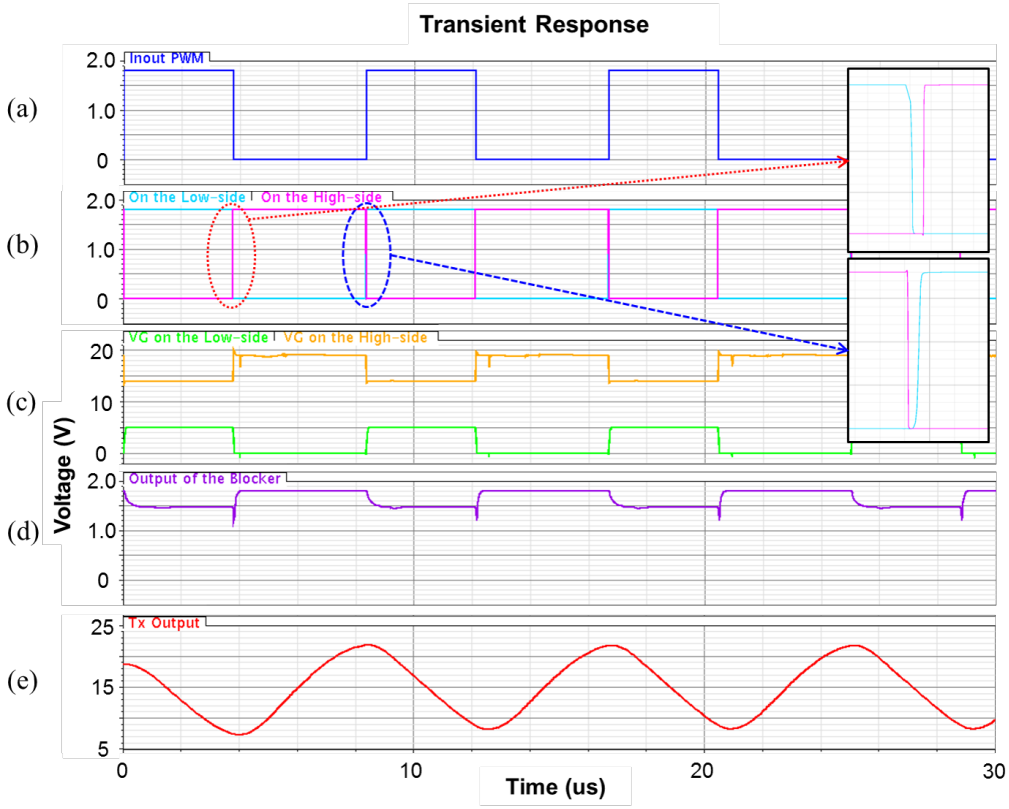

Fig. 6. Simulated voltage waveforms of the amplifier in Fig. 1 under normal conditions: (a) Input PWM signal, (b) outputs of the dead-time generator, (c) gate signals of the switching transistors, (d) Output of the breakdown blocker, and (e) output of the amplifier. Block-box insets: Detailed view of the outputs of the generator.

The nominal values of the resistance R and the capacitance C are set, respectively, at 1 KΩ and 50 fF at the 120 KHz operating frequency. The value of the capacitance can be varied up to 1 pF to control the dead time. Though the output of the breakdown blocker has noise signals, the output maintains the on-state voltage because the switching transistors operate in each by the logic signals with the dead time. The half bridge class D power amplifier using the proposed gate driver IC has a 7.2 W transmitted power and a 0.5 A maximum drain-source current at 120 KHz operating frequency. The values of the inductor and the capacitor of the LC resonator, shown in Fig. 1, are set at 17.6 μH and 100 nF. The value of the load impedance of the amplifier is set at 12 Ω, according to the test conditions of the WPC standard [12].

Simulation waveforms under abnormal conditions are shown in Fig. 8. The dead-time generator does not work in this condition, and arbitrary signals with 15 ns overlapping time are inputted to the output nodes of the generator. When both gate input signals of the switching power transistors are simultaneously in the on-state voltage, the breakdown blocker resets the gate signals before turning on the switching transistors. As shown in Fig. 8, the gate signals are changed to the off-state voltages, while the output voltage of the blocker is under the threshold voltage of the logic level. Figure 9 shows that the proposed blocker can be successfully operated at the 300 ns overlapping time between two input PWM signals. It is verified using simulation that the breakdown blocker can securely protect the power cells under 500 ns overlapping time. In the simulation with 300 ns overlapping time, oscillation signals are observed at the output of the driver, as shown in Fig. 9. The signals are caused by long overlapping time. Because the dead-time generator prevents the generation of long overlapping time and controls the time to within several nanoseconds, as shown in Fig. 7, these signals cannot occur in real operation. In addition, the signals do not have any effect on the operation of the switching transistors because the operating state of the transistors cannot be changed in a short period of time. The output signals of the driver should be maintained at the same state for a certain period of time in order to change the state of the transistors. Because the signal variation for a short period of time is out of the operating frequency of the switching

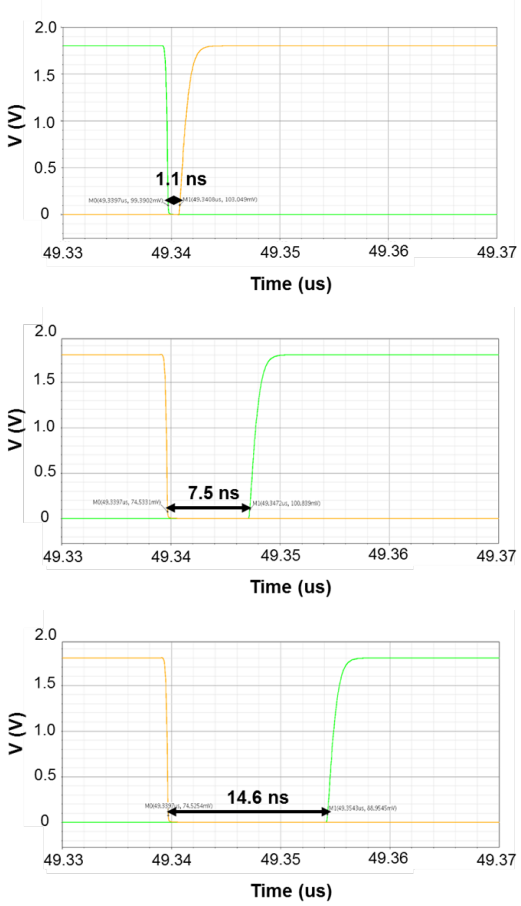

Fig. 7. Generated dead times using capacitance variation of the RC filter: (upper) $49.9\,fF$*, (middle)* $500\,fF$*, and (lower)* $1000\,fF$*.*

transistors, the transistors are not both simultaneously on.

The additional glitches shown in Fig. 8 (d) are generated from short pulses at the gate of the switching transistor shown in Fig. 8 (c). These pulses, which are called 'false triggers', are generated from large input capacitances of the switching transistors [15]. The process of pulse formation can be understood as follows: the electrical charges at the gate of the switching transistors are not totally discharged because of the insufficient reset time of the blocker. When false triggers are generated, the additional charge due to the triggers and the remains of the charge are summed up at the gate. The blocker accidentally operates if the sum is high enough to change the input state of the transistor. The glitches are caused by the lack of reset time at the output of the blocker and the generation of the false triggers. In Fig. 9, the glitches are seen not to occur in the case in which the output of the blocker remains in the reset state for a sufficiently long time. The reset time can be increased by using additional capacitors at the output of the blocker, as shown in Fig. 10. The problem of false triggers can be solved by appropriate design of the level shifters, such as the resonant gate driver [15].

The output power and the dc power consumption are almost the same for the two conditions because the power consumption when operating the breakdown blocker is negligible consumption in the power amplifier. As shown in Fig. 11, the output voltage spectrums are not much different whether the breakdown blocker is operating or not. For small differences of the harmonic level, the efficiency is nearly the same whether the breakdown blocker operating or not.

4 CONCLUSION

A gate driver IC with breakdown protection circuits is proposed for the power amplifiers of a tightly-coupled wireless power transfer system. The driver IC includes a dead-time generator, a level shifter, and a breakdown blocker; the driver IC is designed on a $600\,\mu\text{m} \times 550\,\mu\text{m}$ die area using TowerJazz's $0.18\,\mu$m BCD process. The optimum dead time, which leads to both operational stability and high efficiency in the amplifiers, can be obtained from by using the dead-time generator to precisely control the capacitance in the feedback path. The switching power cells can be prevented from temporary undesired operation at the gate inputs of the transistors by using a breakdown blocker. The operation and performance of the power amplifier with the gate driver are demonstrated using a circuit simulation that considers the effects of the layout. The proposed IC can improve the operation stability of the amplifier; it is also useful for applications of power transmitters, such as wireless power transfer systems, ultrasound therapy, medical devices, and LED drivers.

ACKNOWLEDGEMENTS

The author specially thanks In-Hye Kim and Young-Joon Song for technical assistance. This work was supported by the development software of the converged component technology of the Korea Evaluation Institute of Industrial Technology funded by the MKE (No. 10047687).

[1] M. K. Kazimierczuk, *RF Power Amplifiers*, John Wiley & Sons, 2008.

[2] A. Grebennikov, and N. O. Sokal, *Switchmode RF Power Amplifiers*, Newnes, 2007.

[3] J. Honda, and J. Adams, International Rectifier AN-1071, 2005.

[4] S. Hong, H.-J. Kim, J. Cheon, D.-H. Han, and K.-Y. Lee, "A novel dead-time generation method of clock generator for resonant power transfer system," in *Proceedings of the International SoC Design Conference*, (Seoul, Korea), pp. 51-54, November 2010.

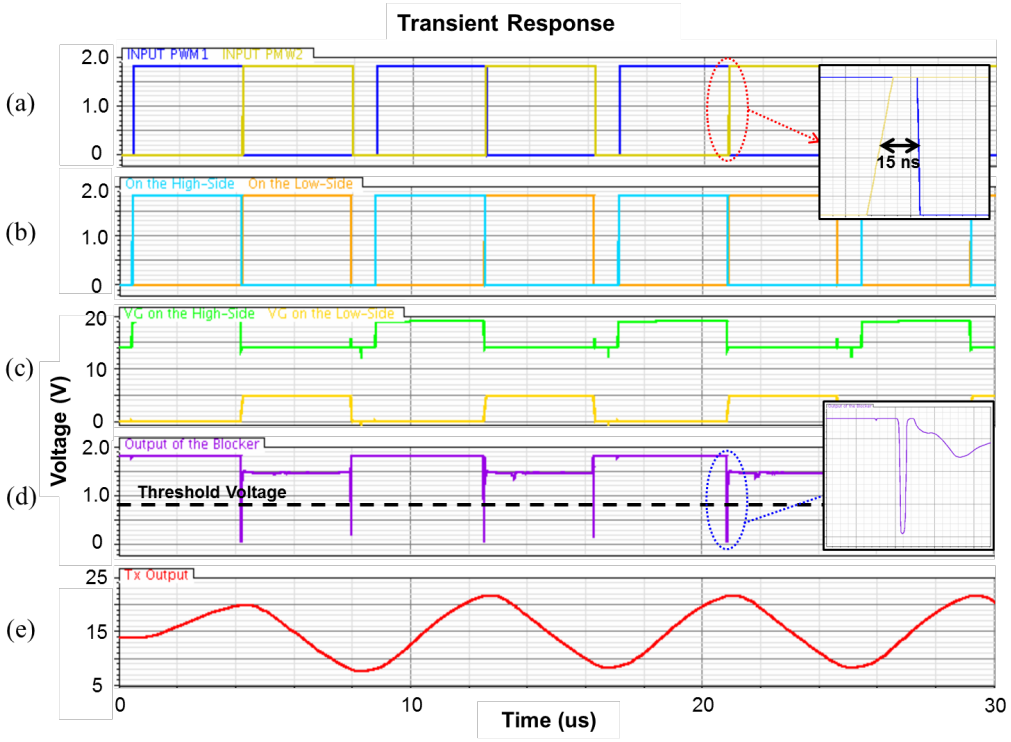

Fig. 8. Simulated voltage waveforms of the amplifier when 15 ns overlapping signals are connected to the output nodes of the dead-time generator: (a) Input overlapping signals, (b) inputs of the level shifters, (c) gate signals of the switching transistors, (d) output of the breakdown blocker, and (e) output of the amplifier. Block-box insets: Detail view of the input overlapping signals and the output of the blocker.

[5] I. D. Mosely, P. H. Mellor, and C. M. Bingham, "Effect of dead time on harmonic distortion in class-d audio power amplifier," *Electronics Letters*, vol. 35, no. 12, pp. 950-952, June 1999.

[6] K. Cho, S. Lee, and D. Kwon, "A high voltage half bridge gate driver with mismatch-insensitive dead-time generator," *IEICE Electronics Express*, vol. 9, no. 16, pp.1322-1328, 2012.

[7] S.-A. El-Hamamsy, "Design of high-efficiency RF class-D power amplifier," *IEEE Transactions on Power Electronics*, vol. 9, no. 3, May 1994.

[8] J. Strydom, and D. Reusch, Efficient Powre Conversion Corporation, *Dead-time optimization for maximum efficiency* (white paper), 2013, Retrieved from http://epc-co.com/epc/documents/papers/Dead-Time%20Optimization%20for%20Maximum%20Efficiency.pdf

[9] A. N. Laskovski, and M. R. Yuce, "Class-E oscillators as wireless power transmitters for biomedical implants," in *Proceedings of the International Symposium of Applied Sciences in Biomedical and Communication Technologies*, (Rome, Italy), pp. 1-5, November 2010.

[10] J.-R. Yang, H.-C. Son, and Y.-J. Park, "A class E power amplifier with coupling coils for a wireless power transfer system," *Progress In Electromagnetics Research C*, vol. 35, pp. 13-22, 2013.

[11] J.-R. Yang, J. Kim, and Y.-J. Park, "Class E power amplifiers using high-Q inductors for loosely coupled wireless power transfer system," *Journal of Electrical Engineering and Technology*, vol. 9, no. 2, pp. 569-575, March 2014.

[12] Wireless Power Consortium, WPC-ver.1.1.2, 2013, http://www.wirelesspowerconsortium.com.

[13] Power Matters Alliance, PMA-TS-0003-0, 2014, http://www.powermatters.org.

[14] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, 3rd edition, 2006.

[15] Y. Chen, F. C. Lee, L. Amoroso, and H.-P. Wu, "A resonant MOSFET gate driver with efficient energy recovery," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, March 2004.

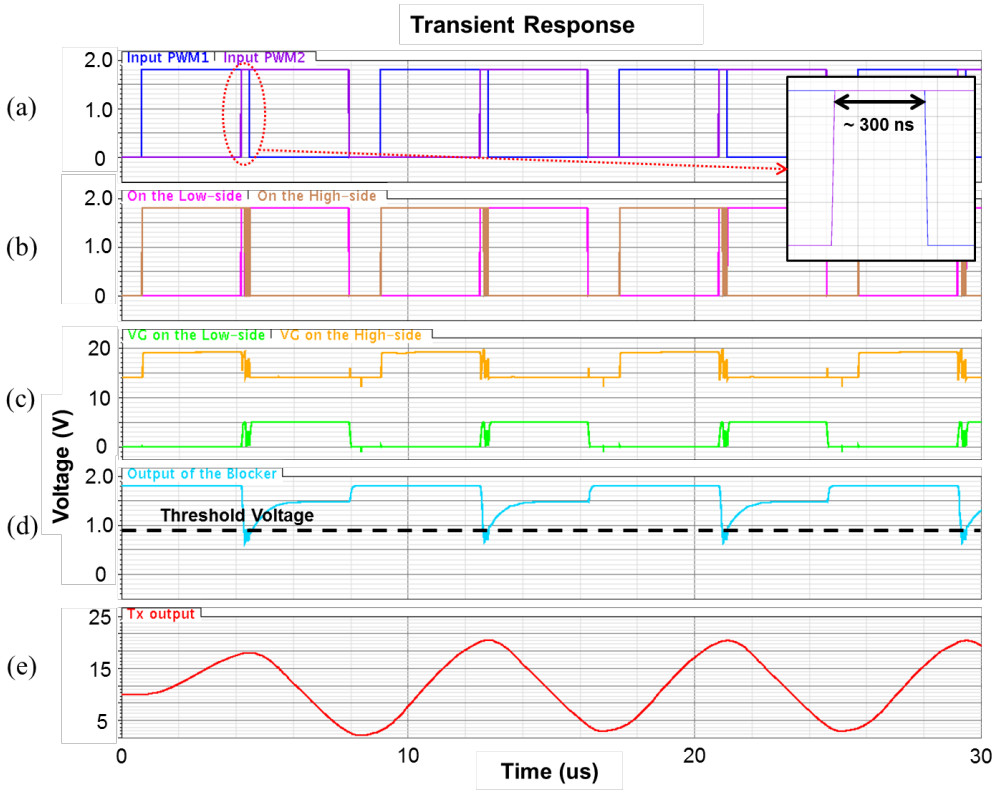

Fig. 9. Simulated voltage waveforms of the amplifier when 300 *ns overlapping signals are connected to the output nodes of the dead-time generator: (a) Input overlapping signals, (b) inputs of the level shifters, (c) gate signals of the switching transistors, (d) output of the breakdown blocker, and (e) output of the amplifier. Block-box inset: Detailed view of the input overlapping signals.*

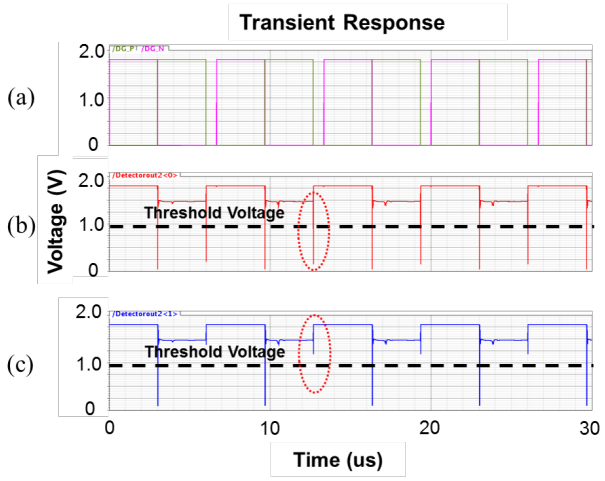

Fig. 10. Output voltage waveforms of the blocker depending on the value of the additional capacitance in the output node: (a) Input signals with overlapping time of 15 *ns, (b) output of the breakdown blocker without the additional capacitor, and (c) output with the capacitor of* 150 *fF.*

Jong-Ryul Yang received the B.S. degree in electrical engineering and material science from Ajou University, Suwon-city, Korea, in 2003, and the Ph. D. degree in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 2009. From Jan.2009 to Oct.2011, he was with the Mixed Signal Core Design Team, Samsung Electronics, Yongin, Gyeonggi, Korea. From Nov. 2011 to Aug. 2016, he was with the Converged Medical Device Research Center, Korea Electrotechnology Research Institute, Ansan, Gyeonggi, Korea. Since Sep. 2016, he has been with the Department of Electronic Engineering, Yeungnam University, Gyeongsan, Gyeongbuk, Korea. His research interests are Analog/RF/mmw/THz Integrated Circuits for miniaturized radar sensors, THz imaging systems, remote vital signal detectors, and wireless power transfer systems.

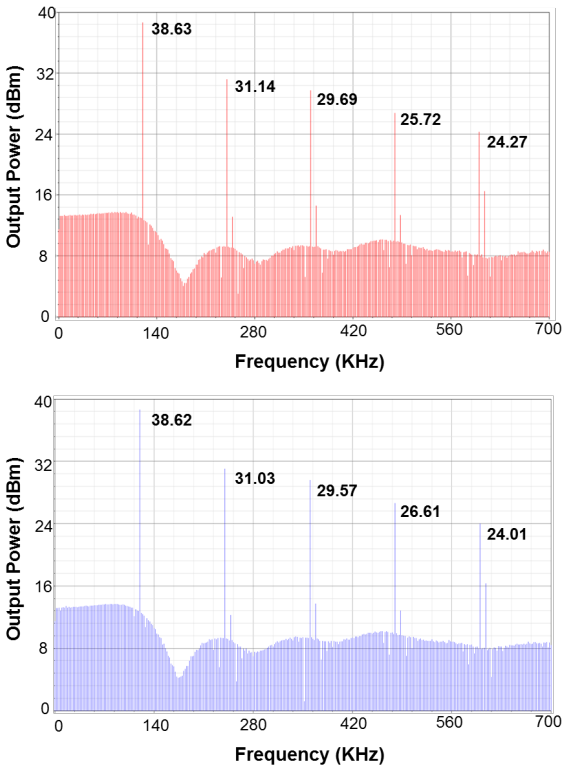

Fig. 11. Output power spectrum of the power amplifier: (upper) without the operation of the breakdown blocker and (lower) with the operation of the blocker.

AUTHORS' ADDRESSES
Prof. Jong-Ryul Yang, Ph. D.
Department of Electronic Engineering,
Yeungnam University,
280 Daehak-ro, Gyeongsan-si, Gyeongbuk-do,
38541, Korea.
email: jryang@yu.ac.kr

Received: 2014-09-24
Accepted: 2015-07-20