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Conventional and sub-threshold operation regimes of CMOS digital circuits

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Original scientific paper

In this paper a comparison of static and dynamic parameters of CMOS logic circuits operated in standard and sub-threshold regimes is presented. Analytic models of logic threshold voltage, logic delay and power consumption are derived for the sub-threshold operation regime. Certain analytic models analogies between these two regimes are shown. Threshold voltages of inverter, NAND and NOR logic circuits depend on the same parameters in both regimes. These circuits functional differences appear as a consequence of the drain current analytic model differences in the strong and weak inversion regimes. In both of these regimes, the inverter and transmission gate temperature characteristics are analyzed. Analytic models are verified by PSPICE simulation using the BSIM3 transistor models of the 0.18 μm CMOS technology process.

Key words: CMOS design methodology, sub-threshold, low-power, energy efficiency

Konvencionalni režim i režim slabe inverzije kanala CMOS digitalne logike. U ovome radu dana je usporedba statičkih i dinamičkih parametara CMOS logičkih krugova u standardnom režimu i režimu slabe inverzije kanala. Izvedeni su analitički modeli napona logičkog prada, logičkog kašnjenja i potrošnje električne energije u režimu slabe inverzije kanala. Prikazane su analogije analitičkih modela ovih parametara u oba režima. Naponi praga invertora, NI i NILI logičkih krugova ovise o istim parametrima u oba režima. Njihove funkcionalne razlike posljedica su razlika analitičkih modela struja odvoda MOS tranzistora u režimima jake i slabe inverzije. Analizirane su temperaturske karakteristike invertora i prijenosnog upravljačkog elementa u oba CMOS režima. Svi analitički modeli potvrđeni su PSPICE simulacijom primjenom BSIM3 tranzistorskog modela 0,18 μm CMOS tehnološkog procesa.

Ključne riječi: Metodologija projektiranja CMOS-a, režim slabe inverzije kanala, mala potrošnja, energetska efikasnost

1 INTRODUCTION

One of the greatest challenges for every digital system designer is to provide necessary performance along with the lowest possible consumption. In the last decade, the attention of both the researchers and the integrated circuits manufacturers is focused on the CMOS circuits operating in sub-threshold region. In this region, the supply voltage V_{dd} is less then the transistor threshold voltage V_t ($V_{ddsub} < V_t$). Thus, the drain current is decreased by several orders of magnitude, so that the short-circuit dissipation is decreased by more than 10^5 times compared to the standard CMOS regime. It is also, the reason why the operation speed is decreased by 10^3 times, compared to the standard region [1], [2], [3].

Nevertheless, such significant speed decrease is not always a limiting factor. Namely, there are applications where the CMOS circuits operating in sub-threshold region satisfy the speed demands. For example, the conversion of ambient energy present in the environment into electrical energy represents energy harvesting [4]. The primary interest in the technology derives from its capability to act as an independent power supply for wireless self-powered microsystems, as an alternative to, or to supplement the use of batteries. There are several ways to generate electrical energy locally, such as making use of the kinetic energy of vibrations widely present in the environment, photovoltaic or thermoelectric effects provided there is sufficient incident light or temperature gradient, respectively. Except for vibrations, there are other kinetic energy harvesting applications where the electrical power is generated from footstrikes, knee bends and backpacks [4] [5].

The application possibilites of the low power logic circuits are obvious. Since the energy harvester system takes a lot of time to collect enough energy from the environment, it is reasonable that the time interval needed for

data processing can last much longer than usual, up to microseconds or, even, miliseconds [4], [5].

This paper represents a continuation of the authors' research reported in [6]– [8]. Namely, in [6] it the analytic model of CMOS transistors working in the subthreshold regime was derived. In [7] low power CMOS circuits were treated, whereas in [8] a revew on energy efficient CMOS digital logic circuits was presented. In this paper the analysis is expanded to include the basic CMOS logic circuits parameters in standard and sub-threshold regime mathematical model comparison. It is shown that the complete analogy exists between the functional dependences of parameters in both CMOS operating regimes. Logic threshold voltage, delay time intervals and transmission gate on-resistance comparative temperature characteristics are provided. A complete transition dissipation analytical model for the standard operating regime is derived. As a consequence, we conclude that the power dissipation resulting from gate-source voltages ranging from zero to MOS transistor threshold voltage can not be neglected in the standard operating mode, especially when technology nodes lower than 100 nm are in question.

2 MOS TRANSISTOR CURRENT MODELS

When operating in strong inversion region, well-known simplified MOS transistor current model is used [9]. The MOS transistor drain current, when operating in sub-threshold region is given by [3]:

$$I_{dsub} = \begin{cases} I_0 e^{\frac{V_{gs}-V_t}{n\phi_t}} \left(1 - e^{-\frac{V_{ds}}{\phi_t}}\right), & V_{ds} < 3\phi_t \\ I_0 e^{\frac{V_{gs}-V_t}{n\phi_t}}, & V_{ds} > 3\phi_t \end{cases} \quad (1)$$

where, I_0 represents the drain current when $V_{gs} = V_t$, and is given by:

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) {\phi_t}^2. \quad (2)$$

The parameters in Eq. (2) are: μ_0 is the carrier mobility, $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance (ϵ_{ox} is the dielectric constant and t_{ox} is the gate oxide thickness), W and L are the channel width and length, V_t is the threshold voltage, $\phi_t = kT/q$ is the thermal potential ($\phi_t = 26$ mV at $300K$), and $n = 1 + C_d/C_{ox}$ is the sub-threshold slope factor.

According to Eq. (1), when $V_{ds} > 3\phi_t = 78$ mV the drain current I_{dsub} does not depend on the drain-source voltage (V_{ds}), because $e^{-3} \ll 1$. However, this dependance is exponential when $0 \leq V_{ds} \leq 3\phi_t$, Fig. 1. Thus, analogous to the strong inversion region operation, in sub-threshold there are two regions of the $I_{dsub} = f(V_{ds})$ characteristic: the saturation ($V_{ds} > 3\phi_t$) and non-saturation (linear) region ($0 \leq V_{ds} \leq 3\phi_t$). The difference is that the

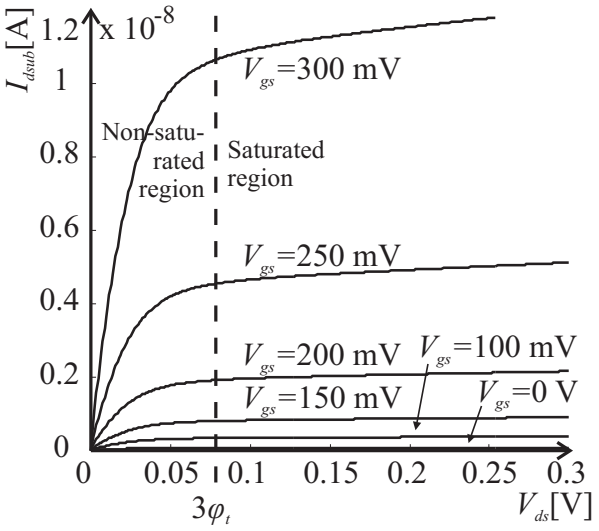

Fig. 1. MOS transistor $I_{dsub} - V_{ds}$ characteristics in sub-threshold operation region [3]

drain current in strong inversion is a quadratic function of the drain-source and the gate-source voltage, while in sub-threshold this function is exponential ($I_{dsub} \sim e^{V_{ds}, V_{gs}}$ in non-saturated and $I_{dsub} \sim e^{V_{gs}}$ in saturated region). Because there are saturation and non-saturation regions in the $I_d - V_{ds}$ characteristic, there are analogies in the operation, synthesis and analysis of the CMOS logic circuits in the sub-threshold and standard regimes.

3 CMOS LOGIC CIRCUITS STATIC CHARACTERISTIC ANALOGIES

In Fig. 2a a CMOS inverter is shown. CMOS operation region depends on the relation between supply voltage V_{dd} and nMOS and pMOS threshold voltages, V_{tn} and V_{tp} (in this paper, we assume $V_{tn} = |V_{tp}| = V_t$), while the transistor operation regime depends on the gate-source voltage

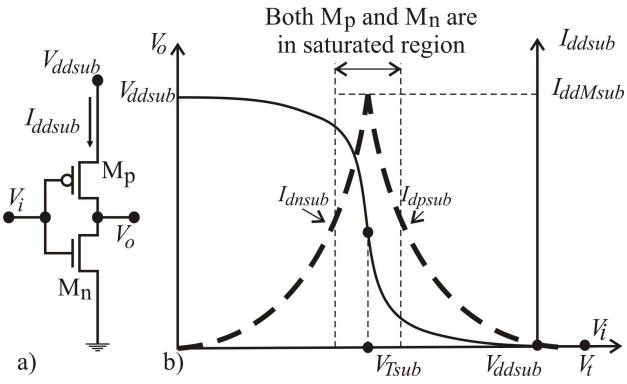

Fig. 2. CMOS inverter (a) and its $V_o - V_i$ and $I_{ddsub} - V_i$ static characteristics in sub-thresold region

to the threshold voltage ratio. Therefore, we need to distinguish the CMOS operation regime from the transistor operation regime. When $V_{dd} < V_t$, both nMOS and pMOS transistors operate in the weak inversion (sub-threshod) regime. This represents the CMOS sub-threshold operation regime. The standard (conventional) operation regime is when the inequality $V_{dd} > V_{tn} - V_{tp} = 2V_t$ is satisfied [10].

The MOS transistor threshold voltage V_t is the value of gate-source voltage which delimits weak and strong inversion (Fig. 2). In strong inversion operation regime we assume the transistor turned on when $V_{gs} > V_t$ and turned off at $V_{gs} < V_t$.

Even though the function $I_{dsub}(V_{gs})$ is exponential in the whole sub-threshold regime, because of the analogy with the strong inversion, it is convinient to define the sub-threshold regime operating transistor threshold voltage V_{tsub}. We assume that it is the gate-source voltage $V_{gs} = V_{tsub}$ at which the current I_{dsub} is 100 times less than its value at $V_{gs} = V_{ddsub}$, i.e. $I_{dsub}(V_{tsub}) = 0.01 I_{dsub}(V_{ddsub})$. Thus, we have:

$$V_{tsub} = V_{ddsub} - 4.6 \cdot n \times \phi_t. \tag{3}$$

When trasistor operates as a switch, it is considered turned off at $V_{gs} < V_{tsub}$ and turned on at $V_{tsub} < V_{gs} < V_{ddsub}$.

When operating in the standard regime, the CMOS inverter threshold voltage V_T and the maximum short-circuit current I_{ddM} are, respectively, given by:

$$\begin{aligned} V_T &= V_t + \frac{V_{dd} - 2V_t}{1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}}, \\ I_{ddM} &= \mu_n \frac{C_{ox}}{2} \frac{W}{L} \frac{(V_{dd} - 2V_t)^2}{\left(1 + \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}\right)^2}. \end{aligned} \tag{4}$$

Both voltage and current transfer characteristics of the CMOS inverter operating in sub-threshold regime are shown in Fig. 2b. Complete analogy with the corresponding characteristics of the standard regime is obvious. The threshold voltage V_{Tsub} in sub-threshold is obtained, in the same way as in standard regime, by equalizing currents $I_{dnsub} = I_{dpsub}$ in the saturated region of the characteristic, i.e. [6]– [7]:

$$I_{0n} e^{\frac{V_i - V_t}{n\phi_t}} = I_{0p} e^{\frac{-V_i + V_{dd} - V_t}{n\phi_t}}. \tag{5}$$

Replacing $V_i = V_{Tsub}$ in Eq. (5), and solving by V_{Tsub}, we obtain:

$$V_{Tsub} = \frac{V_{ddsub}}{2} - \frac{n\phi_t}{2} ln\left(\frac{I_{0n}}{I_{0p}}\right). \tag{6}$$

If the inverter is symmetric, i.e. if:

$$\frac{I_{0n}}{I_{0p}} = \frac{\mu_{0n} W_n / L_n}{\mu_{0p} W_p / L_p} = 1, \tag{7}$$

the threshold voltage is given as $V_{Tsub} = V_{ddsub}/2$. The threshold voltage of the symmetric CMOS inverter operated in standard region is also $V_T = V_{dd}/2$.

Supply voltage current is given as:

$$I_{ddsub} = \begin{cases} I_{0n} e^{\frac{V_i - V_t}{n\phi_t}}, & 0 \le V_i \le V_{Tsub} \\ I_{0p} e^{\frac{-V_i + V_{dd} + V_t}{n\phi_t}}, & V_{Tsub} \le V_i \le V_{dd} \end{cases} \tag{8}$$

where, $V_{dd} = V_{ddsub} < V_t$.

The maximum value of I_{ddsub} is obtained at $V_i = V_{Tsub}$, so:

$$I_{ddMsub} = I_{0n} \sqrt{\frac{I_{0p}}{I_{0n}}} \cdot e^{\frac{V_{ddsub}/2 - V_t}{n\phi_t}}. \tag{9}$$

Maximum short-circuit currents ratio of the symmetric CMOS inverter in the standard and sub-threshold operation regime, according to Eqs. (4), (7) and (9), at $V_t = 500$ mV, $V_{dd} = 2$ V, $V_{ddsub} = 350$ mV and $n = 1.5$, is $I_{ddM}/I_{ddMsub} = 0.22 \times 10^6$. In general, we can say that standard regime maximum current I_{ddM} is greater than that of sub-threshold I_{ddMsub} by 10^4 to 10^6 times.

Eqs. (6) and (9) show that the threshold voltage and the maximum short-circuit current of the CMOS inverter in sub-threshold region depend on the transistor geometry ratio $(W_n/L_n)/(W_p/L_p)$, just as is the case in the standard regime, Fig. 3. The difference is in the functional dependence and the parameter values.

NAND and NOR m-input circuits threshold voltages depend on the number of inputs m and the number of active inputs $1 \le k \le m$ [11]. In sub-threshold mode, just as in standard, inversion regime, m transistors in series can be replaced with one, channel length of which is mL. Also, k turned on transistors in parallel can be replaced with one, channel width of which is kW. NAND circuit threshold voltage is the lowest when the only active is the input at the gate of the nMOS transistor the source of which is grounded. In that case, the NAND threshold voltage is equal to the inverter threshold voltage, Eq. (3). When all the inputs are active ($k = m$), the m-input NAND circuit threshold voltage is at its maximum:

$$maxV_{Tsub} = \frac{V_{ddsub}}{2} - \frac{n\phi_t}{2} \ln\left(\frac{I_{0n}}{m^2 I_{0p}}\right). \tag{10}$$

The NOR circuit maximum threshold voltage is obtained when the only active is the input at the gate of the pMOS transistor the source of which is connected to the

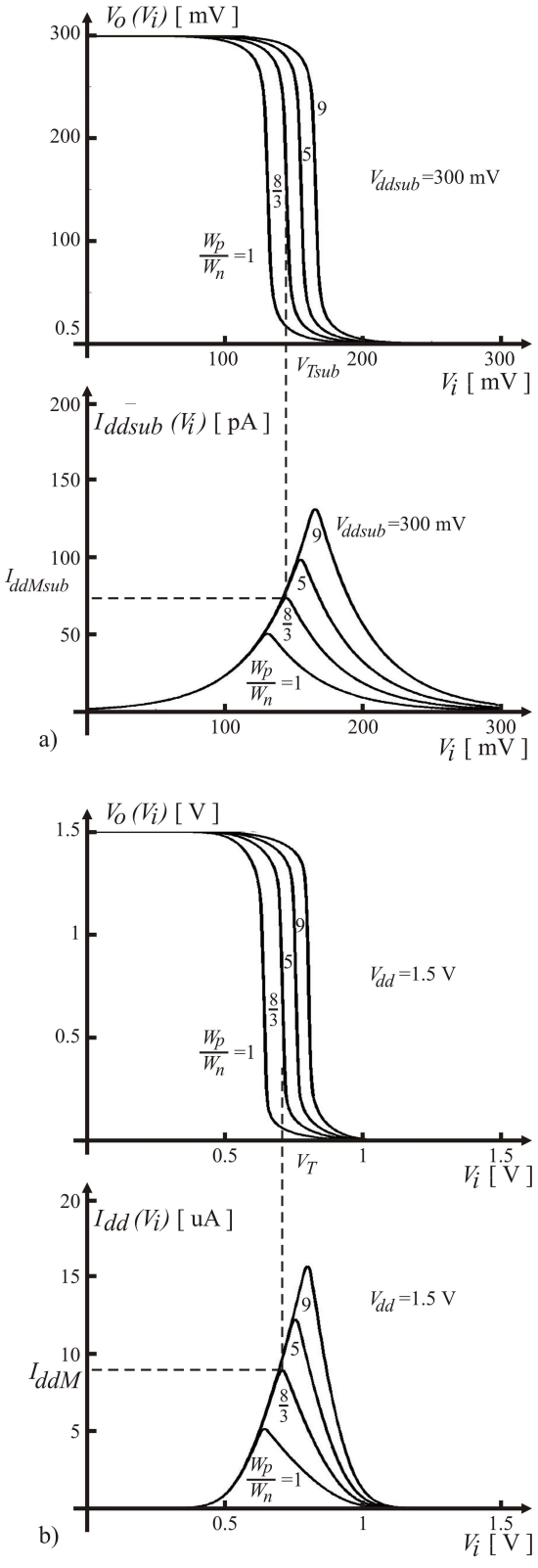

Fig. 3. CMOS inverter PSPICE voltage and circuit transfer characteristics in weak (a) and strong (b) inversion regime, where the ratio W_n/W_p is varied for the same $L_n = L_p$

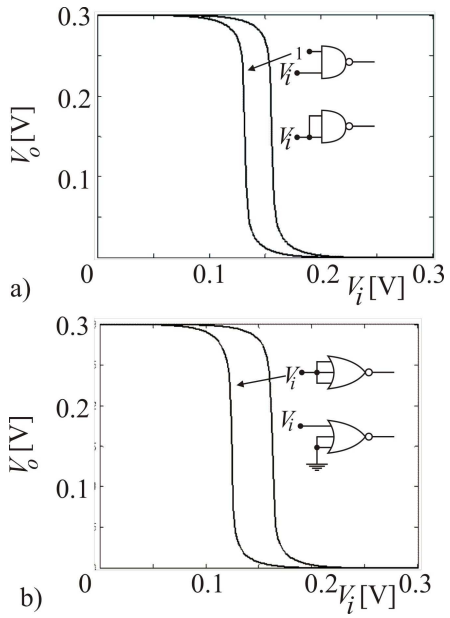

Fig. 4. NAND2 (a) and NOR3 (b) $V_o - V_i$ static characteristics in sub-threshold operation region when only one input is active and when all inputs are active at $V_{ddsub} = 300$ mV

supply voltage [11]. In sub-threshold operation mode it is given in Eq. (3). When all the inputs are active ($k = m$), m-input NOR circuit threshold voltage is at its minimum:

$$minV_{Tsub} = \frac{V_{ddsub}}{2} - \frac{n\phi_t}{2} \ln\left(\frac{m^2 I_{0n}}{I_{0p}}\right). \qquad (11)$$

PSPICE $V_o - V_i$ characteristics of NAND2 and NOR3 logic circuits with only one active and all inputs active are shown in Fig. 4. The nMOS and pMOS transistors are symmetric.

4 DYNAMIC MODEL

In Fig. 5a CMOS inverter and its parasitic capacitances are shown and in Fig. 5b, its model for switching process analysis is shown. In Eq. 12 capacitances C_{gdp} and C_{gdn} are mapped to the input and to the output, but with capacitance values doubled:

$$\begin{aligned} C_I &= C_{gsn} + C_{gsp} + 2\,(C_{gdn} + C_{gdp})\,, \\ C_o &= C_{dsn} + C_{dsp} + 2\,(C_{gdn} + C_{gdp})\,. \end{aligned} \qquad (12)$$

At step input voltage, when changing from 0 to V_{dd}, pMOS transistor is turned off (S_p off) and nMOS is turned on (S_n on), so the capacitor C_L is discharged by the current I_{dn}. The transistor M_n is first in saturated region and then in non-saturated region. The dynamic model shown in Fig. 5 is valid for both CMOS operation regimes.

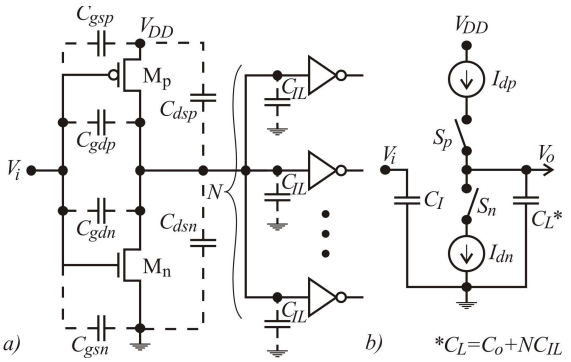

Fig. 5. CMOS inverter with corresponding capacitances (a) and its dynamic model (b) [6]

The output voltage fall time t_f of CMOS inverter operating in standard inversion regime is given by [9]:

$$t_f = \frac{C_L}{\beta_n \left(V_{dd} - V_{tn}\right)} \left(1.45 + \frac{V_{tn}}{V_{dd} - V_{tn}}\right). \quad (13)$$

On the falling edge of the input voltage, i.e. change from V_{dd} to 0, causes M_n to be turned off (S_n off) and M_p turned on (S_p on). Thus, C_L is charged by the current I_{dp}, so the output voltage rise time is given by:

$$t_r = \frac{C_L}{\beta_p \left(V_{dd} + V_{tp}\right)} \left(1.45 + \frac{|V_{tp}|}{V_{dd} + V_{tp}}\right), \quad (14)$$

where: $\beta_n = \mu_n \frac{C_{ox}}{2} \frac{W_n}{L_n}$ and $\beta_p = \mu_p \frac{C_{ox}}{2} \frac{W_n}{L_p}$.

In comparison to the rise (t_r) and fall (t_f) time intervals analytical models provided in [6], in this paper the derivation is extanded to include the non-saturated operating area of the $I_{dsub} - V_{ds}$ MOS transistor characteristic. Namely, the operating point trajectory in the sub-threshold operation regime is the same as in the standard operation regime, Fig. 6. In the beginning of the switching regime, the operating point is in saturation, and in the end it is in the linear region. The new derived model is more precise in the context of the rise (t_r) and fall (t_f) time intervals temperature characteristic analysis.

Let us assume a step function from 0 to V_{ddsub} for the input voltage. In that case, the transistor M_p is turned off, so C_L is discharged by the drain current of the turned on M_n. The discharge time consists of two intervals. In the first of those, M_n operates in saturation so:

$$\begin{aligned} V_o(t) &= V_{ddsub} - \frac{1}{C_L}\int_0^t I_{dn} dt = \\ &= V_{ddsub} - \frac{I_{0n}}{C_L} e^{\frac{V_{ddsub} - V_t}{n\phi_t}} t. \end{aligned} \quad (15)$$

Setting up the condition $V_o(t_{fsub1}) = 3\phi_t$, we obtain:

$$t_{fsub1} = C_L \frac{V_{ddsub} - 3\phi_t}{I_{0n}} e^{\frac{V_t - V_{ddsub}}{n\phi_t}}. \quad (16)$$

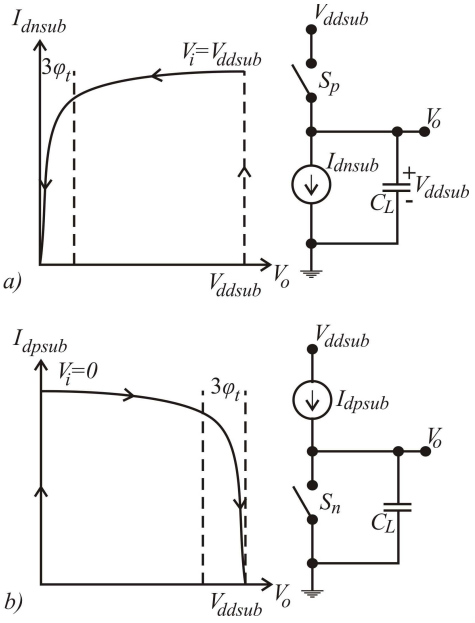

Fig. 6. Sub-threshold mode operating points trajectory and the equivalent circuits to charge (a) and discharge C_L (b)

In linear region, we have:

$$V_o(t) = 3\phi_t - \frac{1}{C_L}\int_0^t I_{0n} e^{\frac{V_{ddsub} - V_t}{n\phi_t}} (1 - e^{-\frac{V_o}{\phi_t}}) dt. \quad (17)$$

Since $V_o = f(t)$, we first calculate the derivate in Eq. (17) and then:

$$\int_{3\phi_t}^{V_o} \frac{dV_o}{1 - e^{-\frac{V_o}{\phi_t}}} = -\frac{dV_o}{C_L} e^{\frac{V_{ddsub} - V_t}{n\phi_t}} \int_0^t dt. \quad (18)$$

Assuming $e^3 \gg 1$, the solution to Eq. (18) is given as:

$$t = C_L \frac{\phi_t}{I_{0n}} e^{\frac{V_{ddsub} - V_t}{n\phi_t}} \left[3 - ln(e^{\frac{V_o}{\phi_t}} - 1)\right]. \quad (19)$$

The switching regime is finished when $V_o = 0$. However, at $V_o = 0$ the Eq. (19) is undetermined. Therefore, just like in the standard CMOS operation mode, we assume that t_{fsub2} is the time after which V_o is equal to 10% of its value at the border of the saturated and linear region $I_{dnsub} - V_{ds}$ characteristics of nMOS transistor, i.e.:

$$V_o(t_{fsub2}) = 0.1 \times 3\phi_t. \quad (20)$$

Combining Eqs. (18) and (20), yields:

$$t_{fsub2} \approx C_L \frac{\phi_t + 3\phi_t}{I_{0n}} e^{\frac{V_t - V_{ddsub}}{n\phi_t}}. \quad (21)$$

The total output voltage fall time is:

$$\begin{aligned} t_{fsub} &= t_{fsub1} + t_{fsub2} = \\ &= C_L \frac{V_{ddsub} + \phi_t}{I_{0n}} e^{\frac{V_t - V_{ddsub}}{n\phi_t}}. \end{aligned} \quad (22)$$

The rise time is calculated in the same way, and we obtain:

$$t_{rsub} = t_{rsub1} + t_{rsub2} = = C_L \frac{V_{ddsub} + \phi_t}{I_{0p}} e^{\frac{V_t - V_{ddsub}}{n\phi_t}}. \quad (23)$$

For the inverter input pulse period needs to be valid: $T \geq t_f + t_r$, so that its maximum working frequency $F = 1/T_{min}$ in the standard CMOS regime is a linear function of $V_{dd} - V_t$, $F_M \sim (V_{dd} - V_t)$. In the sub-threshold region, this dependence is exponential, $F_{subM} \sim e^{(V_{ddsub} - V_t)}$. In Fig. 7, normalized F_M and F_{Msub} (relative to the process constant, $\mu_0 C_{ox} W/L$) values are shown. The maximum working frequency in the standard operation mode is greater by several orders of magnitude, e.g. for $C_L = 1$ fF, $V_{dd} = 1.5$ V and $V_{ddsub} = 400$ mV, we obtain $F_M > 10^4 F_{Msub}$

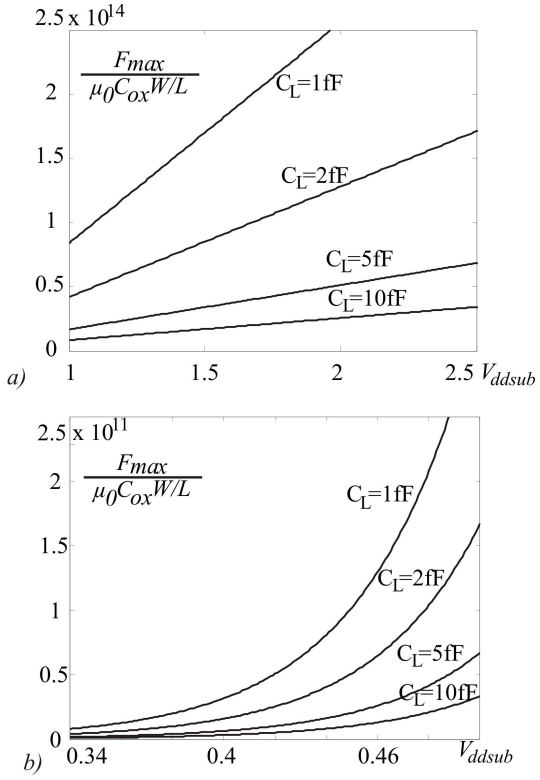

Fig. 7. Normalized F_{max} as a function of V_{dd}, shown for different values of C_L, when operating in strong (a) and weak (b) inversion region

5 TEMPERATURE CHARACTERISTICS

The MOS transistor threshold voltage, the carrier mobility and the thermal potential yield the dominant influence to the CMOS temperature characteristics. The V_{tn} and V_{tp} dependence on the temperature change is approximately linear, and dependence for μ_n and μ_p is approximately exponential [12]. In [12] it is demonstrated that the CMOS inverter threshold voltage, V_T, in the standard operation mode is a linear function of temperature. The temperature coefficient dV_T/dT depends on V_{dd} and on the transistor geometry ratio, $\beta_R = \beta_n/\beta_p$. If $\beta_R < 1$, $dV_T/dT > 0$, and at $\beta_R > 1$, $dV_T/dT < 0$.

The CMOS inverter threshold voltage in sub-threshold regime, Eq. (3) is also approximately a linear function of temperature. Namely, the temperature dependence of the current ratio I_{0n}/I_{0p} is proportional to μ_n/μ_p. Since the temperature coefficients are approximately equal, then: $I_{0n}/I_{0p} \neq f(T)$. Therefore:

$$\frac{dV_{Tsub}}{dT} \approx -\frac{n\phi_t}{2T} ln(\frac{I_{0n}}{I_{0p}}) \lessgtr 0. \quad (24)$$

Hence, in the sub-threshold regime, the threshold voltage thermal coefficient can be less than, equal to or greater than zero, in dependence on nMOS and pMOS transistor geometries. In Fig. 8 a relative change of V_{Tsub} as a function of temperature and pMOS and nMOS channel widths ratio (W_p/W_n) is shown, at equal channel lengths ($L_n = L_p$). If the transistors are symmetric ($W_p/W_n = \mu_n/\mu_p$), then we have: $dV_{Tsub}/dT = 0$. Such conclusions are valid also for the threshold voltage V_T in the standard operation mode [12].

The CMOS inverter logic delay in the standard operation mode is almost linear function of temperature (Fig. 9a), whereas it is exponential in the sub-threshold regime (Fig. 9b). The logic delay thermal coefficient in the standard regime is positive, while it is negative in sub-threshold.

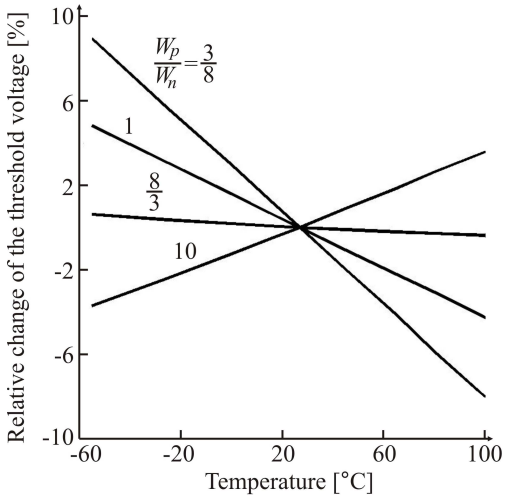

Fig. 8. CMOS inverter threshold relative change as a function of temperature for different ratios W_p/W_n (sub-threshold mode)

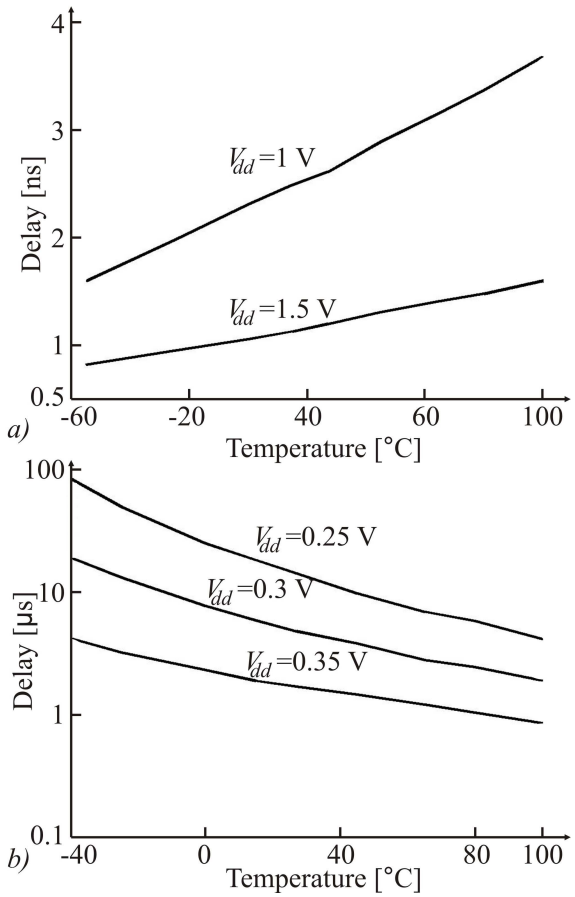

Fig. 9. The symmetric CMOS inverter delay as a function of temperature and supply voltage in: standard operation mode (a) and sub-threshold regime (shown in logarithmic scale) (b), at C_L=20 fF. The results are obtained by PSPICE circuit analysis

6 DISSIPATION

The CMOS logic circuits have two energy consumption components: static (standby) and active (dynamic) [10]. The static consumption for both operation modes is a consequence of the MOS transistor currents in the static states and it is given by:

$$P_{ddS} = V_{dd} I_S, \tag{25}$$

where I_S represents total static current.

There are four main static current sources in CMOS circuits [10]:

- gate tunnel current (I_g),
- sub-threshold drain current (I_{dsub}),
- reversed bias pn junction saturation current (I_{dSS}),
- hot carriers gate current (I_H).

The first two components dominate the static dissipation of the CMOS circuit in nanometer technologies. The gate current I_g exists when the transistor conducts. Namely, the MOS transistor dimension scaling decreases the oxide thickness (t_{ox}) under the gate. Therefore, the electric field in the gate oxide increases, which leads to carrier tunneling from the gate to the bulk and vice-versa. The gate current consists of four components: gate-channel (I_{gc}), gate-drain (I_{gd}), gate-source (I_{gs}) and gate-body (I_{gb}). Total gate current is given by:

$$I_g = I_{gd} + I_{gb} + I_{gs} + I_{gc}. \tag{26}$$

The gate currents depend on the supply voltage V_{dd} and the technology process as shown in Table 1, [13]. Therefore, the supply voltage increase from $V_{dd} = 0.2$ V to $V_{dd} = 1.2$ V, leads to the gate current increase of 1.4×10^3 times. The transistor dimensions decrease also leads to the gate current increase. For an nMOS transistor, according to the Table 1, the gate current increase for the 45 nm technology process in comparison to the 65 nm process is 7 (at $V_{dd} = 1.2$ V) to 14 times (at $V_{dd} = 0.2$ V).

The nMOS transistor leakage gate current is larger (up to 40 times) than that of the pMOS transistor, because the electron tunneling probability through the gate oxide is much greater than the holes tunneling probability.

When the transistor is turned off, i.e. $V_{gs} = 0$, there exists a sub-threshold leakage drain current and it is given as:

$$I_{dleak} = I_0 e^{\frac{\eta V_{dd} - V_t}{n\phi_t}}. \tag{27}$$

where η represents DIBL (Drain-Induced Barrier Lowering) factor [14]. This current also depends on the supply voltage, transistor size (the technology process) and the temperature. In Table 2 gate and sub-threshold drain currents are given as functions of the supply voltage V_{dd} and the temperature for the 45 nm technology. Observing Table 2, we see that the I_g dependence on V_{dd} is stronger, whereas I_{dleak} shows stronger dependence on the temperature. On the other hand, at the temperature of 25 °C, for $V_{dd} \leq 0.6$ V we get: $I_g < I_{dleak}$, while for $V_{dd} > 0.6$ V we get: $I_g > I_{dleak}$. Thus, for example, at $V_{dd} = 1.2$ V, $I_g \approx 13 \times I_{dleak}$

The reversed bias pn junction saturation current of the transistor turned off depends on the junction area and the temperature. Per unit area its value is between 10 and 100 pA/μm^2 at the temperature of 25 °C when 0.25 μm technology process is used. In nanometer techonologies this current is much lower than I_g and I_{dleak}, so it can be neglected [10], [15].

Active (dynamic) dissipation also consists of two components: switching and short-circuit dissipation. The

V_{dd}	I_g	
[V]	45 nm	65 nm
0.2	1.996 nA	85.506 pA
0.4	14.258 nA	1.2376 pA
0.6	66.954 nA	6.5488 nA
0.8	225.97 nA	25.244 nA
1.0	647.38 nA	82.378 nA
1.2	1.6811 μA	243.21 nA

Table 1. The two different technology process nMOS transistor gate currents as a function of the supply voltage [13]

V_{dd}	I_g [nA]		I_{dleak} [μA]	
[V]	25 °C	110 °C	25 °C	110 °C
0.2	1.996	1.2689	40.999	0.88086
0.4	14.258	15.776	56.493	1.1586
0.6	66.954	75.437	72.47	1.4401
0.8	225.97	256.33	89.397	1.7334
1.0	647.38	736.31	107.42	2.0428
1.2	1681.1	1914.3	127.12	2.3785

Table 2. The nMOS transistor gate and sub-threshold leakage drain currents as functions of the supply voltage and the temperature [13]

switching dissipation P_{dsw} is a consequence of the capacitive load C_L charging and discharging. In both standard and sub-threshold operation modes:

$$P_{dsw} = C_L V_{dd}^2 f, \tag{28}$$

where $f = 1/T$ represents the input pulses frequency. Thus, switching dissipation, in both operating regimes, is proportional to ${V_{dd}}^2$. Since V_{dd} is several times greater than V_{ddsub}, the switching dissipation of the standard operation mode is greater by several tens of times.

The above analysis is valid when ideal input voltage and ideal MOS transistors are considered. In practice, there are always input voltage rise and fall times. These are the reasons why, during the transition, both transistors are turned on, causing additional dissipation. The CMOS inverter transition dissipation in the standard operation regime consists of two components: the sub-threshold dissipation ($0 < V_i < V_{tn}$ and $V_{dd}+V_{tp} < V_i < V_{dd}$) and the short-circuit dissipation ($V_{tn} < V_i < V_{dd} + V_{tp}$), Fig. 10a.

According to Fig. 10b, supply power current $I_{dd}(t)$ is:

$$I_{dd} = \begin{cases} I_{dnsub}, & 0 < t < t_1 \text{ and } t_8 < t < t_9 \\ I_{dpsub}, & t_3 < t < t_4 \text{ and } t_5 < t < t_6 \\ I_{dn}, & t_1 < t < t_2 \text{ and } t_7 < t < t_8 \\ I_{dp}, & t_2 < t < t_3 \text{ and } t_6 < t < t_7, \end{cases} \tag{29}$$

where I_{dsub} and I_d are MOS transistor currents in saturation for sub-threshold and standard regime, respectively.

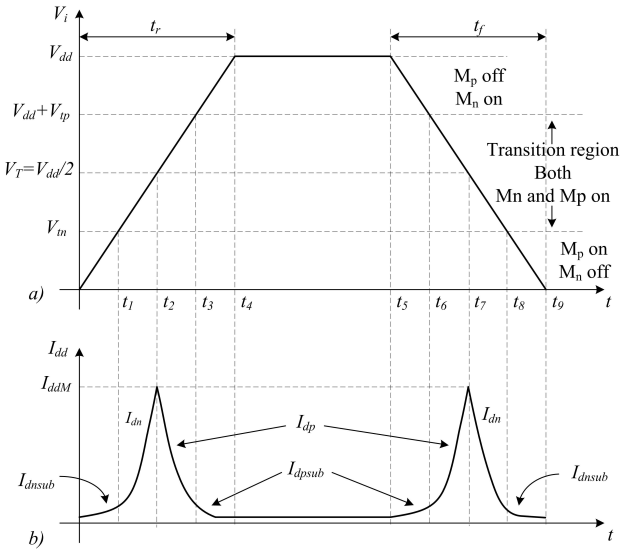

Fig. 10. The CMOS inverter transistor states (a) and the supply voltage current (b) at $0 \leq V_i \leq V_{dd}$ (standard operation mode)

Total transition dissipation for one period, T, is given as:

$$P_{dt} = \frac{1}{T} \int_0^T V_{dd} I_{dd}(t) dt. \tag{30}$$

Sub-threshold transition dissipation for the interval $0 < t < t_1$, during which the transistor M_n is in sub-threshold regime, is given as:

$$P_{dtsub} = \frac{V_{dd}}{T} \int_0^{t_1} I_{0n} e^{\frac{V_i - V_t}{n\phi_t}} dt. \tag{31}$$

Observing Fig. 10a, the input voltage is $V_i = (V_{dd}/t_r) \cdot t$, so that from the Eq. (31):

$$P_{dtsub} = \frac{n\phi_t t_r I_{0n}}{T} e^{-\frac{V_t}{n\phi_t}} \left[e^{\frac{V_{dd}}{n\phi_t} \cdot \frac{t_1}{t_r}} - 1 \right]. \tag{32}$$

From $V_i(t_1) = V_t$ we obtain $t_1 = (V_{tn}/V_{dd}) \cdot t_r$ and including it in Eq. (32), the final expression of P_{dtsub} is:

$$P_{dtsub} = n\phi_t I_{0n} \left(1 - e^{-\frac{V_t}{n\phi_t}} \right) t_r f. \tag{33}$$

The same expression is valid in the interval $t_8 < t < t_9$, if we replace t_r with t_f. For the intervals $t_3 - t_4$ and $t_5 - t_6$, during which M_n is on and the M_p is in sub-threshold operation regime, I_{0n} in Eq. (33) should be replaced with I_{0p}. If the transistors are symmetric ($I_{0n} = I_{0p} = I_0$), total sub-threshold transition dissipation is:

$$P_{dtsub} = 2n\phi_t I_0 \left(1 - e^{-\frac{V_t}{n\phi_t}} \right) f \left(t_r + t_f \right). \tag{34}$$

In the transition region, where both transistors are turned on, I_{dn} and I_{dp}, are the drain currents of the nMOS and the pMOS transistors, respectively. The short-circuit dissipation is given as:

$$P_{dtsc} = \frac{I_{ddM}}{3}\left(V_{dd} - 2V_t\right) f\left(t_r + t_f\right), \qquad (35)$$

where I_{ddM} is given by Eq. (4). There it is shown that $I_{ddM} \sim (V_{dd} - 2V_t)^2$, hence we have $P_{dtsc} \sim (V_{dd} - 2V_t)^3$.

Total transition dissipation is given as $P_{dt} = P_{dtsub} + P_{dtsc}$, thus, taking into account Eqs. (34) and (35), we obtain:

$$\begin{aligned} P_{dt} &= \left[2n\phi_t I_0\left(1 - e^{-\frac{V_t}{n\phi_t}}\right) + \right. \\ &+ \left. \frac{I_{ddM}}{3}\left(V_{dd} - 2V_t\right)\right] \cdot f\left(t_r + t_f\right) \end{aligned} \qquad (36)$$

Supply voltage current response in the sub-threshold regime to an input voltage linear change is shown in Fig. 11. To calculate the P_{dtwi} dissipation using Eq. 30, instead of V_{dd} and I_{dd}, we use V_{ddsub} and I_{ddsub}, respectively, where $I_{ddsub} = I_{dnsub}$ for time intervals of $0 \le t \le t_1$ and $t_2 \le t \le T$, and $I_{ddsub} = I_{dpsub}$ for time interval of $t_1 \le t \le t_2$, 11. The currents I_{dnsub} and I_{dpsub} are the drain currents of the nMOS and the pMOS transistors in saturated region, respectively. If the inverter is symmetric, then $I_{dnsub} = I_{dpsub}$.

Thus, the dissipation is equal for all periods: $0 < t < t_1$, $t_1 < t < T/2$, $T/2 < t < t_2$ and $t_2 < t < T$. Furthermore, we have:

$$\begin{aligned} P_{dtwi} &= 4\frac{V_{ddsub}}{T}\int_0^{t_1} I_{dnsub}\left(t\right) dt = \\ &= 4\frac{V_{ddsub}}{T} I_{0n}\int_0^{t_1} e^{\frac{St - V_t}{n\phi_t}} dt, \end{aligned} \qquad (37)$$

where $S = dV_i/dt$ represents the input voltage slope changes. When the input signal is symmetric, we have: $|S| = V_{dd}/t_r = V_{dd}/t_f$, where t_r and t_f are rise and fall times of the input voltage, respectively. Solving Eq. (37), yields:

$$P_{dtwi} = 2n\phi_t I_{ddMsub}\left(t_r + t_f\right) f, \qquad (38)$$

where I_{ddMsub} is given by Eq. (9).

Comparing the Eqs. (34) and (38) we conclude that the sub-threshold transition dissipation in the standard CMOS mode is much greater than the total transition dissipation in the sub-threshold operation regime. Their ratio is usually several tens to several hundreds. However, the ratio of the standard regime short-circuit dissipation to P_{dtwi} is much greater, because $P_{dtsc} \sim (V_{dd} - 2V_t)^3$,

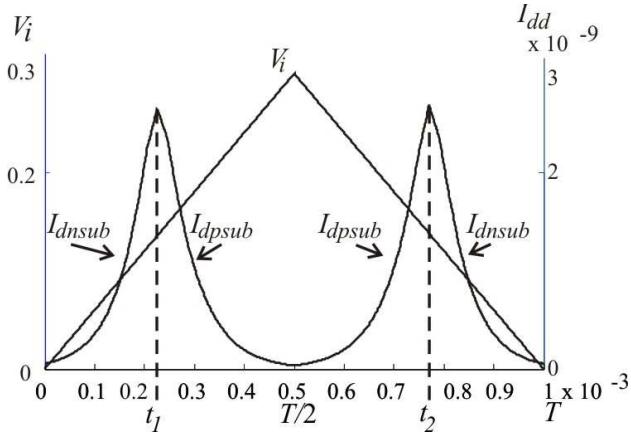

Fig. 11. CMOS inverter supply voltage current response to an input voltage linear change, when operating in sub-threshold [6]

and $P_{dtwi} \sim \phi_t^3 e^{V_{ddsub} - 2V_t}$. For example, if $V_{dd} = 2$ V, $V_t = 0.5$ V, $n = 1.5$ and $V_{ddsub} = 360$ mV, for the symmetric inverter we calculate $P_{dtsc}/P_{dtwi} \sim 4.7 \times 10^6$.

7 TRANSMISSION GATE

The transmission gate consists of the CMOS transistors drain-source parallel connection, with the opposite phase drives. When turned on, its resistivity is equal to the turned on nMOS and pMOS transistors' resistance in parallel. For the resistance of a MOS transistor operating in the standard mode the relation: $R_d \sim 1/(V_{gs} - V_t)$ is widely known. In sub-threshold operation regime, the resistance is:

$$R_{dsub} = \left(\frac{dI_{dsub}}{dV_{ds}}\right)^{-1}\Bigg|_{V_{ds}=0} = \frac{\phi_t}{I_0} e^{\frac{V_t - V_{gs}}{n\phi_t}}. \qquad (39)$$

The transistors gate source voltages: $V_{gsn} = V_{dd} - V_i$ and $V_{gsp} = -V_i$ depend on the input voltage, so the resistivities R_d and R_{dsub} are functions of V_i. In sub-threshold regime:

$$\begin{aligned} R_{dnsub} &= \frac{\phi_t}{I_{0n}} e^{\frac{V_t - V_{dd} + V_i}{n\phi_t}} \\ R_{dpsub} &= 4\frac{\phi_t}{I_{0p}} e^{\frac{V_t - V_i}{n\phi_t}}. \end{aligned} \qquad (40)$$

In both operating regimes, the resistance of the turned on transmission gate depends on the input voltage and on temperature, Fig. 12. The characteristics in Fig. 12 are obtained by PSPICE analysis of the 0.18 μm technology process symmetric transistors. In standard regime $dR_{on}/dT > 0$, while in sub-threshold the resistance thermal coefficient is negative, i.e. $dR_{onsub}/dT < 0$.

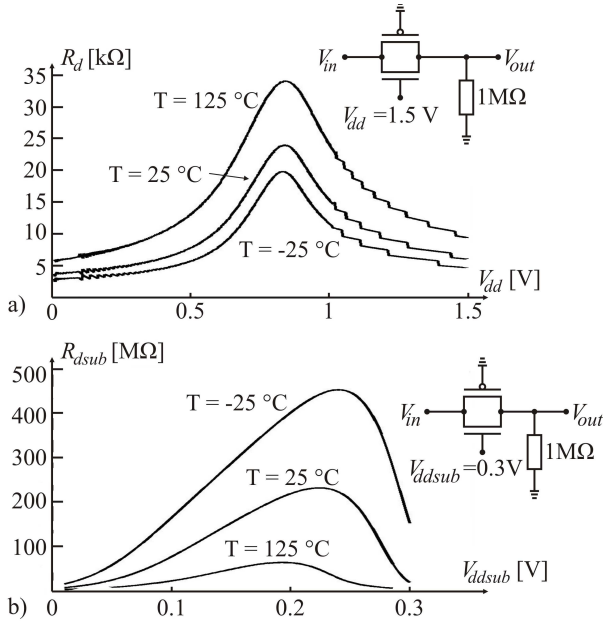

Fig. 12. The transmission gate resistance temperature dependence in standard operation mode at $V_{dd} = 1.5$ V (a) and in sub-threshold at $V_{ddsub} = 300$ mV (b) obtained by PSPICE analysis

8 CONCLUSION

Analysis results show complete analogy in behaviour of standard and sub-threshold operating modes. The logic circuits threshold voltage depends on, besides the supply voltage, transistor geometry ratio. Only the functional dependence is different; namely, in the saturation region of the standard operating regime, the drain current characteristic is a quadratic function of the gate-source voltage and, therefore, the logic threshold voltage is a square root function of the transistors' geometries ratio. On the other hand, in the sub-threshold operating mode, the $I_d - V_{gs}$ characteristic is an exponential function, thus making the logic threshold voltage a logarithmic function of the transistors' geometries ratio. In both operation modes, threshold voltage of the symmetric inverter is equal to half the supply voltage.

In both regimes, the NAND and NOR circuits static transfer characteristic depends on the number of active inputs. The transition dissipation is proportional to ${V_{dd}}^3$ in the standard and to ${\phi_t}^3 e^{V_{ddsub}}$ in the sub-threshold regime. Thus, sub-threshold transition dissipation is 10^5 to 10^6 times less than the standard regime dissipation. Maximum inverter operation frequency, while operating in sub-threshold, is 10^3 to 10^4 times less than frequency while operating in the standard region. This frequency is proportional to $e^{V_{ddsub}}$ in sub-threshold, and to V_{dd} in standard region.

The logic threshold voltage (V_T) temperature coefficient depends on the nMOS and pMOS transistors geometry ratio in both regimes. Its value is zero when the transistors are symmetric. The logic delay temperature sensitivity is much larger in the sub-threshold operation regime.

The transmission gate resistivity variance with temperature is several times larger in the sub-threshold operation mode. That variance is positive with temperature in the standard and negative in the sub-threshold regime.

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