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Original scientific paper

A Three Phase Interleaved Boost Converter with L & C Voltage Extension Mechanism

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Abstract: In this paper a high step-up dc-dc voltage converter is proposed. The proposed converter employs coupled inductors and voltage extension capacitors for obtaining a high voltage gain. The coupled inductors and extension capacitors are merged in traditional interleaved boost converters to get the additional advantage of high step-up voltage conversion ratio and reduced voltage stress on switches along with existing features of interleaved boost converters. The main operating principle of the proposed converter is discussed and the key principle waveforms and equations are analysed. A simulation in PSIM is carried out for the proposed converter as well as traditional interleaved boost converter for the same parameters which shows that the proposed converter has better performance as compared to the traditional interleaved boost converter. Finally, an experiment is carried on a 32 W, 20 V input, 160 V output prototype in the laboratory for experimental validation of the proposed converter. Important future directions have also been given for future research on the proposed topology.

Keywords: boost converter; coupled inductors; interleaved; switch stress; voltage conversion ratio

1 INTRODUCTION

Renewable energy sources are becoming more and more popular due to low maintenance and less pollution. Most of the renewable energy sources generate power at low dc voltages and therefore a high step-up dc-dc voltage conversion is needed as in case of photovoltaic and fuel cells. The traditional boost converter does not meet this requirement as it must operate at very low duty cycle and there is a very high voltage stress across its semiconductor switches. During the last two decades increased research has been carried out on power electronics converters and especially a lot of research has been done on high step-up dc-dc converter topologies [1-4].

A cascaded/two stage boost converter which uses two boost converters in series is used to achieve high step-up voltage gain. However, the overall efficiency is the product of the efficiencies of two converters and is low [5, 6]. Quadratic boost converters which simplify the cascaded boost into a single switch structure are used to achieve the high step-up voltage conversion ratio. The voltage gain is equal to the product of the gains of two boost converters [7, 8]. A three level boost converter is presented in [9, 10]. Three level boost converter offers the advantage of reducing the voltage stresses across the semiconductor switches, but does not improve the voltage gain.

High step-up converters with voltage multiplier cells are presented in [11-13]. This method uses voltage multiplier cells to achieve high step-up voltage conversion ratio. Each cell is made of two capacitors and two diodes. However, for high voltage gain several numbers of cells are required. Coupling the inductors among the phases of interleaved boost converters reduces the current ripples and also helps in obtaining high step-up voltage conversion ratio. However, the existence of leakage inductance can cause large voltage overshoots [14]. Switched capacitor step-up converters can also achieve high voltage gain, however the efficiency of switched capacitor circuits is very low [15].

To get a high step-up voltage conversion ratio a new topology of dc-dc converter is presented in this paper. The idea is obtained by using coupled inductors and voltage extension capacitors in the traditional interleaved boost converter. This helps in additional advantages of high voltage gain and reduced voltage stress of switches along with existing features of interleaved topologies. Fig. 1(b) shows the circuit diagram of the proposed converter. It is a three phase interleaved boost converter with coupled inductors in the first phase and an extension capacitor in each second and third phase. In the proposed technique coupled inductors with turn ratio of x are always used in the first phase and extension capacitors are used in the rest of phases. The number of extension capacitors is $(m-1)$, where m is the number of phases. The idea can be implemented for more than three phases. Increasing x and m will increase the voltage conversion ratio to a higher degree. Fig. 1(a) and 1(c) shows the two phases and m phase versions of the proposed converter respectively. The three phase version of the proposed converter shown in Fig. 1(b) is further analysed in this paper. This paper is an extension of our previous work presented in the conference mentioned in Ref [17].

2 Principle of Operation of the Proposed Converter

The circuit diagram of the proposed converter is shown in Fig. 1(b) which is a three phase interleaved boost converter with coupled inductors and two voltage extension capacitors. S_1, S_2 and S_3 are the active switch of phase#1, Phase#2 and phase#3 respectively. D_1, D_2 and D_3 are the rectifying diodes of three phases. L_1 is filter inductor of phase#1 and L_2 is filter inductor of phase#2. L_C is the coupled inductor in phase#3 with primary winding inductor L_P and secondary winding inductor L_S. C_1 and C_2 are the extension capacitors connected in phase#1 and phase#2 respectively. C_O is the output filtering capacitor and R_O is load resistance.

For the proposed converter, the following assumptions are made.

- $L_1 = L_2 = L_P = L$ (where, L is the filtering inductance/phase)
- The converter operates in continuous conduction mode (CCM)
- Duty ratio D is greater than 66 %.

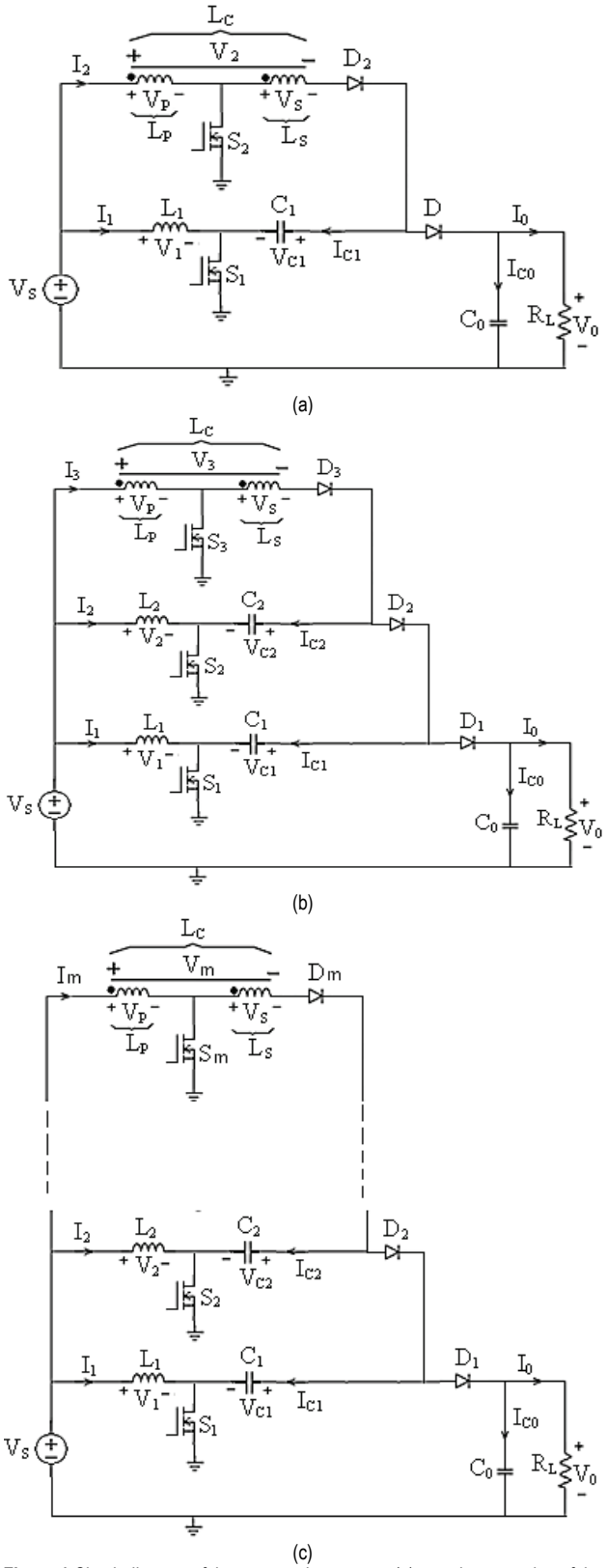


Figure 1 Circuit diagram of the proposed converter: (a) two phase version of the proposed converter; (b) three phase version of the proposed converter; (c) *m* phase version of the proposed converter

The turn ratio n of the two coupled inductors L_P and L_S is defined as follows [16]:

$$n = \frac{V_3}{V_P} = \frac{n_1 + n_2}{n_2}. \quad (1)$$

where n_1 is number of turns of primary windings L_P, n_2 is the number of turns of secondary windings L_S, V_P is the voltage across primary windings L_P, V_S is the voltage across secondary windings L_S and V_3 is the voltage across both the primary and secondary windings L_C. From (1) we get:

$$V_3 = \left(\frac{n_1 + n_2}{n_2} \right) \cdot V_P. \quad (2)$$

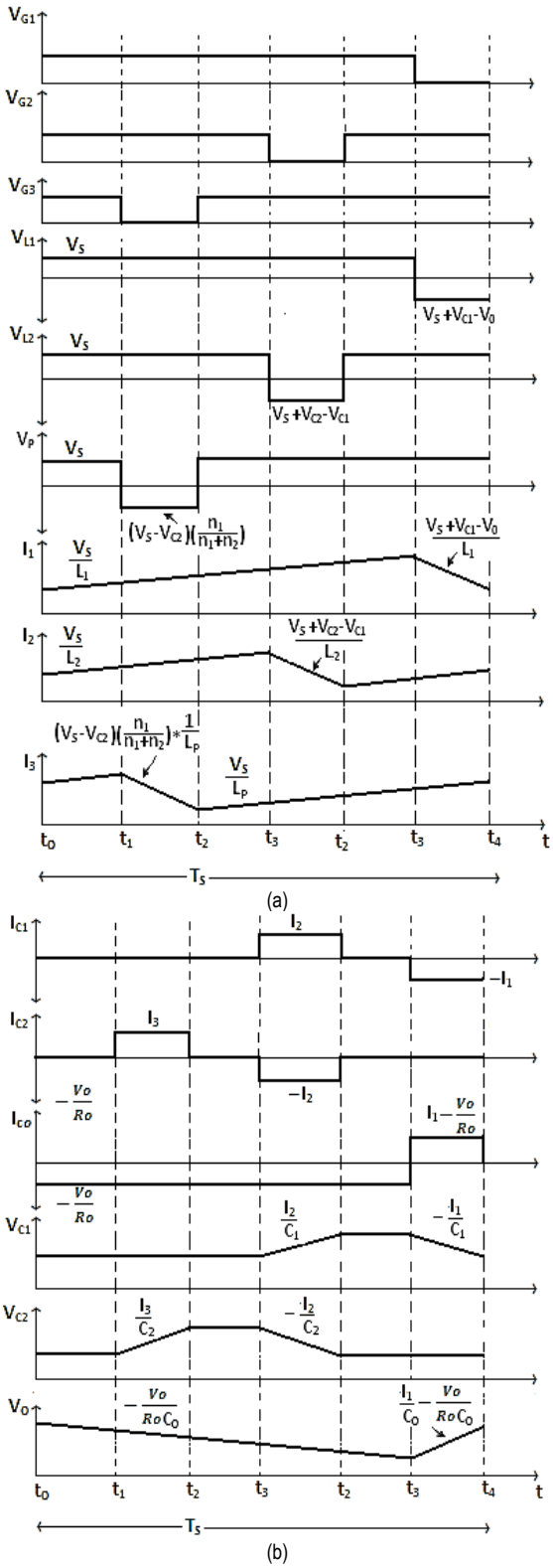


Figure 2 Steady state waveforms of the proposed converter

Three PWM signals phase shifted 120 degrees from each other are applied to the gates of the switches S_1, S_2 and S_3. The duty ratio All the three PWM signals have the same switching frequency F_S, switching period T_S and same duty ratio. There are six switching states/modes in one complete switching. Fig. 2 shows the principle waveforms of the proposed converter and Fig. 3 gives the circuit diagram of the proposed converter in each state.

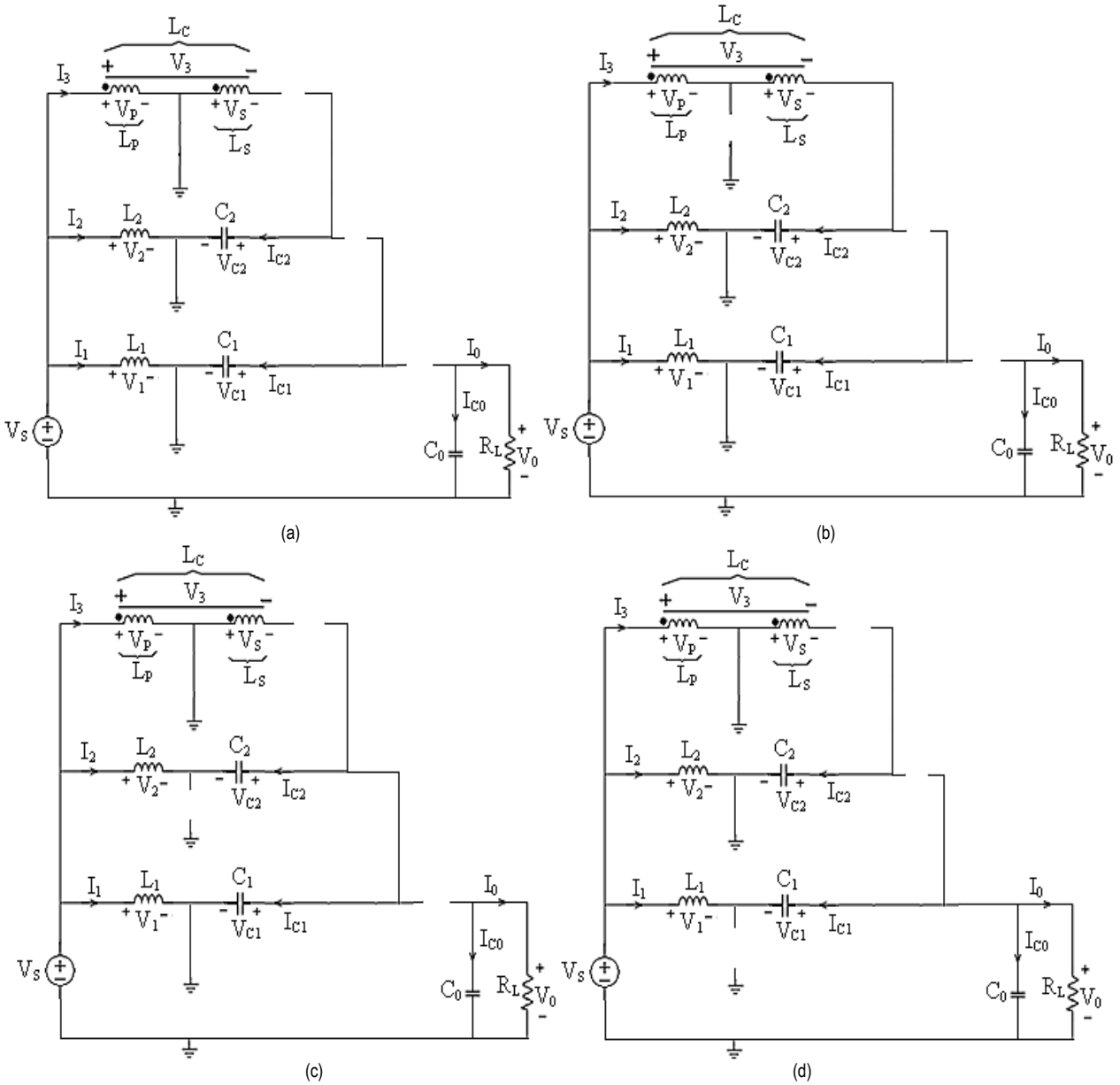


Figure 3 Circuit diagram of proposed converter in each state: (a) State I, III and V; (b) State II; (c) State IV, (d) State VI

2.1 State I ($t_0 \le t \le t_1$)

This state starts when all the transistors S_1, S_2 and S_3 are turned on. All the diodes D_1, D_2 and D_3 are off in this state. Fig. 3(a) shows the circuit diagram of the proposed converter in this state. Inductors L_1, L_2 and L_P are charged by the supply voltage and the voltages V_{L1} across L_1, V_{L2} across L_2 and V_P across L_P are positive. Therefore, the currents I_1 through L_1, current I_2 through L_2 and current I_3 through L_P increase linearly with slopes of V_S/L_1, V_S/L_2 and V_S/L_P respectively. Capacitors C_1 and C_2 are disconnected and they neither charge nor discharges. The current I_{C1} through C_1 and current I_{C2} through C_2 is zero. Therefore the voltage V_{C1} across C_1 and voltage V_{C2} across C_2 are constant. Capacitor C_0 discharges to load, the current I_{C0} through it is negative and output voltage V_0 decreases linearly with a slope of $(-V_0)/(R_0C_0)$. This state ends when switch S_3 is turned off at time t=t_1.

2.2 State II ($t_1 \le t \le t_2$)

During this state switches S_1 and S_2 are on and switch S_3 is off. Therefore, diodes D_1 and D_2 are off and diode D_3 is on. Fig. 3(b) shows the circuit diagram of the proposed converter in this state. Inductors L_1 and L_2 are still charged by the supply and currents I_1 and I_2 increase with same slopes. Inductor L_P discharges through its secondary coupled winding to extension capacitor C_2. Hence, the current I_3 falls linearly with a slope of $\{(V_S - V_{C2})(n_1/n_1 + n_2)\}/L_P$. The capacitor C_2 is charged up and voltage V_{C2} across it increases with a slope of I_3/C_2. Capacitor C_1 is still disconnected and V_{C1} remains

constant. Capacitor C_0 still discharges to load and output voltage further falls with the same slope. This state ends when switch S_3 is again turned on at $t = t_2$.

2.3 State III ($t_2 \le t \le t_3$)

This state is similar to State I. All the transistors are on and all diodes are off and the circuit diagram is same as shown in Fig. 3(a). This state starts at $t = t_2$ and ends at $t = t_3$.

2.4 State IV ($t_3 \le t \le t_4$)

In this state switches S_1 and S_3 are on and switch S_2 is off. The diodes D_1 and D_3 are off and diode D_2 is conducting. The circuit diagram of proposed converter in this state is shown in Fig. 3(c). Inductors L_1 and L_P are charged by the supply and current I_1 and I_3 increases with slopes of V_S/L_1 and V_S/L_P respectively. Inductor L_2 and capacitor C_2 discharge to capacitor C_1 and C_1 is charged up. The output capacitor C_0 is still supplying the load and discharges. Current I_2 falls linearly with a slope of $V_S+V_{C2}-V_{C1})/L_2$ and voltage V_{C2} falls with a slope of $(-I_2)/C_2$. Since C_1 is charged up, voltage V_{C1} increases with a slope of I_2/C_1 and output voltage falls with the same slope of $(-V_0)/(R_0C_0)$. This state ends at $t = t_4$ when S_2 is again turned on.

2.5 State V ($t_4 \le t \le t_5$)

This state is also similar to State I and State III and it ends at $t = t_5$.

2.6 State VI ($t_5 \le t \le t_6$)

This state starts when S_1 is turned off at $t = t_5$. S_2 and S_3 remain off in this state. Diode D_1 is conducting and diodes D_2 and D_3 are off. Fig. 3(d) shows the circuit diagram of proposed converter in this state. During this state L_2 and L_P are charged and I_2 and I_3 rise with slopes of V_S/L_2 and V_S/L_P respectively. C_2 is disconnected and V_{C2} is constant. L_1 and C_1 are discharged to the load and C_0 is charged in this state. I_1 falls with a slope of $(V_S+V_{C1}-V_0)/L_1$ and V_{C1} falls with a slope of $(-I_1)/C_1$. Output voltage V_0 rises in this state with a slope of $I_1/C_0-V_0/(R_0C_0)$. This state ends when S_1 is turned on again at $t = t_6$.

3 STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

For the steady state analysis of the proposed converter, the time of each state is expressed in terms of duty cycle D and switching period T_S (in seconds) as below:

$t_0 = 0$, $t_1 = (DT_S - 2T_S/3)$, $t_2 = T_S/3$, $t_3 = (DT_S - T_S/3)$, $t_4 = 2T_S/3$, $t_5 = DT_S$, $t_6 = T_S$.

3.1 DC Conversion Ratio

To obtain the dc voltage conversion ratio of the proposed converter, we will use the inductor volt second balance principle on the filtering inductors L_1, L_2 and L_P. Now by the volt second balance of L_P we get:

$$V_S(t_1-t_0)+(V_S-V_{C1})\left(\frac{n_1}{n_1+n_2}\right)(t_2-t_1)+V_S(t_3-t_2)+ \\ +V_S(t_4-t_3)+V_S(t_5-t_4)+V_S(t_6-t_5)=0. \quad (3)$$

Eq. (3) can be solved for:

$$V_{C2}=\frac{V_S}{1-D}\left(1+\frac{n_2}{n_1}D\right). \quad (4)$$

Similarly, by the volt second balance of L_2 we get:

$$V_S(t_1-t_0)+V_S(t_2-t_1)+V_S(t_3-t_2)+ \\ +(V_S+V_{C2}-V_{C1})(t_4-t_3)+V_S(t_5-t_4)+V_S(t_6-t_5)=0. \quad (5)$$

Solution of Eq. (5) gives:

$$V_{C1}=\frac{V_S}{1-D}+V_{C2}. \quad (6)$$

From Eq. (4) and Eq. (5) we get:

$$V_{C1}=\frac{V_S}{1-D}\left(2+\frac{n_2}{n_1}D\right). \quad (7)$$

And the volt second balance of L_1 gives:

$$V_S(t_1-t_0)+V_S(t_2-t_1)+V_S(t_3-t_2)+ \\ +(V_S+V_{C2}-V_{C1})(t_4-t_3)+V_S(t_5-t_4)+ \\ +(V_S+V_{C1}-V_0)(t_6-t_5)=0. \quad (8)$$

Eq. (8) can be solved for:

$$V_0=\frac{V_S}{1-D}+V_{C1}. \quad (9)$$

From Eq. (7) and Eq. (8) we get:

$$V_0=\frac{V_S}{1-D}\left(3+\frac{n_2}{n_1}D\right). \quad (10)$$

Eq. (10) gives the expression for the output voltage of the proposed converter. The dc conversion ratio/voltage gain M is given by:

$$M=\frac{V_0}{V_S}=\frac{1}{1-D}\left(3+\frac{n_2}{n_1}D\right). \quad (11)$$

Let the ratio of secondary winding of coupled inductor to its primary winding be expressed by x, that is, $(n_2/n_1) = x$, then the expression of voltage gain can be written as:

$$M = \frac{V_0}{V_S} = \frac{1}{1-D}(3+xD). \quad (12)$$

Since the analysis is done for a three phase version of the proposed converter, number 3 appears in the expression of output voltage and voltage gain. For m number of phases of the proposed converter, the expressions of output voltage and voltage gain are:

$$V_0 = \frac{V_S}{1-D}(m+xD), \quad (13)$$

$$M = \frac{V_0}{V_S} = \frac{1}{1-D}(m+xD). \quad (14)$$

Thus by increasing the number of phases m and increasing the ratio x, a higher voltage gain can be achieved.

3.2 Voltage Stress of Transistors

The voltage stress of switch S_1 can be found when it is off in State IV. Using Fig. 3(d), the voltage stress V_{S1} of S_1 is given by:

$$V_{S1} = V_0 - V_{C1}. \quad (15)$$

Similarly, using Fig. 3(c), the voltage stress V_{S2} of switch S_2 is given by:

$$V_{S2} = V_{C1} - V_{C2}. \quad (16)$$

And using Fig. 3(b), the voltage stress V_{S3} of switch S_3 can be obtained as:

$$V_{S3} = V_S + \left(\frac{n_1}{n_1+n_2}\right)V_{C2} - \left(\frac{n_1}{n_1+n_2}\right)V_S. \quad (17)$$

From Eqs. (15), (16) and (17) we get:

$$V_{S1} = V_{S2} = V_{S3} = \frac{V_S}{1-D}. \quad (18)$$

4 SIMULATION RESULTS

To verify the performance of the proposed converter, theoretical and simulation results are obtained for the proposed converter as well as a traditional three phase interleaved boost converter [18] using the parameters listed in Tab. 1.

Using the parameters of Tab. 1 and Eq. (10) value of the ratio is obtained which is D=0.7 or 70 %. Using the parameters in Eq. (4) and Eq. (7) the voltage across extension capacitors is obtained which is: V_{C1}= 273 V, V_{C2}= 207 V. Using Eqs. (15), (16) and (17) the voltage stresses of transistors are: V_{S1}= 67 V, V_{S2}= 67 V, V_{S3}= 67 V. Using the parameters in Eq. (14) the voltage gain is M=17.

Fig. 4 shows the simulation results of the proposed for a duty cycle of 70 %. As it is clear from Fig. 4(a), the proposed converter generates an output voltage of 343 volts for 20 volt input. Fig. 4(b) and (c) shows that capacitor C_1 voltage V_{C1} is 269 volts and voltage across C_2 is 209 volts. Fig. 4(d), (e) and (f) shows the waveforms of voltage stress across Mosfets S_1, S_2 and S_3 which are all nearly 70 volts.

Table 1 Parameters used for simulation

Name of parameter	Symbol	Value
No of phases	m	3
Output power	P_O	40 W
Input voltage	V_S	20 V
Output voltage	V_O	340 V
Load resistance	R_L	400 Ω
Frequency	F_S	100 kHz
Number of turns of Inductor L_P	n_1	100 Turns
Number of turns of Inductor L_S	n_2	300 Turns
Filter inductor/phase	L	300 mH
Extension Capacitor 1	C_1	1 μF
Extension Capacitor 2	C_2	1 μF
Output smoothing capacitor	C_0	1 μF

Fig. 5 shows the simulation waveforms of a traditional three phase interleaved boost converter. For 70 % duty cycle the waveform of output voltage is shown in Fig. 5(a) which is only 73 volts. This converter produces an output voltage of 340 volts from 20 volts input at 94.1 % duty cycle as shown in Fig. 5(b). Fig. 5(c), (d) and (e) shows the voltage stress across MOSFETs of traditional 3 phases interleaved boost converter which are all equal to 340 volts.

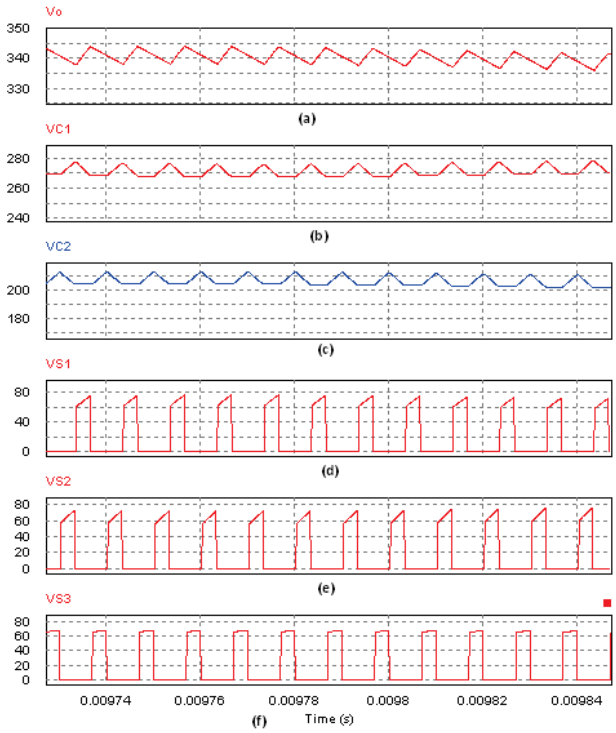


Figure 4 Simulation waveforms of the proposed converter at 70 % duty cycle: (a) Waveform of output voltage; (b) Waveform of voltage across capacitor C_1; (c) Waveform of voltage across capacitor C_2 (d) Voltage stress of MOSFET S_1; (e) Voltage stress of MOSFET S_2; (f) Voltage stress of MOSFET S_3

The simulation results show that the proposed converter generates and outputs voltage of 340 volts from a 20 volts input at a duty cycle of 70 %, whereas the traditional 3 phases interleaved boost converter produces

the same output at a duty cycle of 94 % which is very high and will cause severe reverse recovery problem. At 70 % duty cycle the traditional interleaved boost converter gives only 73 volts output, thus the voltage gain of the proposed converter is almost five times higher than the traditional interleaved boost converter. Moreover, the voltage stress across the main switches of the proposed converter is only 70 V which is very low, whereas that of the MOSFETs of traditional interleaved boost converter is 340 V. Thus the switching losses in the proposed converter will be less and also low rating MOSFETs can be used which will help in reducing the overall size and cost

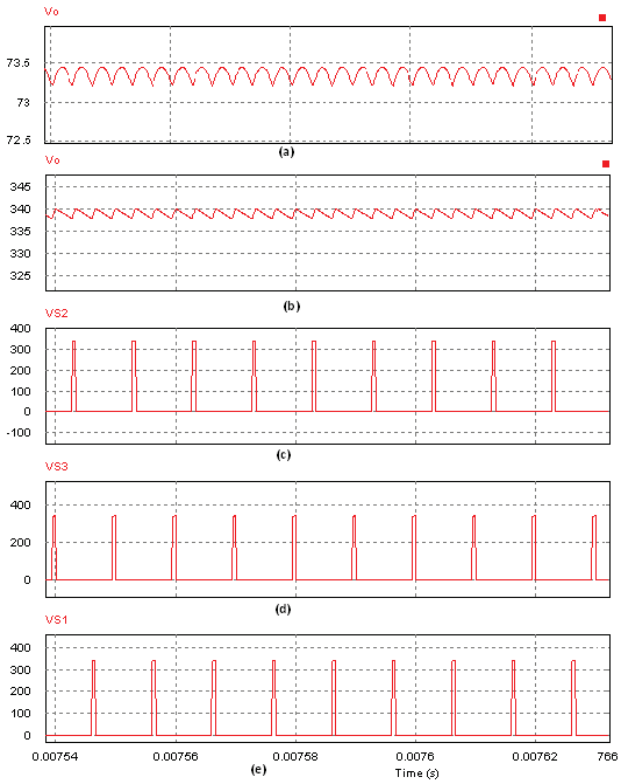


Figure 5 Simulation results of traditional 3 phases interleaved boost converter: (a) Waveform of output voltage at 70 % duty cycle; (b) Waveform of output voltage at 94,1 % duty cycle; (c) Voltage stress of MOSFET S_2; (d) Voltage stress of MOSFET S_3; (e) Voltage stress of MOSFET S_1.

5 EXPERIMENTAL VALIDATION

Experiment is carried out on a two phase version of the proposed converter on a 32 W prototype. The photograph of experimental setup is shown in Fig. 6. For experiment the parameters listed in table II are used. The parameters used for experiment differ from those of simulation due to the lack of some Lab instruments.

Using these parameters in Eq. (13) and Eq. (14), D=0.6 60 % and M=8. The voltage stress on MOSFETs is 2.5V_S for the two phase version of the proposed converter.

Fig. 7 shows the experimental waveforms. The waveforms of input voltage of 20 volts and the two gate pulses with 60% on time are shown in Fig. 7(a). Fig. 7(b) shows the output voltage and voltage stress across MOSFETs S_1 and S_2. The output voltage is 150 volts which is close to ideal value of 160 volts. The voltage stress across both the switches S_1 and S_2 is 50 volts which is 2.5 times of the supply voltage.

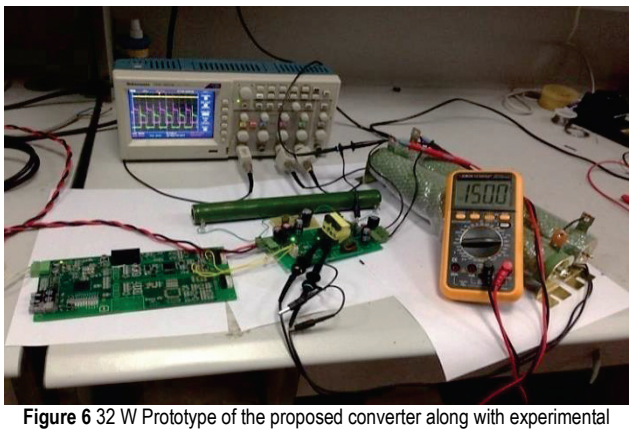
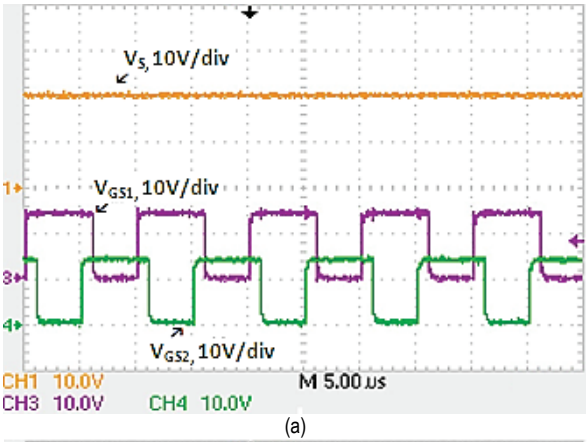


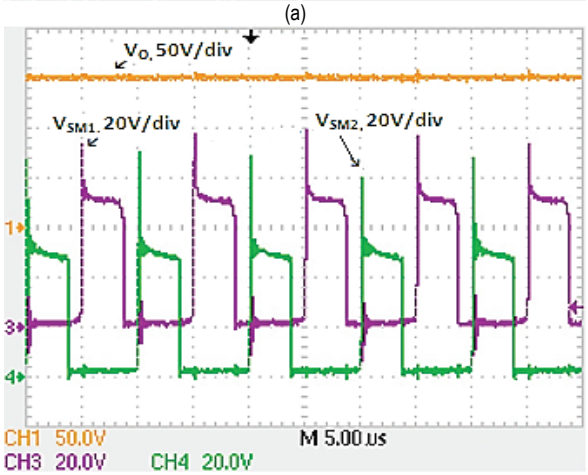
Figure 6 32 W Prototype of the proposed converter along with experimental setup

Table 2 Parameters used for experiment

Name of parameter	Symbol	Value
No of phases	m	2
Output power	P_O	32 W
Input voltage	V_S	20 V
Output voltage	V_O	160 V
Load resistance	R_L	800 Ω
Load current	I_O	0.2 A
Frequency	F_S	100 kHz
Number of turns of Inductor L_P	n_1	12 Turns
Number of turns of Inductor L_S	n_2	25 Turns
Filter inductor in phase#1	L_1=L	1 mH
Filter inductor in phase#2	L_P=L	1 mH
Intermediate capacitor	C_1	1 μF
Output smoothing capacitor	C_O	1 μF



(a)



(b)

Figure 7 Experimental results of the proposed converter at 60 % duty cycle: (a) input voltage and gate pulses; (b) output voltage and voltage stress across MOSFETs S_1 and S_2

6 CONCLUSION

By using the coupled inductors and voltage extension capacitors a high voltage gain is achieved by the proposed converter. The voltage stress across the main transistor switches which is always equal to the output voltage in traditional interleaved boost converter is considerably reduced. From theoretical analysis, simulation and experimental results it is clear that the two phase version of the proposed converter has three times higher conversion ratio and three times lesser voltage stress across its transistors switches as compared to a traditional two phase interleaved boost converter and the three phase version of the proposed converter has five times higher conversion ratio and five times lesser voltage stress of transistors as compared to a traditional three phase interleaved boost converter. For more than three phases of the proposed converter, the conversion ratio can be higher and voltage stress can be further reduced. These features make the proposed converter a candidate topology for renewable energy applications especially photovoltaic where high step-up dc-dc voltage conversion is essential. . The proposed topology is designed and tested for power ratings of 32 watts. To move the proposed converter topology from laboratory prototypes to industrial applications, the proposed can be tested at high power ratings, that is, at kilo watt level. Further future research on the proposed topology includes developing small signal dynamic model for the proposed converter to realize the closed loop, studying the effects of the proposed converter on the dynamic stability of the dc grids and implementing the proposed converter on higher power and voltage ratings using insulated gate bipolar transistors (IGBTs) instead of Mosfets.

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