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Simulation and Control Strategy of a 5.6 kV 17-level STATCOM Under SVG Condition

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Original scientific paper

To achieve high-voltage reactive power compensation, a 5.6kV 17-level STATCOM under SVG Condition is presented. In this paper, we use a cascaded H-bridge multilevel star-connection converter whose system structure and circuit schematic are described. Then by using the phase-shifted carrier modulation strategy and the active-reactive current decoupling method, the STATCOM performs quite well. Moreover modulation strategy of the 17-level STATCOM based on the active disturbance rejection control (ADRC) is presented and the analytical formulas are described. For implementation, control strategy for DC bus voltage balance in cascaded H-bridge multilevel converters, time average distribution method and extreme value offset method are applied in our design. Finally, simulation results demonstrate that the proposed 17-level STATCOM is capable of reactive power compensation, simultaneous controlling and balancing the DC side voltages during the work and verify that high-voltage reactive power can be accurately and effectively compensated.

Key words: STATCOM, Static var generation (SVG), Control strategy, Active-reactive current decoupling, Cascaded H-bridge (CHB) multilevel converters, Time average distribution, Extreme value offset

Simuliranje i upravljačka strategija 5.6 kV 17-razniskog STATCOM sustava uz SVG uvjet. Za postizanje kompenzacije jalove snage uz visoki napon, predstavljen je STATCOM s 5.6 kV i 17-razina uz SVG uvjet. U ovom radu koristimo kaskadni višerazinski H-mosni pretvarač u zvijezda spoju uz opisane strukturu i shemu spoja. Zatim korištenjem strategije modulacije s fazno-pomaknutim signalom nosioca i metode rasprezanja radno-jalove struje, STATCOM pokazuje prilično dobro vladanje. Uz to, prikazana je strategija modulacije 17-razinskog STATCOM-a zasnovana na upravljanju s aktivnim odbacivanjem smetnji (ADRC) te su opisane analitičke formule. Za implementaciju, u naš dizajn primjenjene su upravljačka strategija balansiranja napona DC sabirnice u kaskadnom višerazinskom H-mosnom pretvaraču te metoda vremenskog uprosječavanja razdiobe i metoda ekstremne vrijednosti pomaka. Konačno, simulacijski rezultati pokazuju da je predloženi 17-razinski STATCOM sposoban za kompenzaciju jalove snage, istovremeno upravljanje i balansiranje napona DC strane u radu te potvrđuju da je jalovu snagu uz visoki napon moguće točno i djelotvorno kompenzirati.

Ključne riječi: STATCOM, proizvodnja energije uz statičku jalovu snagu (SVG), upravljačka strategija, rasprezanje radne-jalove struje, višerazinski H-mosni pretvarači (CHB), vremenski uprosječena razdioba, ekstremna vrijednost odmaka

1 INTRODUCTION

In recent years, the major power has been consumed through instantaneous reactive loads like asynchronous motor, synchronous motor, pumps etc. According to the concepts and principles of instantaneous reactive power compensation, the static synchronous compensator (STATCOM) performs well in the stability of the system voltage, system steady-state and dynamic [1, 2]. Compared with the traditional static var compensator (SVC), it has advantages such as high adjustment speed, wide operation range, continuous compensation, small harmonic current and low loss etc [3]. In addition, two-level inverters which can reduce the harmonics while increasing the capacity are introduced into STATCOM [4]. However the necessary expensive transformer leads to the high system cost and energy consumption. Cascaded H-bridge (CHB) multilevel inverters without transformer are applied in the area of high-voltage and high-power STATCOM [5,6], and those inverters uses multi-level square wave synthesis staircase to obtain sinusoidal output voltage. With the increasing in output voltage level, a better harmonic spectrum is achieved, and switches have low voltage stress. Due to its low cost,

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high reliability, security, and good controllability, the CHB STATCOM has been widely applied in the reactive power compensation, power quality control and other fields.

There are many control methods for CHB multilevel STATCOM such as modulation technique based on ladder wave, PWM (pulse width modulation) modulation technique based on space vector (SVPWM), and PWM modulation method based on carrier [7, 8]. All these control methods have their advantages and disadvantages. We can select and use the appropriate control methods in practical applications. CPS-SPWM (carrier phase shifted sinusoidal pulse with modulation) can control output of inverter according to SPWM law in high power applications, improve the output waveform greatly, reduce the output harmonics and reduce cost with smaller filter. On account of its high equivalent switching frequency and wide transmission bandwidth, a variety of advanced control strategies can be used to optimize the overall system performance.

CHB multilevel inverter is connected with DC side capacitors which are isolated from each other, based on this, it exists multi-independent DC bus voltage and unbalanced DC capacitor voltage. Moreover because each H-bridge inverter is a linear, multi-variable and strong coupling system, thus the parallel loss, switching loss, modulation ratio and pulse delay are different among inverters [9, 10]. DC bus voltage balance control is directly related to AC side of inverter output waveform quality, active and reactive power output, voltage and current of switching device, and dynamic response of converter. Unbalanced DC capacitor voltage can decrease the performance of CHB multilevel converter [11].

Given above all, novel control strategies for DC bus voltage balance, time average distribution method and extreme value offset method are applied in this paper. The paper is organized in the following manner. In Section 2, the system structure of STATCOM including the schematic of CHB multilevel converter is reviewed Section 3 describes the modulation strategy of 17-level STATCOM using active-reactive current decoupling. he novel control strategy for DC bus voltage balance in CHB multilevel converters is presented in Section 4 and in Section 5 the simulation results are illustrated. Section 6 is devoted to total voltage of CHB multilevel converters conclusions.

2 SYSTEM STRUCTURE OF STATCOM

Fig. 1 shows the system structure of STATCOM. In this figure, u_{sa}, u_{sb} and u_{sc} are grid voltage, i_{la}, i_{lb} and i_{lc} stand for load current, u_{ca}, u_{cb} and u_{cc} are voltage of STATCOM, i_{ca}, i_c and i_{ca} are the output current of STATCOM. L_c is the filter inductance while L_s is the line inductance. The main circuit of STATCOM is 17-level CHB multilevel converters which is shown in Fig. 1. It consists

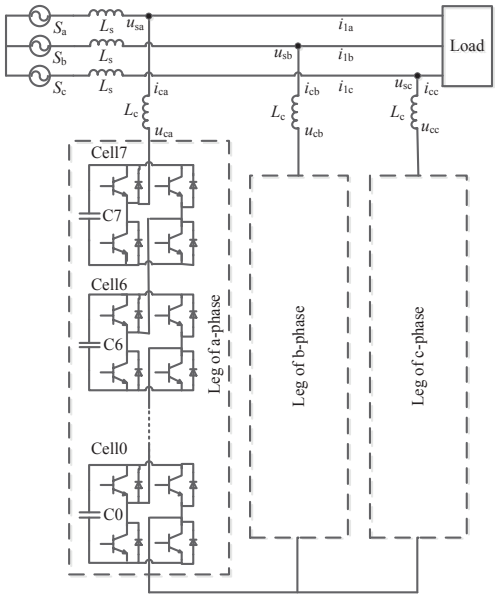


Fig. 1. System structure of 17-level STATCOM

of three legs in star-connection and each leg consists of eight cells (H-bridge converter) and filter inductances. The output voltage level be increased by connecting H-bridge converter in sequence. Besides the DC side capacitor of H-bridge converter is independent. STATCOM is mainly used to realize the current reactive power compensation. Energy exchange between the grid and STATCOM is realized by adjusting the phase and amplitude of the STATCOM output voltage, respectively. The amount of exchanged energy is determined by STATCOM active power and load reactive power. 17-level CHB as STATCOM produce high-quality sine wave without transformer. Three small smoothing reactors are required to filter out high-frequency current harmonics generated by STATCOM.

3 MODULATION STRATEGY OF 17-LEVEL STATCOM BASED ON ADRC

In Fig. 2, the controller detects the reactive component, i_{qref},of the load side current, i_{labc}, by using the park transform and phase-locked loop (PLL). The active and reactive component of i_{ab}, i_d ,and i_q are got from the output current, i_{cabc}, of STATCOM by Park transform. The active component, i_{dref}, from PI controller is determined by the DC side reference value, u_{dcref}, and feedback voltage, u_{dc}. By Park transform, u_{sd} and u_{sq} are got from System voltage, u_{abc}. All the variables above are used by reactive decoupling controller, and the output voltage vector, u_d and u_q, are obtained.Input signal of CPS-PWM,u_α) and u_β, are got from u_d and u_q by dq-$\alpha\beta$ transform. Finally, CSP-PWM generator engender PWM signal. The driving

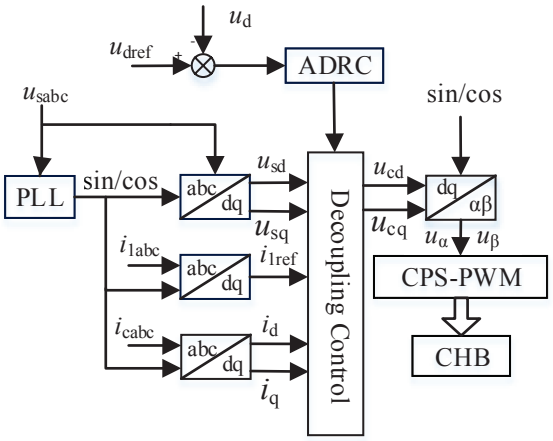


Fig. 2. Control principle of STATCOM

circuit makes the CHB work, and STATCOM generates the desired reactive power.

3.1 CHB switching modulation signals

Among the different pulse generation methods, the PWM which is achieved by comparing reference signal with a high-frequency 'carrier' signal is the most preferred approach in multilevel converters. It has the advantage of switching frequency been fixed and implementation simplicity. Carrier phase-shift PWM (CPS-PWM) is the most commonly used modulation method for H-bridge multilevel converter, because of it's power distribution among all of the CHBs and easy to implement [12–14]. The phase of each carrier signal is shifted in a proper angle to reduce the harmonic of current flowing from each leg and to lower the output current ripple of the CHB.

The modulation method, unipolar dual frequency CPS-SPWM, is used. The working principle is that all H-bridge converters have the same modulation reference signal, and the phase of its triangular carrier signal shifts 1/N of the carrier cycle, and the cascaded H bridge inverters consists of N cells in sequence connection. The carrier phase is shifted half carrier cycle for the two legs of an H-bridge converter, and the same modulation reference sine signal is used to generate the unipolar dual frequency CPS-SPWM. Because a common modulation reference signal is used, the fundamental output is exactly the same. The output of each H-bridge converter can be added together, the general output is N times of single H-bridge output, and the output voltage is 2N+1 level. For the carrier phase shift, the low-order harmonics cancel each other out which leads to the improvements of the equivalent switching frequency.

3.2 System control based on ADRC

ADRC is a new type of controller which can inherit the advantage as independent of the object model and improve inherent defects of the traditional PID. ADRC can automatically detect the real-time effects of the system and compensates the error. ADRC detects and compensates the total disturbances of the system, whether internal disturbances or external disturbances. ADRC does well, whether parameters change or uncertain disturbance, which shows that it has strong adaptability, robustness and maneuverability [15].

For the nonlinear uncertain objects of SISO, equation (1) is given as below:

$$y(n) = f(y, \dot{y}, \cdots, y^{(n-1)}, t) + \bar{\omega}(t) + bu, \qquad (1)$$

where $f(y, \dot{y}, \cdots, y^{(n-1)}, t)$ is unknown function, $\bar{\omega}(t)$ is unknown disturbances, y is measurement output, u is control input.

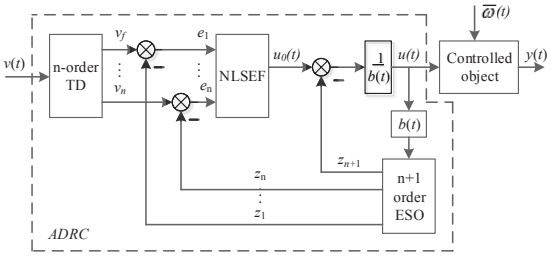


Fig. 3. The diagram of ADRC

The diagram of ADRC corresponding to equation (1) is shown in Fig. 3. It is composed of a tracking differentiator (TD), an extended state observer (ESO), and a nonlinear state error feedback controller (NLSEF). TD realizes the fast non-overshoot tracking of the input signal and gives the reference input of corresponding derivative. ESO can be used to estimate system state, real-time effect of model and external disturbance and compensate it. The nonlinear uncertainty object with unknown interference is controlled as integral tandem object. NLSEF realizes the disturbances compensation control by using the error between the output of the TD and ESO.

The realization of the first order ADRC is given as

$$\begin{cases} v_1 = -r \cdot fal\,(v_1 - v(t), a_0, \delta_0) \\ \varepsilon = z_1 - y \\ \dot{z}_1 = z_2 - \beta_1 \cdot fal(\varepsilon, a_1, \delta_1) + bu \\ \dot{z}_2 = -\beta_2 \cdot fal(\varepsilon, a_1, \delta_1) \\ \varepsilon_1 = v_1 - z_1 \\ u_0 = \beta_3 \cdot fal(\varepsilon_1, a_2, \delta_2) \\ u = (u_0 - z_2)/b \end{cases}, \qquad (2)$$

where $fal(\varepsilon, a, \delta) = \begin{cases} |\varepsilon|^a \mathrm{sgn}(\varepsilon) & |\varepsilon| > \delta \\ \varepsilon/\delta^{1-a} & |\varepsilon| \le \delta \end{cases}$.

It can be seen from equation (2) that the input and output of the object, u and y, is needed, which means it is simple and easy to implement.

From Fig. 1, according to the voltage balance of system, mathematical model of the main circuit is obtained in equation (1).

$$L\frac{di}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} u_{sa} \\ u_{sb} \\ u_{sc} \end{bmatrix} - \begin{bmatrix} u_{ca} \\ u_{cb} \\ u_{cc} \end{bmatrix} + R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \quad (3)$$

where R is a known resistance.

Based on Park transform, equation (3) transforms from abc coordinate to dq coordinate and the sum of three-phase currents is zero in three-phase three-wire system. Mathematical model under dq coordinate is defined in equation (4).

$$L\frac{di}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ \omega L & -R \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} u_{sd} - u_{cd} \\ u_{sq} - u_{cq} \end{bmatrix}, \quad (4)$$

where L is known electrical inductance, ω is a known parameter.

Laplace transform is applied to (4) and we can get:

$$Ls\begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ \omega L & -R \end{bmatrix}\begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} + \begin{bmatrix} U_{sd}(s) \\ U_{sq}(s) \end{bmatrix} - \begin{bmatrix} U_{cd}(s) \\ U_{cq}(s) \end{bmatrix}. \quad (5)$$

Active current i_d and reactive current i_q coupled to each other by connection inductance which makes it difficult to control. To obtain the optimal control effect, it is necessary to decouple i_d and i_q.

From equation (4), equation (6) can be obtained:

$$\begin{cases} L\dfrac{dI_d}{dt} = -RI_d + \bar{\omega}_d - U_{cd} \\ L\dfrac{dI_q}{dt} = -RI_d + \bar{\omega}_q - U_{cq} \end{cases}. \quad (6)$$

Voltage u_{sd} and u_{sq} are difficult to measure and uncertainty. $\bar{\omega}_d = \omega L \cdot I_q + U_{sd}$ and $\bar{\omega}_q = -\omega L \cdot I_d + U_{sq}$ are internal disturbances.

Decoupled d, q axis ADRC is obtained. Diagram of active-reactive decoupling control is shown in Fig. 4.

Reactive power control is described as an example. Reactive current reference from reaction power detection, i_q^*, is reference of ADRC. Reactive current flowing through STATCOM is output. The output voltage, u_{cq}, is the control signal. The reactive current follows the change of reference current.

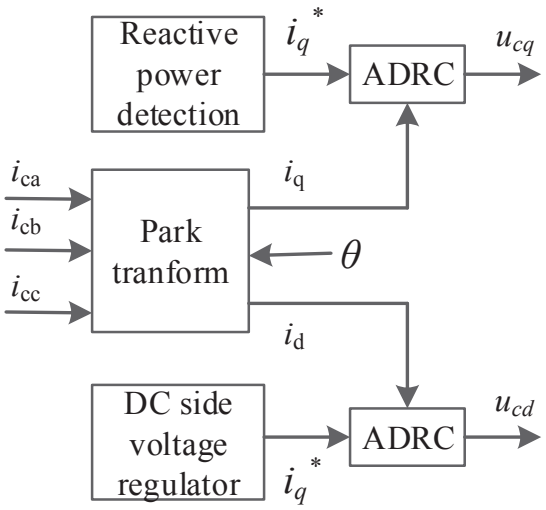


Fig. 4. Diagram of active-reactive decoupling control

According to equation (4), control system of reactive power is 1st order and 1st order TD is needed. Supposing the output of 1st TD is

$$v_1 = -k_1 \cdot fal\left[(v_1 - i_q^*), a_1, \delta_1\right], \quad (7)$$

2nd order ESO is built and given as below

$$\begin{cases} \dot{z}_1 = z_1 - k_{21} \cdot fal(\varepsilon_2, a_2, \delta_2) - U_{cq} \\ \dot{z}_2 = -k_{22} \cdot fal(\varepsilon_2, a_2, \delta_2) \end{cases}, \quad (8)$$

where $\varepsilon_2 = z_1 - i_q$. NLSEF can be obtained from nonlinear function of system state error feedback, $\varepsilon = z_1 - v_1$, and is given

$$\begin{cases} u_0 = k \cdot fal(\varepsilon, a, \delta) \\ u_{cq} = (u_0 - z_2) \cdot (-1) \end{cases}, \quad (9)$$

where k_1, a_1, δ_1, k_{21}, k_{22}, a_2, δ_2, k, a, and δ are pending parameters.

4 CONTROL STRATEGY FOR DC BUS VOLTAGE BALANCE IN CHB MULTILEVEL CONVERTERS

There are mainly two kinds of implementations for DC side voltage control strategies used: hardware implementation [2–4, 16] and software implementation [6, 7, 17].

The working principle of hardware implementation is to use hardware circuit to supply DC energy consumption, such as the shunt resistance, AC bus energy exchange and the DC link energy exchange. The aforementioned hardwares are PWM rectifier, diode bridge rectifier and inverter. The differences between these circuits are topology,

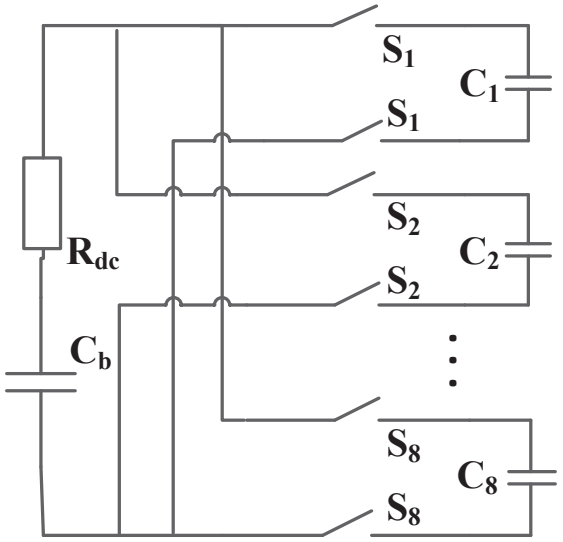


Fig. 5. Working principle of DC bus balance in CHB multilevel converters

energy sources and energy path. The voltage balance effect of hardware implementation method is perfect, however, it is not easy to use due to its high cost, large volume and, low efficiency [17].

By adjusting the pulse width or the phase angle of each cell, software implementation can keep the balance of DC side capacitance voltage, and it is useful for CPS-PWM. Pulse width and phase angle change can make the output voltage of CHB asymmetric, and introduce more harmonics. When the number of cells is higher, it is even worse, and lower frequency harmonics is introduced.

Given above all, a balance control method based on ADRC is applied which can be used in both two cells CHB multilevel inverters and eight cells CHB multilevel inverters in Fig. 5.

The working principle of DC bus balance in CHB multilevel converters is shown in Fig. 5, where C_b and R_{dc} are auxiliary capacitance and current limiting resistor respectively. Then simulation is carried out by MATLAB, and balanced DC capacitor voltage can be obtained. In a working period, DC side capacitance exchange energy with the auxiliary capacitance, C_b and later another DC side capacitance exchange energy with the auxiliary capacitance, C_b. In a word, extra energy of the DC side capacitance can be send transferred to the auxiliary capacitance, and these the energy will be used by another DC side capacitance. Finally, voltage balance will be achieved.

4.1 Time average distribution method

The method is that each unit is assigned the same time to consume the capacitor energy storage. Based on that, the voltage is achieved balancing. In this paper, DC side capacitance sorted in accordance with the sequence of cell, and the time connecting cell and auxiliary capacitance is the same, thus the charging and discharging probability of each module is the same. As long as the parameters are properly designed, the voltage balance between the modules can be achieved.

4.2 Extreme value offset method

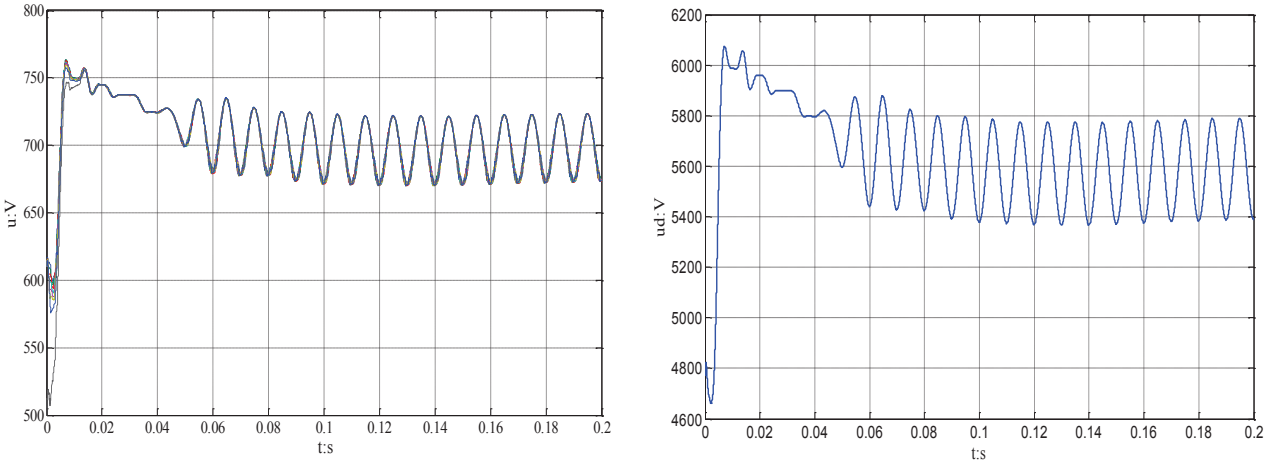
Extreme value offset method is applied to detect unit capacitor and voltage in real time, which passing the stored energy in the capacitor from highest voltage to the lowest one. In this paper, by detecting the maximum and minimum DC side capacitance voltage, and finding the corresponding cell, the energy in the corresponding capacitance will be exchanged. The maximum voltage capacitance transfer energy to the auxiliary capacitance first, then auxiliary capacitance transfer energy to the minimum voltage capacitance. At last, voltage balance between each module can be achieved.

5 SIMULATION RESULTS

The main goal of the experimental setup is to validate the structure of 17-level STATCOM and its corresponding control strategy. Simulation is carried out to demonstrate the high-voltage reactive power can be accurately and effectively compensated by the proposed methods. The system is established based on MATLAB/Simulink, parameters are described as below: each leg of CHB consists of eight cells in serial connection, DC power supply voltage $U_d = 5.6$ kV, DC side capacitance is 600 μF, rating voltage is 700 V, filter inductance $L = 8$ mH. Suppose that the main circuit switch is ideal switch, carrier frequency is 10 kHz, and CHB is in star-connection.

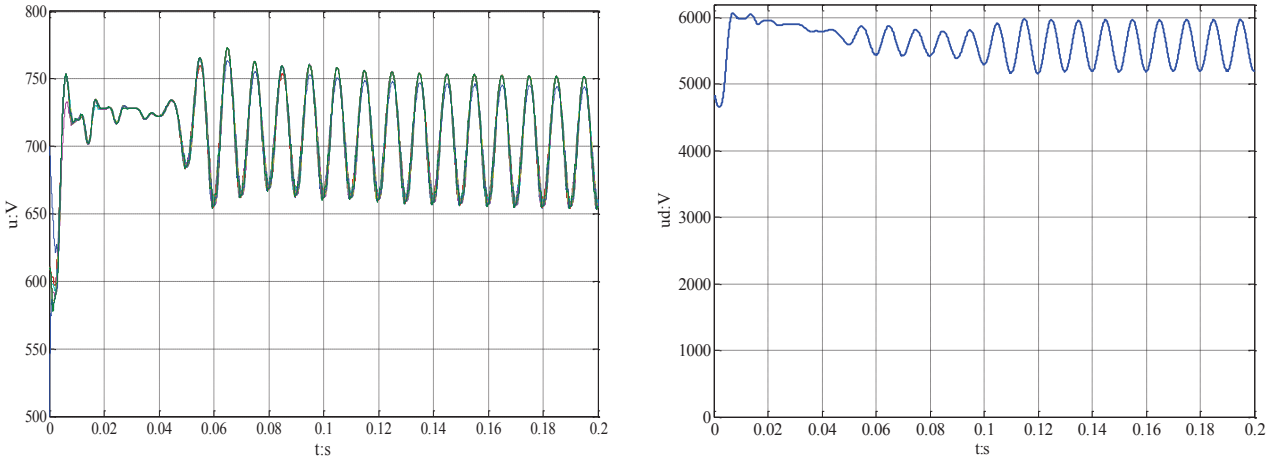
Firstly, in order to show the performance of the control strategy for DC bus voltage balance, the DC side capacitance voltage is tested by using time average distribution method, which is shown in Fig. 6. The DC side capacitance voltage of each cell can be observed in Fig. 6(a), it obviously that the DC bus voltage waveforms of each cell is similar in shape and amplitude. The total voltage of CHB multilevel converter can be observed in Fig. 6(b) where it can be seen that the total voltage is at 5600 V, and volatility is largely controlled within about $\pm 3.57\%$ after 0.06 s. The voltage shown in Fig. 6 verifies the effectiveness of time average distribution method.

Secondly, a test of the control strategy for DC bus voltage balance is processed; the DC side capacitance voltage using extreme value offset method has been performed. Fig. 7 illustrates the voltage of each cell and the total voltage of CHB multilevel converters. In Fig. 7(a), it is possible to see that the voltage of each cell is stable at 700 V which



(a) Voltage of each cell (b) Total voltage of CHB multilevel converters

Fig. 6. DC side capacitance voltage using time average distribution method



(a) Voltage of cell (b) Total voltage of CHB multilevel converters

Fig. 7. DC side capacitance voltage using extreme value offset method

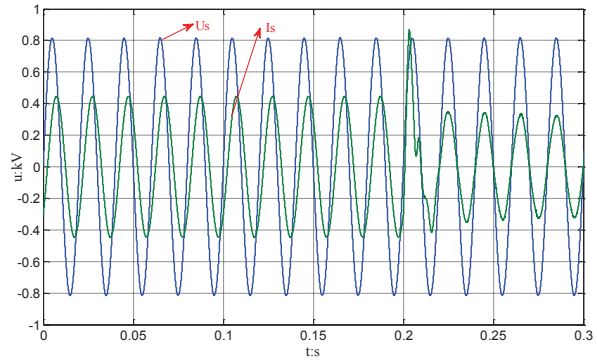
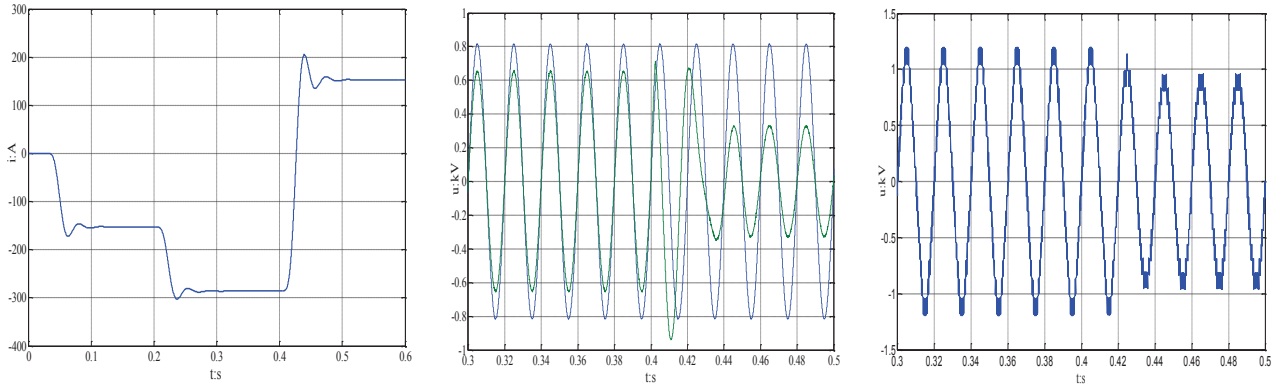


Fig. 8. Compensation effect of STATCOM at $t = 0.2s$

is largely controlled within about $\pm 7.14\%$, and different from each other. The total voltage varies between 5200 V and 6000 V after 0.02 s, which can be clearly observed in Fig. 7(b).

All these show that the sum of the DC side voltage is robust. Waveforms of capacitance voltage on cell coincide with each other and a balanced capacitance voltage are got. According to the results of figs, the DC side capacitance voltage using time average distribution method is better than using extreme value offset method. The relative voltage ripple of time average distribution method is much smaller than DC voltage control strategy used in [18, 19].

Thirdly, a test on compensation effect of STATCOM with putting into it at $t = 0.2$ s. Although it is not a normal operation of STATCOM. Fig. 8 shows the compensa-



(a) Reactive current component, i_{qref} (b) Grid voltage, u_s and grid current, i_s (c) Voltage of CHB multilevel converters, u_a

Fig. 9. Compensation results when load changes and the change of reactive current at $t = 0.4s$

tion effect of STATCOM when the STATCOM is accessed. Where u_s is grid voltage and I_s is grid load current, respectively. It presents that the phase angle of grid volage and load current are consistent in substantial, which shows that the power factor of the load side improves significantly, and the output waveform performs in high quality.

At $t = 0.4$ s, the load switches from L to C, by this way, it can be tested that the reactive compensation ability of CHB multilevel converters when the load changes from inductive to capacitive. Dynamic simulation waveforms are shown in Fig. 9. The waveform of the reactive current component, i_{qref} is shown in Fig. 9(a). Fig. 9(b) shows the waveform of grid voltage, u_s and grid current, i_s. The waveform of voltage of CHB multilevel converters, u_{ca} is shown in Fig. 9(c). It illustrates that even in the present of the load change, the system current and the CHB multilevel converters output changes. When system tuning is completed, the CHB multilevel converters output is consistent with the reactive current component both in the amplitude and the phase. Dynamic compensation effect of CHB inverter is better and the correctness of calculation of reference signals is demonstrated yet.

The diagram of power factor is shown in Fig. 10. At $t = 0.2$ s, inductive load is larger. At $t = 0.4$ s, inductive load is zero and capacitive load exists. from the Simulation result, it illustrate that the reactive power compensation effect is obvious and rapid.

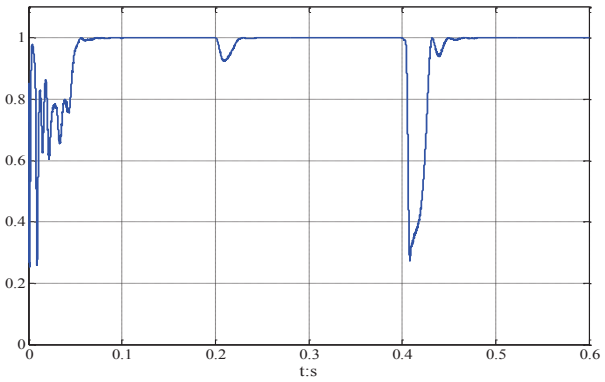


Fig. 10. Diagram of power factor

6 CONCLUSION

A 17-level high-power STATCOM based on ADRC is presented in this paper. The proposed framework includes the schematic of CHB multilevel converter, the operation principle is given and discussed. CSP-PWM is applied in STATCOM and the control signal of 17-level CHB multilevel inverter is obtained by using the active-reactive current decoupling control. Secondly, an appropriate reactive current decoupling controller is presented, which compensates in real time and generates ac currents of the CHB based STATCOM that tracks their references with small ripples. Thirdly, the method of energy balance inside the converter is discussed and it shows that the CHB can regulate DC capacitor voltages at a predetermined level well. Finally, simulation results show that the switch can work with low switching frequency.

The proposed controller can perform well in lower switching power losses and higher energy efficiency, as well as heat dissipation reduction and smaller dimensions of the converter. Simulation results verify that the proposed method is verified as an efficient way of reactive power compensation, and simultaneous controlling and balancing the DC side voltages during the working states.

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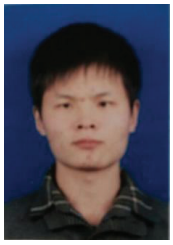

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