A Design of a High-Performance Analog Front-End for Passive UHF RFID Tag EPC C1G2

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Original scientific paper

***Abstract*—This paper introduces a high-performance analog front end for passive UHF RFID tag compatible with the EPC Class-1 Generation 2 (EPC C1G2) standard protocol. The proposed front end of a passive tag which contains the following modules: a power generation circuit which is composed of a matching circuit and an RF-limiter circuit, an NMOS rectifier, a DC limiter, a voltage regulation, a modulation and ASK demodulation circuit, a power-on-reset circuit, a ring oscillator which generates a clock of 1.28 MHz. The originality of this work is the proposal of a voltage regulation circuit composed of two distinct LDO regulators that share the same reference voltage and are designed to generate a Vdd1 (0.5 V) for the analog supply and Vdd2 (1 V) for digital power supply, under conditions of 50 Ω antenna, 900 MHz, a sensitivity of -24 dBm and a maximum consumption of 1 µW. The operating distance of the RFID is more than 25 meters based on the regulated 4 W effective isotropic radiated power (EIRP). The chip area of the proposed analog front end is only 79 µm × 83 µm. The simulation results in 90 nm CMOS process confirm the performance of the proposed analog front-end.**

***Index Terms*—Radio frequency identification (RFID), front-end, ultra-high frequency (UHF), RFID Tag, regulator, clock.**

I. INTRODUCTION

The ultra-high frequency (UHF) passive radio frequency identification (RFID) tags are showing a wide range of prospective applications due to their advantages of low cost, long operating distance, high data rate, and small antenna size [1].

The passive RFID tags working at frequencies between 860 MHz to 960 MHz, and 2.4 GHz are suitable for long distance identification. Long distance identification is important in warehouse monitoring, supply-chain management, logistics, and many other areas [2], [3].

The RFID tags are classified into three types of RFID tags, especially passive [4], [5], semi-passive [6], or active.

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The active RFID tags are used in some applications due to their higher communication range and their simpler structure where there is no need to extract power from the input signal. Today the majority of RFID tags is passive; occupy a major part of the market because they do not need battery where the power is extracted from the reader transmitted RF signals [7]. In order to have a higher operating range, the minimization of energy consumption is extremely important when designing all aspects of the passive label circuit [8].

The figure 1 shows the building blocks for a passive RFID tag system. Therefore, the analog front-end operates in the following way: The rectifier converts the received RF electromagnetic wave into a DC signal. The output of the rectifier must be connected to a voltage regulator in order to obtain a stable voltage supply Vdd for the digital section and the analog front-end. Furthermore, the ASK demodulator (ASK: Amplitude Shift Keying) extracts out the data symbols (Data-in) which are embedded in the carrier waveforms. The backscatter modulation is obtained by switching the input impedance between two reflection states as dictated by the signal Data-out. The power-on-reset is responsible for generating the reset signal for the digital section and the clock generator generates the clock frequency for the digital section.

In this paper a high-performance analog front-end for the UHF passive RFID tag is proposed in compliance with the EPC C1 G2 standard [7]. The goal for the design of this tag is to maximize the read range while providing a full compliance with the protocol. The energy received by the tag depends on the reading distance. Indeed, if the reading distance is large then the energy received by the tag antenna decreases. The tag is entirely passive and relies on the energy provided by the incident radiation. It must receive sufficient energy to power all the tag circuits.

The analog front-end is one of the key elements in passive tags, including these diverse operations as the power generating circuit, the modulation circuit, the ASK demodulation circuit of the incident RF signal, the power on reset and the clock generator.

We are particularly interested by the power generation circuit which contains the matching circuit, the RF-limiter, the NMOS rectifier, the DC-limiter and the voltage regulation circuit. With the RF-limiter circuit and the NMOS rectifier has been already improved by another work that we published in

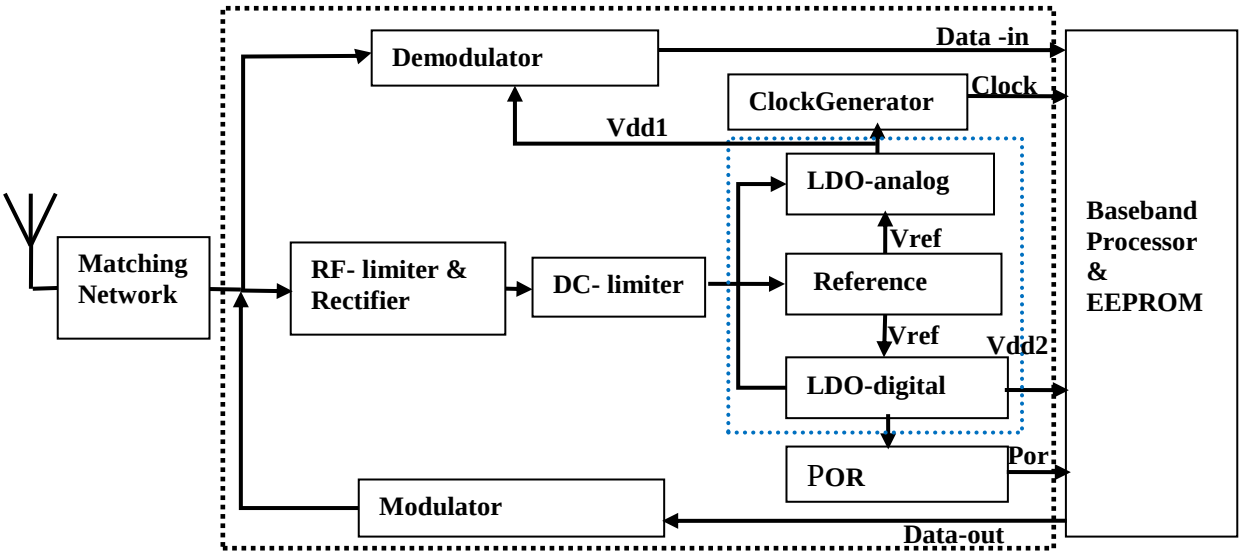

Fig.1. Block diagram of the Passive UHF RFID tag

[9] then the improved voltage regulation circuit will be the subject of this work.

In order to minimize consumption power for our system, we propose a reduction in the supply voltage of the analog circuits of 0.5V while maintaining a supply voltage to the digital part 1V. Thus, we will propose a voltage regulation system composed of two LDO regulators (LDO: Low Dropout) that share the same voltage reference. They are designed to generate two voltages. A voltage of 0.5 V noted Vdd1 which serves for the supply of the analog part and a voltage of 1V noted Vdd2 which serves for the supply of the digital part. To significantly reduce the energy consumption, we have designed the voltage reference and the amplifiers such a way that the transistors operate in the sub-threshold region.

The proposed system requires a minimum -24dBm input power with a 50Ω antenna at 900MHz.

A theoretical analysis and design techniques of the proposed power generating circuit, is presented in Section II. The clock generator is described in section III. In section IV, the design of the power -on-reset is presented. The ASK demodulator is addressed in section V.

The simulation results of the analog front-end proposed are presented in Section VI, followed by the conclusion in section VII. The technology used in this paper is 90 nm CMOS.

II. Power Generating Circuit

This circuit consists of the impedance matching circuit, the RF-limiter circuit, the NMOS Rectifier, the DC-Limiter and the proposed voltage regulation. The impedance matching circuit is required to ensure the maximum RF energy is transferred from the source to the load. The input impedance of a rectifier is generally much higher than the source impedance. The standard RF source impedance is considered 50Ω. The voltage sat the antenna of an RFID system can change from 300 mV to 20V, depending on the vicinity of the reader to the tag [10]. To prevent any damage to transistors at high voltage levels. The RF-limiter is used to ensure that under large RF power levels the voltage swing at the chip input is limited to a fixed value. The RF-limiter acts like a bypass system for the extra current during the large input power.

The NMOS rectifier is another work that we published in [9] converts a part of the RF signal power to DC for power supply for all active circuits on the chip. The efficiency of a rectifier decreases with an increasing number of rectifier stages [11]. Additionally, the working distance of RFID varies dramatically, so the dynamic range of RF input power may be as high as 30dB. In order to make all the circuits work normally, the power supply cannot be too high. The DC-limiter is another work that we published in [9] is needed to limit the power amplitude when the rectifier is in the near field.

The output of the NMOS rectifier must be connected to a voltage regulator. The regulator has taken two main functions: Regulate the front-end output voltage to a preferred value and within a preferred range and protect the inner circuits from breaking at high RF input power. Moreover, RFID tags are usually placed in harsh environments; such that, the operation of a regulator also needs to operate over a wide range of temperature and supply voltage variations. From all the requirements, the series LDO voltage regulator is preferred to use as the regulator topology. Fig.2 shows the block diagram of the proposed voltage regulation. Another, to avoid the interference of the digital switching noise in to the sensitive analog supply voltage [12], two separate LDO regulators, that share the same voltage reference are designed to generate a

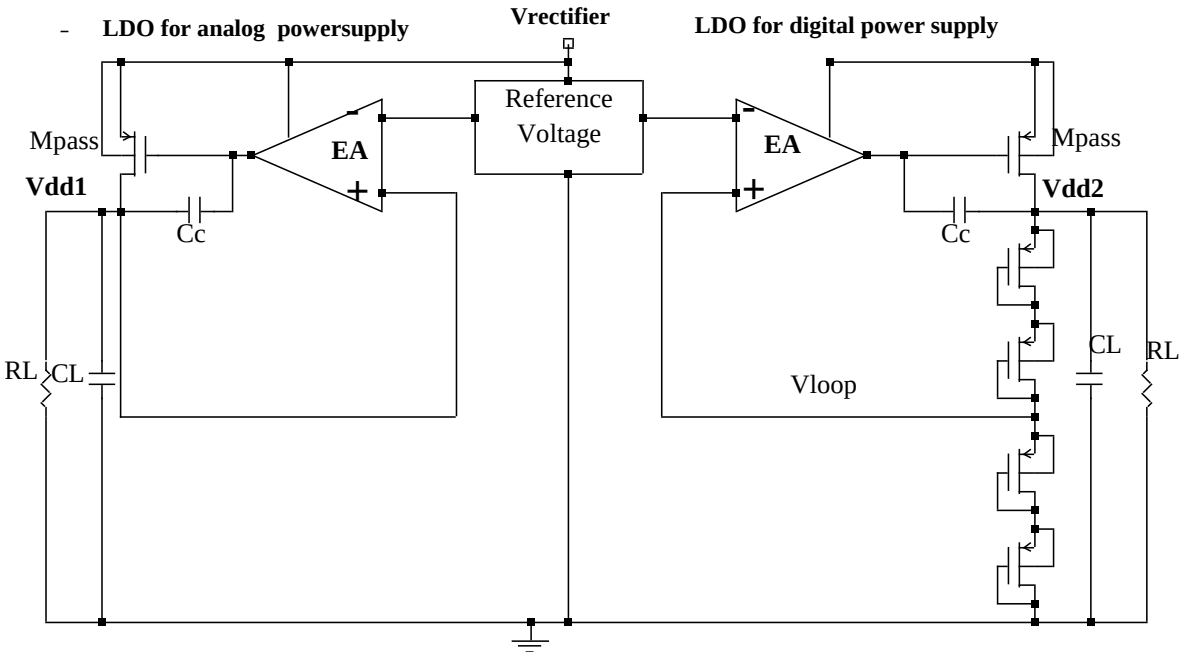

Fig.2. Diagram of the proposed voltage regulation

Vdd1 (0.5V) for the analog power supply and Vdd2 (1V) for the digital power supply respectively.

C.1 Reference voltage generator

The figure 3 shows the schematic of the reference voltage generator, which is a variant of the generator proposed in [13],[14]. The latter composed by current source current source sub-circuit and bias voltage sub-circuit. The former generates a bias current (I_{GS}), while the latter accepts IGS and produces the output voltage (V_{ref}). Under a small supply voltage, most transistors will work in the subthreshold region. The characteristic equation of a transistor operating in the subthreshold region can be expressed as [13].

In this design, the reference voltage is 504mV for the supply voltage of 1.2V with line regulation of 0.9mV/V. The temperature ranges from −30°C to 50°C, with the TC of 12ppm/°C.

C.2 Series Voltage Regulator

The schematic of LDO is shown in Fig. 3, where the OPA(error amplifier) compares the feedback signal from V_{reg} with V_{ref} before producing an error signal to drive the pass device M_{Pass} for the constant V_{reg}.

The feedback signal is generated by a voltage divider, which consists of four diode connected transistors ($M_{f1} \sim M_{f4}$). The stability of V_{reg} strongly depends on the bias current I_{SS} of the OPA, as shown in the following equation:

$$\frac{\Delta V_{reg}}{\Delta I_{SS}} \cong -\frac{(\frac{r_{on} \parallel r_{op}}{2}) g_m p_{ass} (r_{oPass} \parallel R_L)}{1+(\frac{r_{on} \parallel r_{op}}{2}) g_m p_{ass} (r_{oPass} \parallel R_L) \frac{g_{mR} R_{f3,4}}{R_{f3,4}+R_{f1,2}}}$$

$$\cong -\frac{1}{g_{mR}} \frac{R_{f3,4}+R_{f1,2}}{R_{f3,4}} \quad (1)$$

where $r_{on}(r_{op})$ is the output resistance of NMOS (PMOS) transistor, r_{oPass} and R_L the output resistance of M_{Pass} and the load resistor, g_{mR} and $g_m p_{ass}$ the transconductance of NMOS in the differential pair and M_{Pass}, and $R_{f1,2}$ and $R_{f3,4}$ are the equivalent resistance of M_{f1} to M_{f4}, respectively.

The regulated voltage variation caused by ΔV_{DD} (line regulator) can be approximated as

$$\frac{\Delta V_{reg}}{\Delta V_{DD}} \cong -\frac{\dfrac{g_{mPass} r_{oPass} R_L}{r_{oPass} + R_L}}{\dfrac{g_{mR}(r_{on} \parallel r_{op}) g_{mPass}(r_{oPass} \parallel R_L) R_{f3,4}}{R_{f3,4} + R_{f1,2}}}$$

$$\cong \frac{1}{g_{mR}(r_{on} \parallel r_{op})} \frac{R_{f3,4} + R_{f1,2}}{R_{f3,4}} \quad (2)$$

Where $g_{mR}(r_{on} \parallel r_{op})$ represents the voltage gain of the differential amplifier. The effect of load current on the regulated voltage (load regulation) can be approximated as

$$\frac{\Delta V_{reg}}{\Delta I_L} \cong \frac{r_{o,Pass}}{1 + A_V P_2 F_B}$$

$$\cong \frac{r_{o,Pass}}{g_{mR}(r_{on} \parallel r_{op}) g_{mPass}(r_{oPass} \parallel R_L) \dfrac{R_{f3,4}}{R_{f3,4} + R_{f1,2}}} \quad (3)$$

From (1) and (3), a high voltage gain of the amplifier with large channel length for transistors MR1 and MR2 will help improve both LIR and LOR. In addition, the output resistance of the pass device can be reduced by using short channel PMOS transistor.

The proposed voltage regulator is implemented in 90 nm CMOS technology. The output voltage is 1.01 V with line regulation of5.9 mV/V. The load regulation is estimated to be 76.21 μV/49 μA. The PSRR (power supply rejection ratio) for the regulated voltage is −65.4dB at 100Hz and −60.5dB at 1MHz. The temperature ranges from −30 °C to 50 °C, with the TC of 31.3 ppm/°C. The gain and the phase margin are 80.6 dB and 89.7° respectively, show that the voltage regulator is stable. Fig 3.1 shows the output Vdd1 &Vdd2 of the proposed voltage regulation.

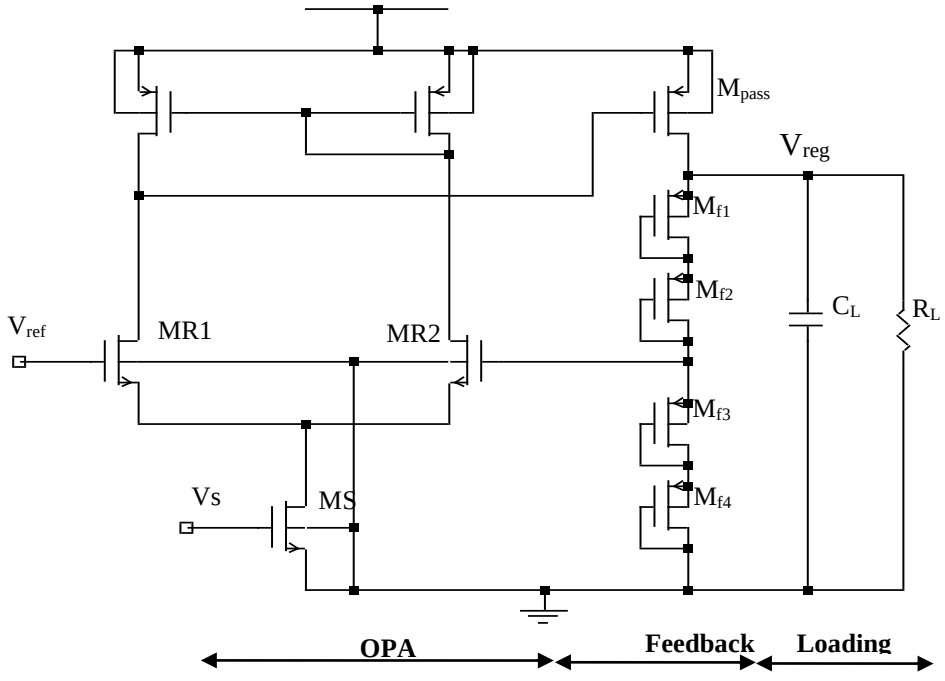

Fig.3. The schematic of LDO regulator

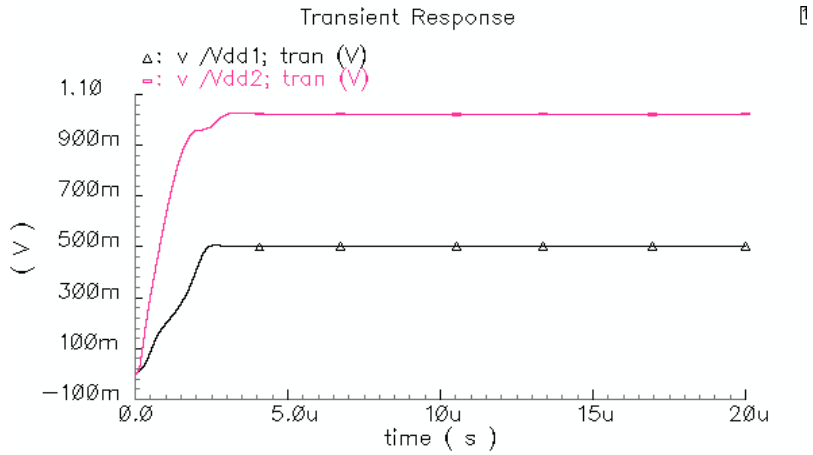

Fig.3.1. Output Vdd1 &Vdd2 of the proposed voltage regulation

III. Clock Generator

The clock generator is needed for the digital section to run and to decode the data. Depending on the system, the clock can be either generated on chip or it can be extracted from the incoming carrier signal. For RFID technology for generating the internal clock there are different circuits that can be used such as current starved ring oscillators, relaxation oscillators, and phase locked loop (PLL), although the latter consumes too much power so it is normally not recommended for RFID.

The ring oscillators can have different amounts of stages, with the output of the last stage fed into the input of the first stage. They have the advantage of being able to operate without bulky passive components such as capacitors, resistors and inductors, making them the preferred topology
as they consume less power and take up less area, which are the most important factors when it comes to clock generators [15].

Today the electronic product- code Class-1 Generation-2 (EPC C1G2) standard [15] is a major UHF RFID standard which ensures reliable data rates and better performance of RFID applications. According to the EPC C1G2 protocol, a system clock of at least 1.28 MHz is needed for the tag.

The ring oscillator proposed is shown in Fig.4. The control current tunes the oscillation frequency and the W/L ratio of the MOS transistors is dimensioned so that with the control current of 65.5 nA at a power supply of 0.5V.

Table 1 shows the ring oscillator parameters and Fig.4.1 shows output of the oscillator has a nominal frequency of 1.28 MHz.

TABLE I
The Ring Oscillator Parameters

Oscillation Frequency	Duty cycle	Power consumption
1.28MHz	30.86%	98nW

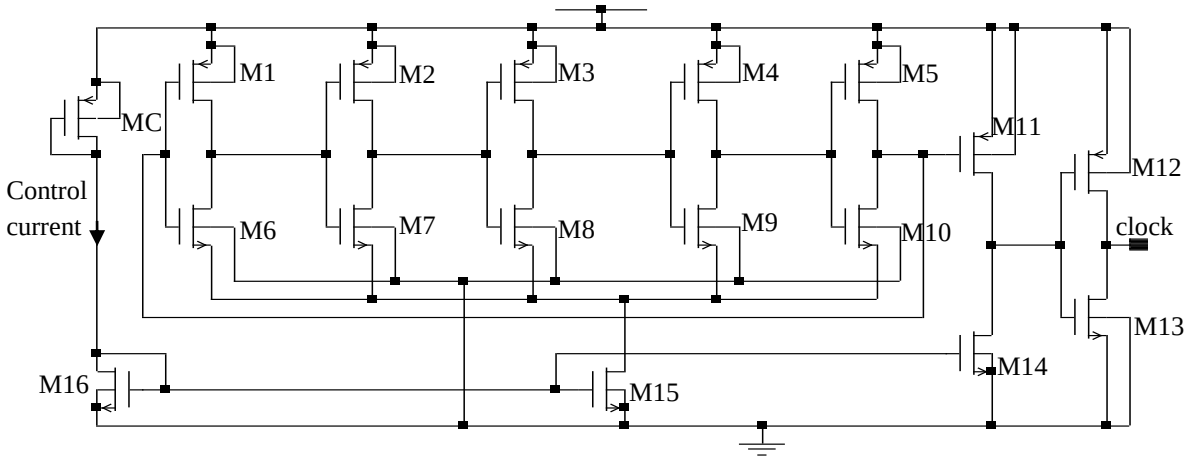

Fig.4. Schematic proposed of the ring oscillator

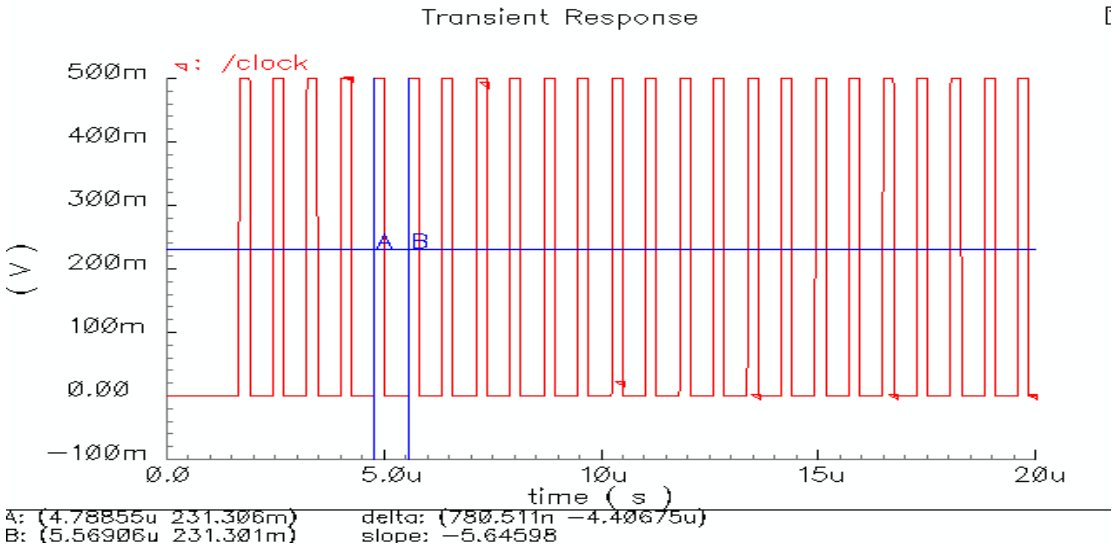

Fig. 4.1. Output of the ring oscillator

IV. Power–on – Reset

The power-on reset (POR) circuit, shows in Fig.5 is responsible for generating the reset signal for the digital section, as well as disconnecting the transponder to avoid malfunction once the required power falls below a certain level, fig.5.1 shows output Vdd2 & Por. Simply put, if the power supply voltage is lower than the reference voltage, the POR circuit has to release control of the baseband processor. If the power supply voltage level is higher than the reference voltage, the POR circuit has to generate the signals to reset and initiate operation of the digital synchronous baseband processor circuit [16].

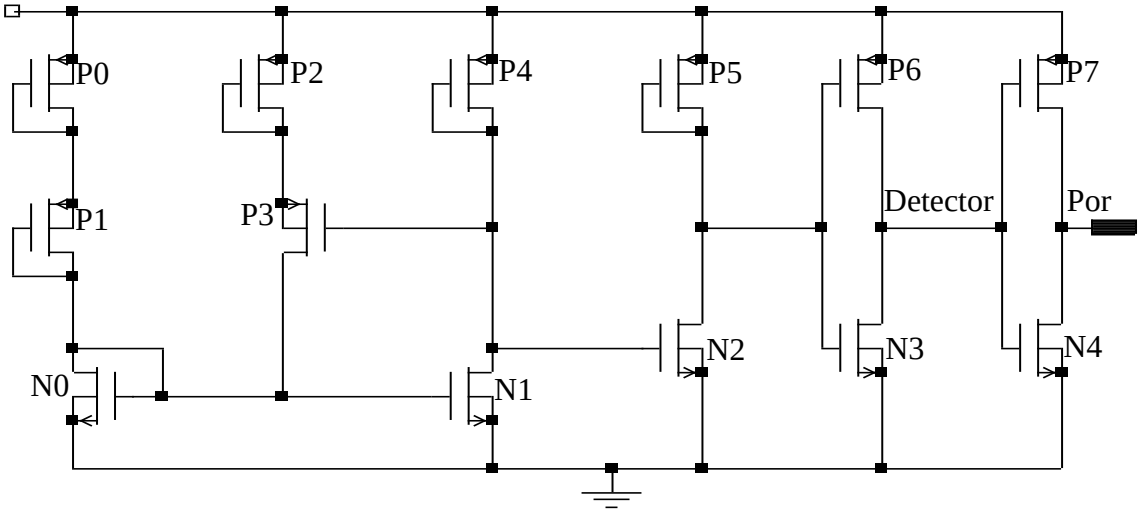

Fig.5. The schematic of power-on reset

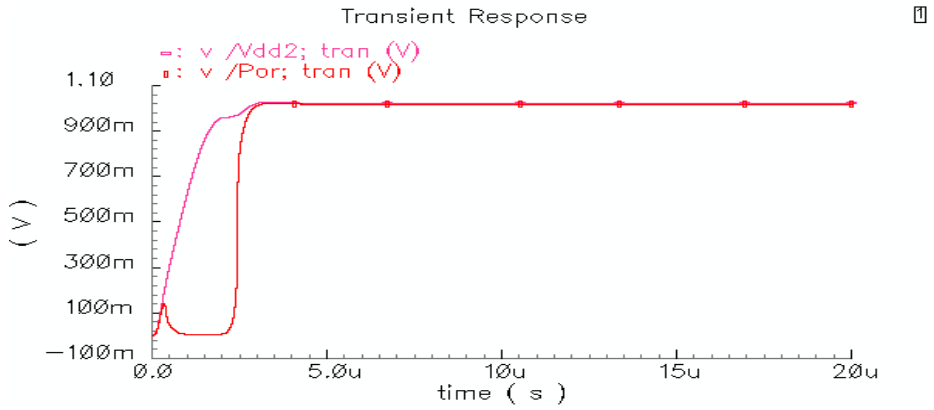

Fig.5.1. Output Vdd2 & Por

V. ASK DEMODULATOR

The block diagram of the demodulator part was shown in Fig. 6(d). The latter uses the envelope detection and comparison with the average of the input voltage to recover baseband data. The envelope detector, shows in Fig.6(c) is consists of a two-stage rectifier is transferred through a low pass filter to get its average value [17]. The envelope detector and its average value are then compared using a comparator with hysteresis. The comparator needs hysteresis for deal with the voltage ripple from the envelope detector.

The main parameter of comparator with hysteresis is the trip point, V_{TRP}, which is the threshold that the input has to reach before the output changes. There are two trip points, one is positive trip point, V_{TRP}^{+}, which the input has to reach when it goes from negative to positive before the output changes, and the other is negative trip point, V_{TRP}^{-}, which the input has to reach when going from positive to negative. Fig. 6(a) shows a schematic of comparator with internal hysteresis. For Vin1 is on ground, the positive trip point is given by (4) when Vin2 goes from negative to positive as

$$V_{TRP}^{+} = V_{GS2} - V_{GS1} = \left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} - \left[\left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1}\right] \quad (4)$$

When Vin2 reaches the trip point, Vo1 and Vo2 change its voltage. At the switching point, we have the relation between currents in transistors [18] as

$$i_1 = i_3 = \frac{i_5}{1+\left[(W/L)_6/(W/L)_3\right]}, i_2 = i_5 - i_1 \quad (5)$$

And when Vin2 goes from positive to negative, the negative trip point V_{TRP}^{-} is given by

$$V_{TRP}^{-} = -\left|\left(\frac{2i_2}{\beta_2}\right)^{1/2} + V_{T2} - \left[\left(\frac{2i_1}{\beta_1}\right)^{1/2} + V_{T1}\right]\right| \quad (6)$$

where $\beta_{1,2}$ and $V_{T1,2}$ are the transconductance and the threshold voltages of the transistors M1 and M2, respectively. Fig. 6(b) shows the simulation result of the designed comparator with Vdd1=0.5 V, Vin1=0V, V_{TRP}= ±60 mv.

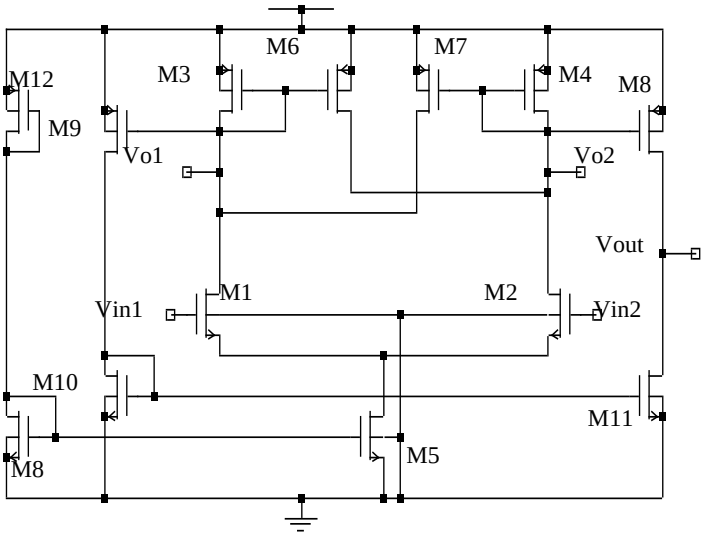

Fig.6. (a). Circuit schematic of comparator with internal hysteresis

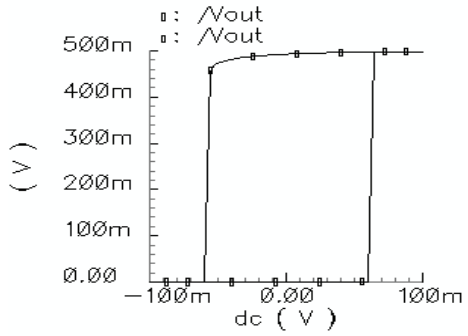

Fig.6. (b). Cycle hysteresis

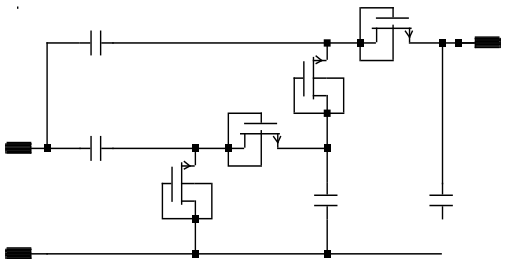

Fig.6. (c). Envelope detector

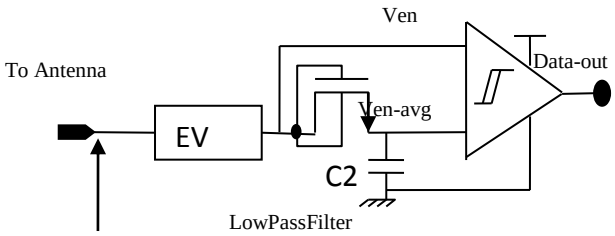

Fig.6. (d). Schematic of ASK demodulator

As a counter part of the demodulator, the return link modulator is another essential part of the RFID tag. By changing the tag IC's input impedance, the electromagnetic wave scattered back by the antenna is modulate [2].A passive RFID tag typically uses this mechanism for the return link. ASK backscatter modulation is used in our design. The schematic of the proposed modulator is shown in Fig.7. The switches in the backscattering circuit are realized using two minimum lengths NMOS and PMOS transistors with 1μm width in parallel to linearize the switch resistance in the large dynamic range of the input signal.

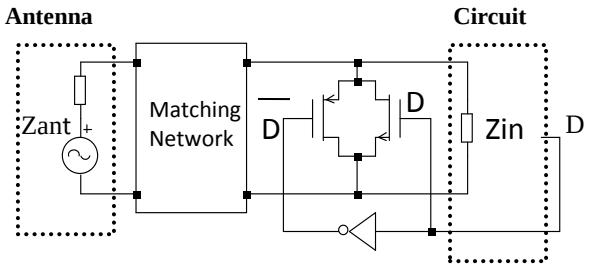

Fig.7. Schematic of the backscatter modulator

The input S11 reflection coefficient is shown as a function of frequency in Fig.8. The S11 at 900 MHz is around -38dB which illustrate a good matching at that frequency.

The communication range depends on the power reflection and can be calculated using the friis free space formula [15]:

$$r_{\max} = \frac{\lambda}{4\pi}\sqrt{\frac{P_t G_t G_r (1-|S11|^2)}{P_{th}}} \tag{7}$$

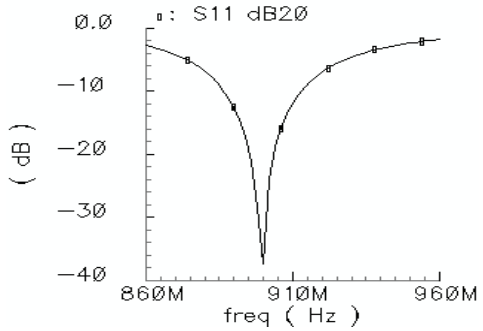

Fig.8. The S11 as a function of frequency

VI. Simulations Results

The simulation results of the main blocks of the analog front-end of the passive UHF RFID tag, is shown in Fig.9 (a), under conditions is 900 MHz, and the data rate is the 160 Kbit/s. The power consumption of the main blocks is shown in table 2. Table 3 compares the power consumption of this work to other reported work. The sensitivity of the analog front-end is -24 dBm to generate a Vdd1 (0.5 V) for the analog supply and Vdd2 (1 V) for digital power supply from a 50 Ω antenna at 900 MHz. The operating range of the RFID circuits is expressed in terms of wavelengths instead of frequency for more relevant comparisons.

A comparison among our RFID circuit and some previously reported works is summarized in table 4.

The Layout of proposed analog front-end is shown in Fig.9 (b).The size of whole chip is only 79 μm × 83 μm.

TABLE II
Power Consume of Main Blocks

Block	power generating circuit & Power-on-reset	Demodulator	Clock
Power Consume	476nW	367nW	98nW

TABLE III
Comparison of Power Consumption

Work	[2]	[19]	[20]	This work
Frequency (MHz)	900	900	900	900
CMOS process	0.5 μm	0.25 μm	0.18 μm	90 nm
Power consumption (μ W)	2.25μ	8μ	2.2μ	0.941 μ

TABLE IV
COMPARISON RESULTS

Ref.	Efficiency	Minimum Input Power	Range	Carrier Frequency	Process
This work	**28%**	**4.2µW****	**77.6λ*****	**900MHz**	**90 nm CMOS**
[9]	26.96%	5.01µW **,15.8 µW*	70.8λ***	900MHz	90 nm CMOS
[2]Schottky Diodes	14.5 %	_	28.2λ	900MHz	0.5 µm CMOS
[21]	10.94%	63µW *	21.3λ***	450MHz	0.25µm CMOS

* Normalized for 3V generation,**Normalized for 1V generation, *** Normalized for 4W EIRP source

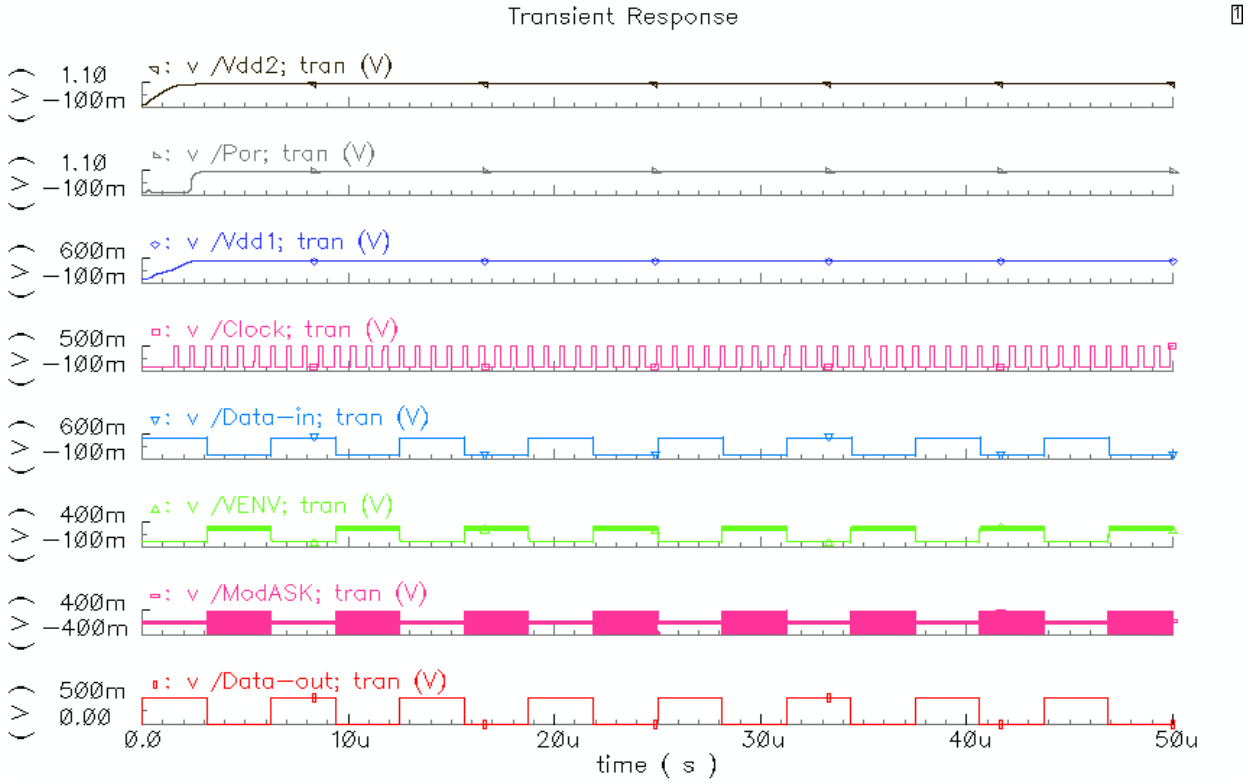

Fig.9.(a). Simulation results of the whole main blocks of the analog front-end

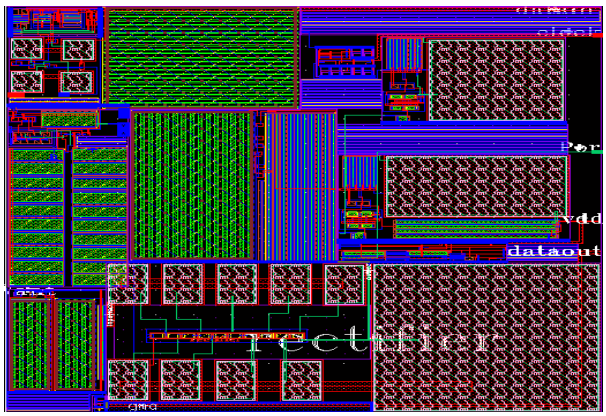

Fig.9.(b).Layout of proposed analog front-end

VII. CONCLUSION

This paper presented a high-performance analog front end for passive UHF RFID tag, which is designed by using the 90 nm CMOS process, consisting of a power generating circuit which consists of the matching & the RF-limiter, the NMOS rectifier, the DC-limiter and the proposed voltage regulation. The modulation and demodulation, power-on-reset, clock generator. The whole analog front-end circuit consumes only 941nW and works in low voltage, 1V. The simulations have been done to verify the proposed ideas.

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