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Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: 0005-1144 (Print) 1848-3380 (Online) Journal homepage: http://www.tandfonline.com/loi/taut20

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To cite this article: Ardavan Kianpour & Ghazanfar Shahgholian (2017) A floating-output interleaved boost DC–DC converter with high step-up gain, Automatika, 58:1, 18-26, DOI: 10.1080/00051144.2017.1305605

To link to this article: https://doi.org/10.1080/00051144.2017.1305605

Published online: 03 Apr 2017.

AUTOMATIKA, 2017
VOL. 58, NO. 1, 18–26
https://doi.org/10.1080/00051144.2017.1305605

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A floating-output interleaved boost DC–DC converter with high step-up gain

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ABSTRACT

A new interleaved boost converter with high step-up gain is presented in this paper. The proposed topology integrates coupled inductors and floating-output capacitors technique into interleaved boost converter to provide high step-up voltage gain without extreme duty cycle. The voltage stress on the power switches and diodes is very low, so low-cost and high-performance semiconductor devices can be employed. Also, the reverse recovery problem of all diodes is mitigated and zero-current-switching (ZCS) turn-on operation of the main switches is established as well. In addition, the passive clamp circuits are employed to suppress the voltage spikes across the main switches during turn-off instants. The operating principles and steady-state analysis of the proposed converter in continuous condition mode are explained. Finally, the simulation and experimental results of prototype 25–400 V circuit with 200 W output power are provided to verify the performance of presented topology.

ARTICLE HISTORY
Received 9 November 2016
Accepted 1 March 2017

KEYWORDS
High step-up converter; interleaved; coupled inductors; floating output

1. Introduction

High step-up DC–DC converters are employed in numerous applications, such as renewable energy systems, motor drives, uninterruptible power systems and electric vehicles [1–6]. In these applications, a high step-up converter is required to adapt the low voltage level of batteries or photovoltaic cells to the high-voltage DC bus [7,8]. In order to perform this voltage conversion, various isolated DC–DC converters are presented in which high voltage gain can be achieved by increasing the transformer turns ratio [9,10]. Nevertheless, these converters suffer from high circulating currents, high voltage stress and low efficiency [11,12].

According to the recent studies, non-isolated DC–DC converters are favourable in high step-up application due to lower size, lower circuit cost and higher efficiency than the isolated types [13]. Conventional boost and buck-boost converters theoretically have a high voltage gain. However, due to many limitation factors, such as equivalent series resistance of the passive elements and reverse recovery problem of the output diode, a high step-up gain cannot be achieved in practice [14–16]. In order to reduce the switches voltage stress in high step-up applications, conventional three-level boost converter can be used. Also, the size of the input inductor is lower than the boost converter [17,18]. However, the voltage gain is still limited. Conventional cuk, sepic and zeta converters can be employed as a high step-up converter, but they are more complex than the boost converter [19,20]. Some efforts are made to combine sepic and boost converters. But despite using further elements, the voltage gain is limited [21,22].

Cascade technique is a simple approach to providing high voltage gain [23,24]. However, these converters need two individual magnetic cores, which increase circuit cost and complexity. Also, due to double power processing, the whole converter efficiency is low. Coupled inductors (CI)-based boost converters are widely used to improve the voltage gain, since the CI turns ratio provide a control freedom in addition to the duty cycle. Also, owing to the leakage inductance of coupled inductors the zero-current-switching (ZCS) turn-on operation of the main switch is accomplished and the reverse recovery problem of output diode is suppressed [25–28]. Despite single-phase CI converters advantages, the pulsating input current ripple reduces the input capacitor lifetime [29]. In order to reduce the input current ripple, interleaved boost converters with winding cross-coupled inductors (WCCI) are presented [30–34]. In these topologies, passive or active clamp circuits are employed to absorb the leakage inductor energy and provide soft switching operation. In [35–37], some interleaved boost converters with voltage multiplier cells are presented. Owing to using the WCCI technique and voltage multiplier cell, an extendable high step-up voltage gain is provided and the input current ripple is conspicuously low. Also, the automatic current sharing feature is established due to using series capacitors between the two interleaved phases. Some interleaved boost converters with series capacitors and voltage multiplier cells are presented

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in [38,39], which have a voltage gain higher than the conventional interleaved boost converter. In [40], an interleaved boost converter with floating-output capacitors is introduced. In this topology, the input voltage source is connected in series with output capacitors to provide high voltage gain. Also, the diodes and switches voltage stress is lower than the conventional interleaved boost converter.

In this paper, a new interleaved boost converter is presented for high step-up applications. The proposed converter encompasses a high voltage gain without extreme duty cycle and low voltage stress across the semiconductor devices with the same number of MOSFET switches in comparison with the conventional interleaved boost converter. Also, the leakage inductor of the coupled inductors provides ZCS turn-on operation of the main switches and alleviates the reverse recovery problem of all diodes. Furthermore, the passive clamp circuits are used to absorb and recycle the leakage energy into the circuit, which leads to suppressing the voltage spikes across the main switches. Thus, low-voltage MOSFET switches with low ON-resistance can be employed to reduce the conduction losses. The remainder of this paper is arranged as follows. In Section 2, the operating principles of the proposed converter in continuous condition mode (CCM) are discussed in details. Steady-state analysis and features of the proposed converter are analysed in Section 3. Simulation and experimental results are presented in Section 4. This paper concludes with some final remarks in Section 5.

2. Proposed converter and operating principles

The circuit configuration of the proposed converter is shown in Figure 1. This converter is based on two CI boost converter modules, which are interleaved connected at the input and series connected at the output. The input gate signals of the converter switches have a 180-degrees phase shift which causes interleaved operation of two modules. In this topology, inductors L_{1l} and L_{2l} comprise the two coupled inductors. Switches S_1 and S_2 are the main switches and diodes D_1 and D_2 are the output-rectifying diodes of the boost converter. Diodes D_{C1} and D_{C2} along with capacitors C_{c1} and C_{c2} comprise two passive clamp circuits which recycle the leakage inductors energy and limit voltage stress on the main switches. In order to simplify the operating principles analysis of the proposed converter, some assumptions are made as follows:

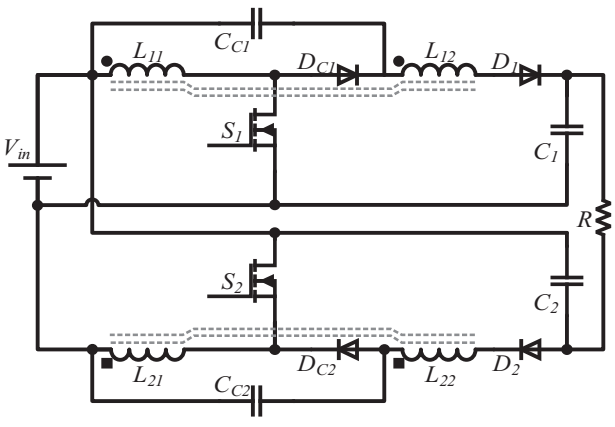


Figure 1. Circuit diagram of the proposed converter.

- All diodes and MOSFET switches are considered to be ideal.
- All capacitors are large enough. Hence, their voltage ripple can be neglected.
- The operating duty cycle of the main switches S_1 and S_2 is equal.
- The coupled inductors are modelled as a magnetizing inductor, a leakage inductor and an ideal transformer with $n = n_{12}/n_{11} = n_{22}/n_{21}$ turns ratio.

The typical waveforms of the proposed converter at steady-state condition are given in Figure 2. According to the following considerations, the proposed converter has eight operating modes during one complete switching cycle. Owing to the symmetrical operation of switches S_1 and S_2, only four operating modes of switch S_1 are explained. The equivalent circuit of each mode is shown in Figure 3. Before t_0, both switches S_1 and S_2 are ON and the magnetizing inductors L_{M1} and L_{M2} are charged through the input.

Mode 1 $[t_0 - t_1]$: At t_0, switch S_1 is turned off and clamp diode D_{C1} starts to conduct. During this mode, a part of magnetizing inductor current i_{LM} transfers to the output via the secondary side of the coupled inductors and diode D_1. Also, the leakage energy which stores in L_{lk1} is absorbed by the clamp capacitor C_{c1}. Therefore, the leakage inductor current i_{Llk1} decreases linearly.

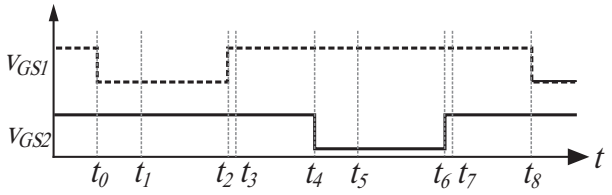
At t_1, i_{Llk1} reaches zero and this mode ends. During this interval, the equations of the leakage inductor and the magnetizing inductors currents are as follows:

$$i_{L_{lk1}}(t) = I_{L_{m1}}(t_0) - \frac{V_{Cc1} - \frac{1}{1+n}.(V_{C1} - V_{in})}{L_{lk1}}.(t - t_0). \quad (1)$$

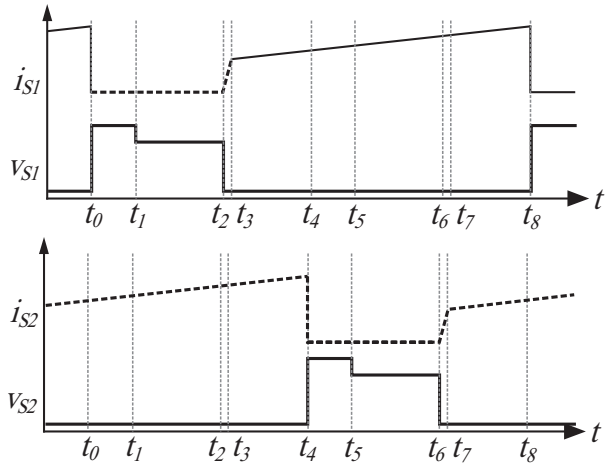
$$i_{L_{m2}}(t) = i_{L_{lk2}}(t) = I_{L_{m2}}(t_0) + \frac{V_{in}}{L_{m2} + L_{lk1}}.(t - t_0). \quad (2)$$

Mode 2 $[t_1 - t_2]$: At t_1, the leakage inductor current becomes zero and the clamp diode D_{C1} is turned off without any reverse recovery problem. During this mode, the magnetizing inductor current i_{LM} is charging the output capacitor C_1 through the secondary side of the coupled inductors. Thus, i_{LM} is decreasing linearly as follows:

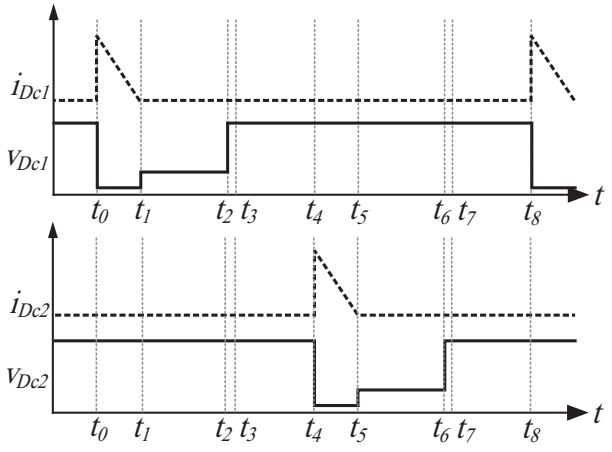
$$i_{Lm1}(t) = I_{Lm1}(t_1) + \frac{V_{C1} - V_{Cc} - V_{in}}{L_{m1}}(t - t_1). \quad (3)$$



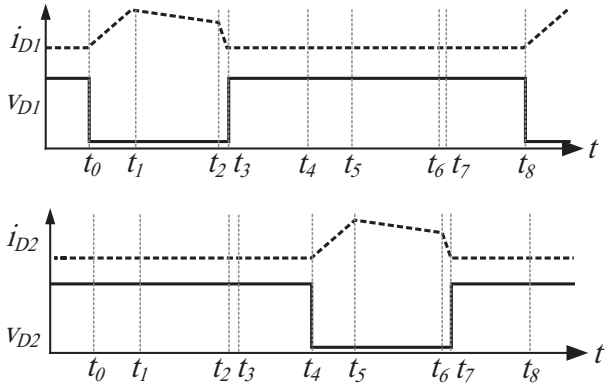
(a) Gate source voltage of the switches S_1 and S_2



(b) Waveforms of voltage and current of the switches S_1 and S_2

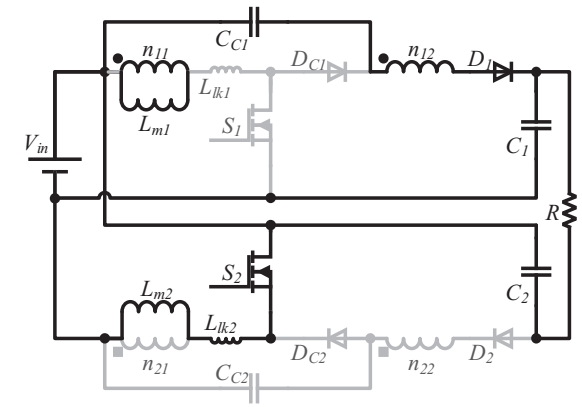


(c) Waveforms of voltage and current of the diodes D_{C1} and D_{C2}

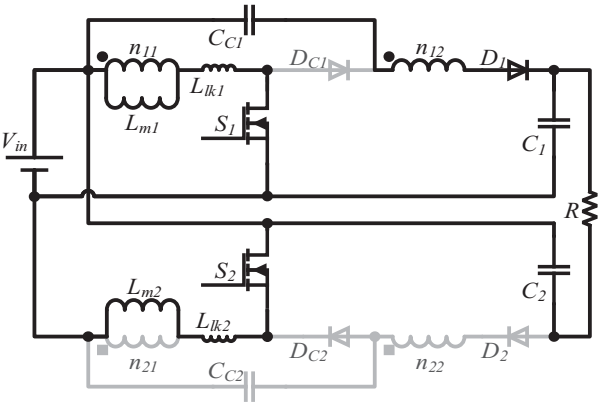


(d) Waveforms of output diodes D_1 and D_2

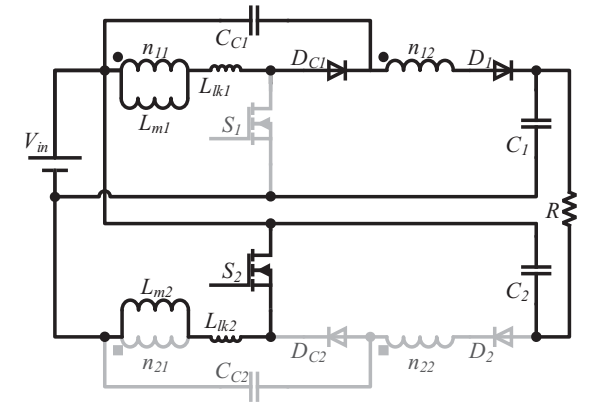
Figure 2. Typical waveforms of the proposed converter.



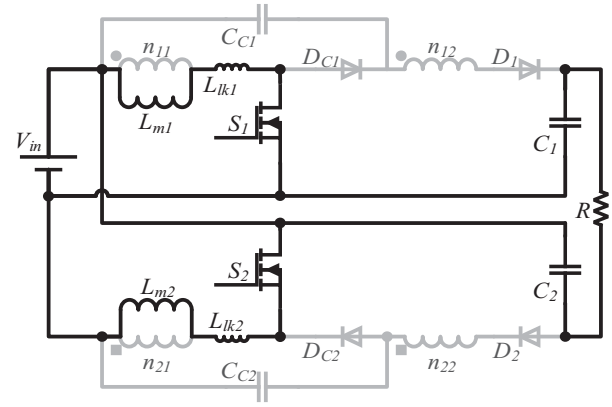
(a) Mode I



(b) Mode II



(c) Mode III



(d) Model IV

Figure 3. Equivalent circuit of the operating modes.

Mode 3 $[t_2 - t_3]$: At t_2, switch S_1 is turned on. Owing to the leakage inductor L_{lk1}, switch S_1 is turned on under ZCS conditions. During this mode, the leakage inductor current i_{Llk1} is increasing linearly. At t_3, the magnetizing inductor and the leakage inductor currents become equal and the diode D_1 is turned off with no reverse recovery problem. Following equations represent the leakage inductor and the diode D_1 currents in this interval:

$$i_{L_{lk1}}(t) = \frac{V_{in} + \frac{V_{C1} - V_{C_{C1}} - V_{in}}{n}}{L_{lk1}}(t - t_2). \quad (4)$$

$$i_{D1}(t) = \frac{1}{n}\left[I_{Lm1}(t_2) - \frac{V_{in} + \frac{V_{C1} - V_{C_{C1}} - V_{in}}{n}}{L_{lk1}}(t - t_2)\right] \quad (5)$$

Mode 4 $[t_3 - t_4]$: At t_3, both switches S_1 and S_2 are ON and all rectifying diodes are OFF. The leakage and magnetizing inductors are charged via the input voltage source V_{in}. Also, the capacitors C_1 and C_2 along with V_{in} provide energy to the output load R_L. During this mode, equations of the magnetizing and leakage inductors currents are expressed as follows:

$$i_{L_{m1}}(t) = i_{L_{lk1}}(t) = I_{Lm1}(t_3) - \frac{V_{in}}{L_{m1} + L_{lk1}}.(t - t_3)] \quad (6)$$

$$i_{L_{m2}}(t) = i_{L_{lk2}}(t) = I_{Lm2}(t_3) - \frac{V_{in}}{L_{m2} + L_{lk2}}.(t - t_3)] \quad (7)$$

3. Steady-state performance analysis of the proposed converter

To simplify the steady-state analysis, the mode 1 is neglected since the duration of this mode is very short.

3.1. Conversion ratio

Due to voltage-second balance for the inductors of all switching circuits, voltage-second balance can be written for inductors L_{m1} and L_{m2} which results in the following equation [41]:

$$V_{in}DT = (V_{C1} - V_{Cc1} - V_{in})(1 - D)\,T \quad (8)$$

Also, in this circuit, due to large values of capacitors and for simplicity of voltage relationships, C_1 and C_2 are considered identical:

$$V_{C1} = V_{C2} = V_C = \frac{V_o - V_{in}}{2}. \quad (9)$$

According to the mode 3, the clamp capacitors C_{c1} and C_{c2} recycle the energy of leakage inductors. By applying the KVL principle, the voltages of C_{c1} and C_{c2} are determined as follows:

$$V_{Cc1} = V_{Cc2} = V_{Cc} = \frac{V_{C1} - V_{in}}{1 + n} = \frac{D}{1 - D}V_{in}. \quad (10)$$

By substituting (10) and (9) into (8), the voltage gain of the proposed converter is obtained as follows:

$$\frac{V_o}{V_{in}} = \frac{1 + (1 + 2n)D}{1 - D}. \quad (11)$$

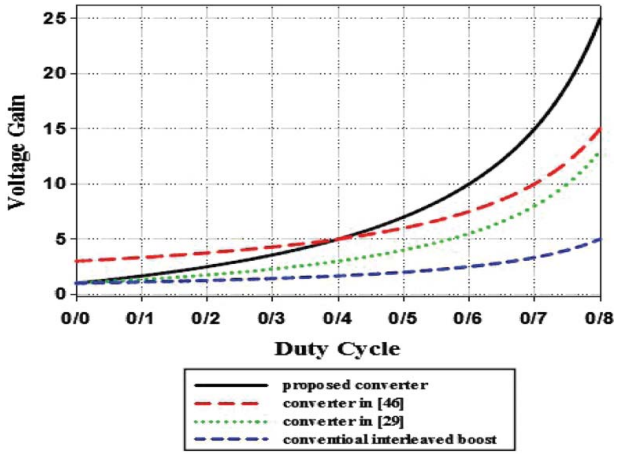


Figure 4. Voltage gain comparison of the proposed converter.

Figure 4 shows a comparison between the proposed converter and some other similar interleaved DC–DC topologies in terms of voltage gain. To make a fair comparison, the coupled inductors turns ratio (n) is considered equal to 2. As can be observed, the proposed converter has a higher voltage gain than the conventional interleaved boost converter and the converters presented in [42,43]. The interleaved converter, which is presented in [44], has a higher voltage gain in duty cycles below 0.4. However, in duty cycles higher than 0.4, which is favourable in high step-up applications, the voltage gain of proposed converter goes out the voltage gain of [45]. Hence, the proposed converter is an appropriate topology for applications, where a high step-up conversion ratio is required.

3.2. Voltage stress on semiconductor devices

According to the foregoing analysis, the voltage stress on the main switches, clamp diodes and output diodes of the proposed converter is derived as follows:

$$V_{S1} = V_{S2} = \frac{V_o}{1 + (1 + 2n)D} \quad (12)$$

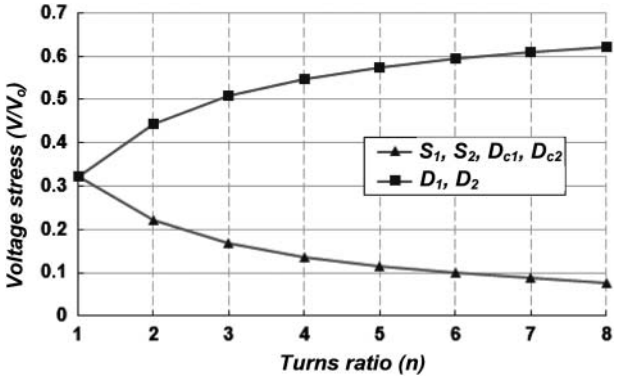


Figure 5. Voltage stress diagram of the semiconductor devices.

$$V_{Dc1} = V_{Dc2} = \frac{V_{in}}{1-D} = \frac{V_o}{1+(1+2n)D} \quad (13)$$

$$V_{D1} = V_{D2} = \frac{nD}{1-D} V_{in} = \frac{nV_o}{1+(1+2n)D} \quad (14)$$

The normalized voltage stress graph of the semiconductor devices versus the coupled inductors turns ratio is plotted in Figure 5. It can be observed that the voltage stress on the main switches and clamp diodes is reduced as the coupled inductors turns ratio increases. On the other hand, the voltage stress on the output diodes is increased. Therefore, the coupled inductors turns ratio should be designed properly to minimize the voltage stress on the main switches and diodes.

3.3. Passive elements design

Regarding the desired current ripple on the magnetizing inductors ΔI_{Lm} in CCM operation, the values of L_{M1} and L_{M2} are calculated as follows:

$$L_{M1} = L_{M2} = \frac{DV_{in}}{f_s \Delta I_{Lm}}. \quad (15)$$

The leakage inductor of the coupled inductors causes ZCS turn-on of the main switches S_1 and S_2. Hence, to accomplish the ZCS condition for the main switches, the value of the leakage inductors L_{lk1} and L_{lk2} is obtained as follows:

$$L_{lk1} = L_{lk2} \geq \frac{V_{Llk}.t_r}{2\Delta I_s}. \quad (16)$$

where t_r is the current rise time of the MOSFET switches and ΔI_s denotes the current variation amplitude of the switches during turn-on instant. The desired voltage ripple (ΔV_c) is the main criteria for choosing the value of the output capacitors. Hence, the proper value of converter capacitors is obtained as follows:

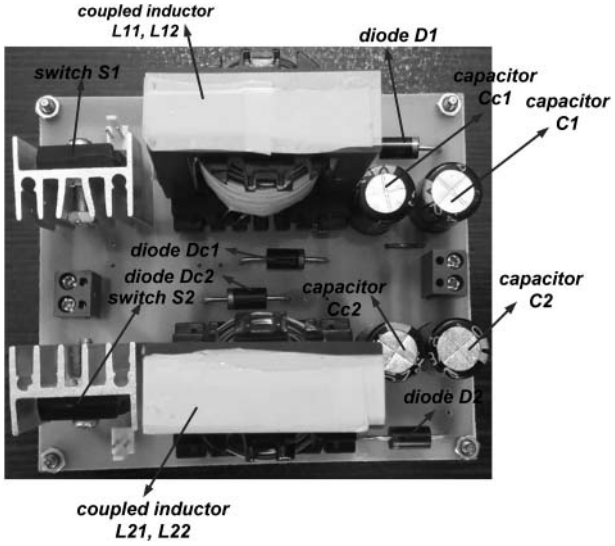


Figure 6. Implemented prototype converter.

$$C_1 = C_2 \geq \frac{V_o(1-D)}{f_s R_L \Delta V_c}. \quad (17)$$

The values of clamp capacitors C_{c1} and C_{c2} are selected such that half of the resonant period formed between C_c and L_{lk} should be greater than the turn-off period of the main switches:

$$C_{c1} = C_{c2} \geq \frac{(1-D)^2}{\pi^2 f_s^2 L_{lk}}. \quad (18)$$

4. Simulation and experimental results

A prototype circuit of the proposed converter is built to evaluate the performance of the proposed topology. The photograph of the implemented circuit is shown in Figure 6. The prototype circuit is designed to convert 25 V input to 400 V output at 200 W nominal power and 100 kHz switching frequency. Specifications of the prototype circuit are given in Table 1.

Moreover, the proposed converter is simulated by ORCAD-PSpice simulator. The simulation circuit is shown in Figure 7. In the simulation circuit, an

Table 1. Specifications of the prototype.

Quantity	Value
Input voltage V_{in}	25 V
Output voltage V_o	400 V
Output power P_o	200 W
Switching frequency f_s	100 kHz
Magnetizing inductors L_{M1}, L_{M2}	100 μH
Leakage inductors L_{lk1}, L_{lk2}	6 μH
Turns ratio (n)	2
Ferrite cores	ER4242
Main switches S_1, S_2	IRFP260
Clamp diodes D_{c1}, D_{c2}	MUR460
Output diodes D_1, D_2	MUR460
Clamp capacitors C_{c1}, C_{c2}	47 μF
Output capacitors C_1, C_2	47 μF

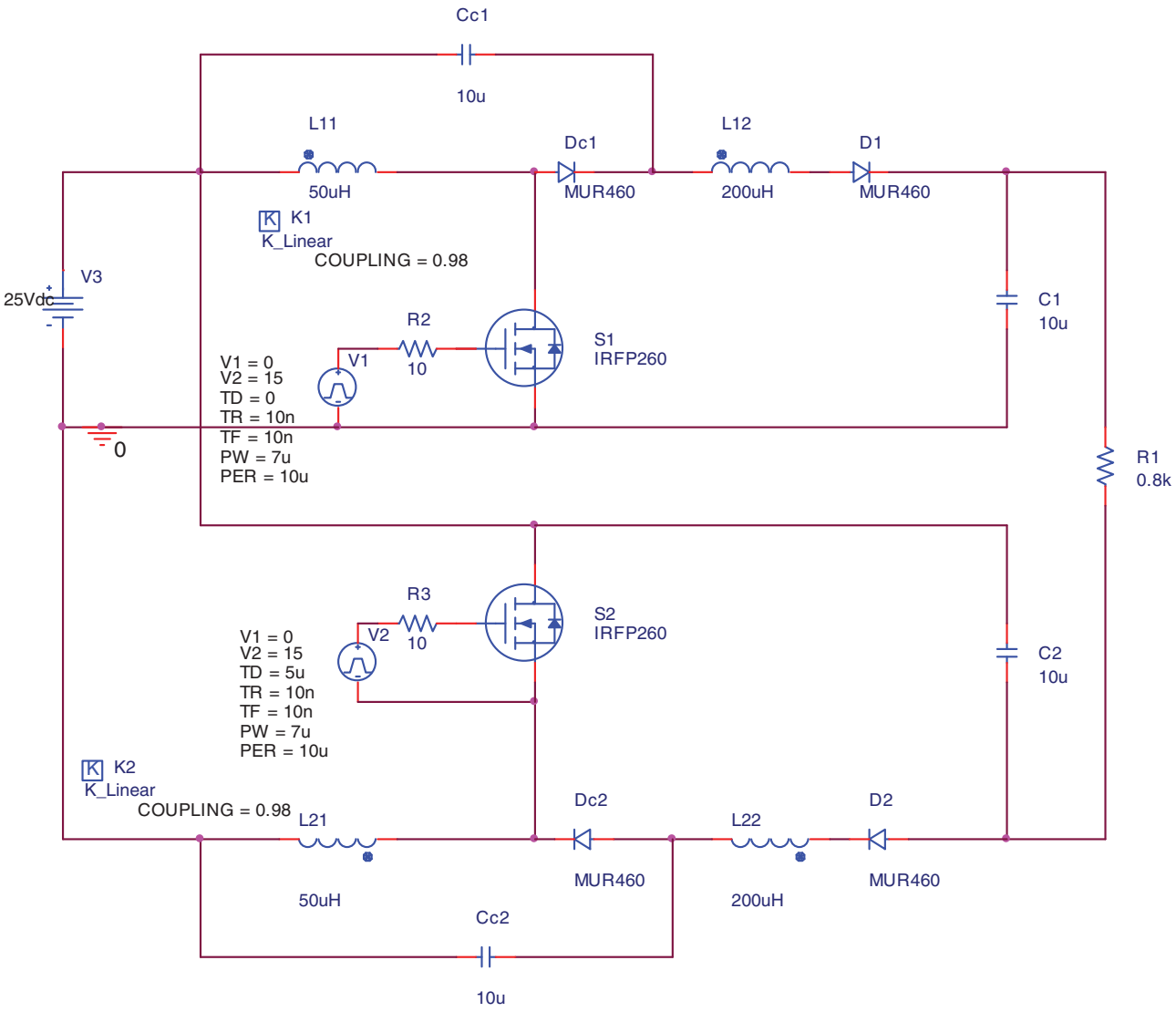


Figure 7. Simulation circuit of the proposed converter.

accurate PSPICE model of all semiconductor devices is used. Also, the coupling coefficient of the coupled inductors is selected 0.98 and the operating duty cycle is 0.7. Figures 8 and 9 show the simulation and experimental waveforms of the proposed converter, respectively. It can be seen that the experimental results show a good agreement with simulation results. The voltage and current waveforms of the main switch S_1 and S_2 are illustrated in Figures 8(a) and 9(a). It can be seen from figures that, for 400 V output voltage, the voltage stress on the MOSFET switches is below 100 V, which is lower than 25% of the output voltage.

In addition, the leakage inductors have accomplished the ZCS turn-on operation of main switches as well.

Figures 8(b) and 9(b) represent the voltage and current waveforms of the clamp diodes D_{c1} and D_{c2}. As can be seen, the voltage stress of clamp diodes is the same as the main switches. Also, the reverse recovery problem of these diodes is completely alleviated. The simulation and experimental waveforms of the output diodes D_1 and D_2 are shown in Figures 8(c) and 9(c).

The voltage stress on the output diodes, which are the most stressful devices in high step-up DC–DC converters, is about 200 V, which is half the output voltage. Also, the reverse recovery problem of the output diodes is completely eliminated.

The efficiency diagram of the proposed converter under different output load condition is plotted in Figure 10. As can be observed, the maximum efficiency of the proposed converter is 94.5% at 140 W output power, and the full-load efficiency is 94.1%.

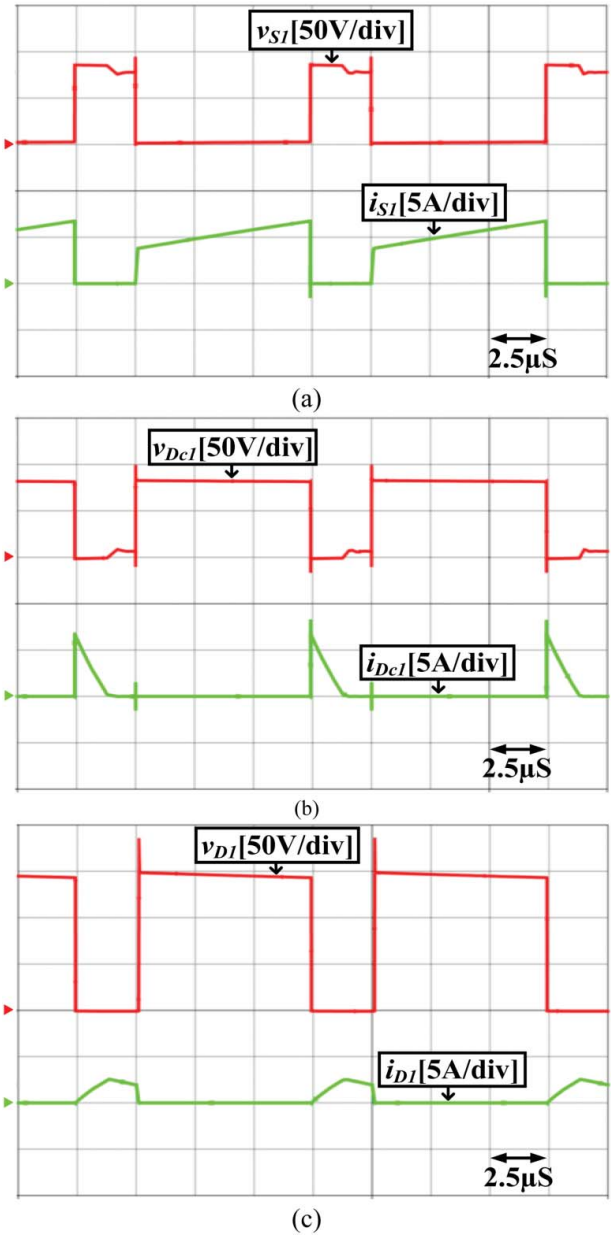


Figure 8. Simulation waveforms of the proposed converter: (a) v_{ds1}, i_{ds1}; (b) v_{Dc1}, i_{Dc1}; (c) v_{D1}, i_{D1}.

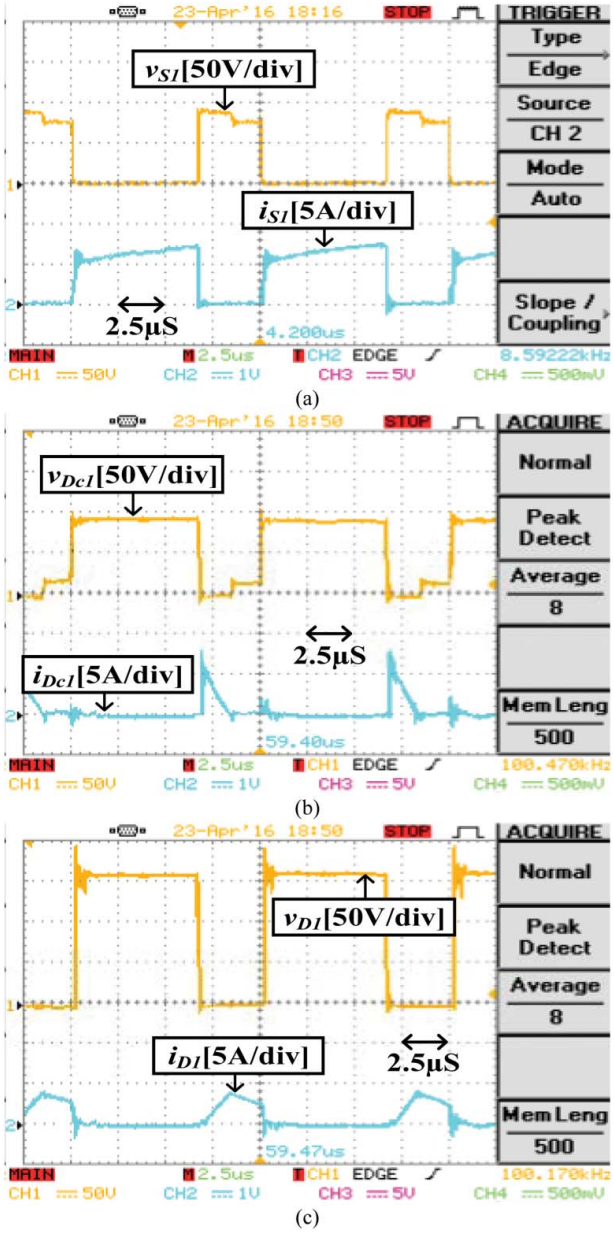


Figure 9. Experimental waveforms of the proposed converter: (a) v_{ds1}, i_{ds1}; (b) v_{Dc1}, i_{Dc1}; (c) v_{D1}, i_{D1}.

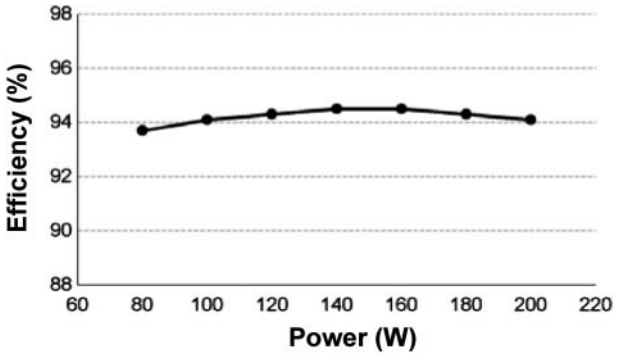


Figure 10. Efficiency diagram of the proposed converter.

5. Conclusion

In this paper, a new interleaved high step-up DC–DC converter based on the floating-output capacitors technique was introduced. The steady-state analysis and derived equations represent that the voltage gain of the proposed converter is much higher than the conventional interleaved boost converter. In this topology, the voltage stress on the main switches and diodes is very low. Consequently, low-voltage, high-performance MOSFET switches and scotty diodes can be used. Also, the output and clamp diodes turn off under ZCS condition.

Moreover, the leakage inductors energy is recycled into the circuit, so the voltage spikes across the main switches are avoided. At last, the proposed converter was simulated and a 200 W prototype circuit was implemented to prove the validity of the steady-state analysis.

Acknowledgments

This work has been extracted from the MSc Thesis entitled "Improvement and implementation of high step-up interleaved dc-dc converter" in Smart Microgrid Research Center, Najafabad Branch, Islamic Azad University, Najafabad, Isfahan, Iran.

Disclosure statement

No potential conflict of interest was reported by the authors.

References

[1] Kim J, Ha K, Krishnan R. Single-controllable-switch-based switched reluctance motor drive for low cost, variable-speed applications. IEEE Trans Power Electron. 2012;27(1):379–387.
[2] Faiz J, Shahgholian G, Ehsan M. Stability analysis and simulation of a single-phase voltage source UPS inverter with two-stage cascade output filter. Eur Trans Electr Power. 2008;18(1):29–49.
[3] Abusara MA, Guerrero JM, Sharkh SM. Line-interactive ups for microgrids. IEEE Trans Ind Electron. 2014;61(3):1292–1300.
[4] Shahgholian G, Faiz J, Sedri N, et al. Design and experimental analysis of a high speed two-phase induction motor drive for weaver machines applications. Int Rev Electr Eng. 2010;5(2):454–461.
[5] Yilmaz M, Krein PT. Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. IEEE Trans Power Electron. 2013;28(5):2151–2169.
[6] Shahgholian G, Shafaghi P. State space modeling and eigenvalue analysis of the permanent magnet DC motor drive system. In: Proceeding of the IEEE/ICECT; Kuala Lumpur, May 2010. p. 63–67.
[7] Ortega M, Jurado F, Valverde M. Novel topology for dc/dc unidirectional converter for fuel cell. IET Power Electron. 2014;7(3):681–691.
[8] Poorali B, Torkan A, Adib E. High step-up z-source dc-dc converter with coupled inductors and switched capacitor cell. IET Power Electron. 2015;8(8):1394–1402.
[9] Li W, He X. Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications. IEEE Trans Ind Electron. 2011;58(4):1239–1250.
[10] Khajeh-Shalaly B, Shahgholian G. A multi-slope sliding-mode control approach for single-phase inverters under different loads. Electronics. 2016;5(4):1–19.
[11] Chen Z, Liu S, Shi L. A soft switching full bridge converter with reduced parasitic oscillation in a wide load range. IEEE Trans Power Electron. 2014;29(2):801–811.
[12] Shahsavary-Babokany A, Jabbaril M, Shahgholian G, et al. A review of bidirectional dual active bridge converter. In: Proceeding of the IEEE/ECTICON; Phetchaburi. 2012. p. 1–4.
[13] Hu X, Gong C. A high voltage gain dc–dc converter integrating coupled-inductor and diode–capacitor techniques. IEEE Trans Power Electron. 2014;29(2):789–800.
[14] Ceraolo M, Poli D. Fundamentals of electric power engineering: from electromagnetics to power systems. Hoboken, NJ: John Wiley & Sons; 2014.
[15] Karady GG, Holbert KE. Electrical energy conversion and transport: an interactive computer-based approach. Vol. 64. Hoboken, NJ: John Wiley & Sons; 2013.
[16] Yazici İ. Robust voltage-mode controller for dc-dc boost converter. IET Power Electron. 2015;8(3):342–349.
[17] Ruan X, Li B, Chen Q, et al. Fundamental considerations of three-level dc–dc converters: topologies, analyses, and control. IEEE Trans Circuits Syst. I. 2008;55(11):3733–3743.
[18] Lu S, Mu M, Jiao Y, et al. Coupled inductors in interleaved multiphase three-level dc-dc converter for high-power applications. IEEE Trans Power Electron. 2016;31(1):120–134.
[19] Wai R-J, Lin C-Y, Lin C-Y, et al. High-efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage. IEEE Trans Ind Electron. 2008;55(10):3702–3714.
[20] Erickson RW, Maksimovic D. Fundamentals of power electronics. Berlin: Springer Science & Business Media; 2007.
[21] Sabzali AJ, Ismail EH, Behbehani HM. High voltage step-up integrated double boost–sepic dc-dc converter for fuel-cell and photovoltaic applications. Renew Ener. 2015;82;44–53.
[22] Ghasemi A, Eilaghi SF, Adib E. A new non-isolated high step-up sepic converter for photovoltaic applications. In: Proceeding of the IEEE/PEDSTC; Tehran. 2012. p. 1–4.
[23] Chan CY. Investigation of voltage-mode controller for cascade boost converter. IET Power Electron. 2014;7(8):2060–2068.
[24] Ye. Y-m, Cheng KWE. Quadratic boost converter with low buffer capacitor stress. IET Power Electron. 2014;7(5):1162–1170.
[25] Liu H, Li F, Ai J. A novel high step-up dual switches converter with coupled inductor and voltage multiplier cell for a renewable energy system. IEEE Trans Power Electron. 2016;31(7):4974–4983.
[26] Hwu K-I, Jiang W-Z, Yang L-C. High-step-up single-switch dc-dc converter with low voltage spike. IET Power Electron. 2015;8(12):2504–2510.
[27] Khalilzadeh M, Abbaszadeh K. Non-isolated high step-up dc-dc converter based on coupled inductor with reduced voltage stress. IET Power Electron. 2015;8(11):2184–2194.
[28] Molavi N, Adib E, Farzanehfard H. Soft-switched non-isolated high step-up dc-dc converter with reduced voltage stress. IET Power Electron. 2016;9(8):1711–1718.
[29] Zhao Q, Lee FC. High-efficiency, high step-up dc-dc converters. IEEE Trans Power Electron. 2003;18(1):65–73.
[30] Li W, Zhao Y, Wu J, He X. Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells. IEEE Trans Power Electron. 2012;27(1):133–143.
[31] Tseng K-C, Huang C-C. High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system. IEEE Trans Ind Electron. 2014;61(3):1311–1319.
[32] e Silva RNAL, Tofoli FL, Praca PP, et al. Soft switching high-voltage gain dc–dc interleaved boost converter. IET Power Electron. 2014;8(1):120–129.
[33] Sizkoohi HM, Milimonfared J, Taheri M, et al. High step-up soft-switched dual-boost coupled-inductor-based converter integrating multipurpose coupled inductors with capacitor-diode stages. IET Power Electron. 2015;8(9):1786–1797.

[34] Nouri T, Hosseini SH, Babaei E, et al. Interleaved high step-up dc–dc converter based on three-winding high-frequency coupled inductor and voltage multiplier cell. IET Power Electron. 2015;8(2):175–189.
[35] Tseng K-C, Huang C-C, Shih W-Y. A high step-up converter with a voltage multiplier module for a photovoltaic system. IEEE Trans Power Electron. 2013;28 (6):3047–3057.
[36] Hu X, Dai G, Wang L, et al. A three-state switching boost converter mixed with magnetic coupling and voltage multiplier techniques for high gain conversion. IEEE Trans Power Electron. 2016;31(4):2991–3001.
[37] Hu X, Gong C. A high gain input-parallel output-series dc/dc converter with dual coupled inductors. IEEE Trans Power Electron. 2015;30(3):1306–1317.
[38] Pan C-T, Chuang C-F, Chu C-C. A novel transformer-less adaptable voltage quadrupler dc converter with low switch voltage stress. IEEE Trans Power Electron. 2014;29(9):4787–4796.
[39] Müller L, Kimball JW. High gain dc-dc converter based on the Cockcroft–Walton multiplier. IEEE Trans Power Electron. 2016;31(9):6405–6415.
[40] Choi S, Agelidis V, Yang J, et al. Analysis, design and experimental results of a floating-output interleaved-input boost-derived dc-dc high-gain transformer-less converter. IET Power Electron. 2011;4(1):168–180.
[41] Kianpour A, Jabbari M, Shahgholian G, High step-up floating-output interleaved-input coupled-inductor-based boost converter. Proceeding of the IEEE/ICEE; Shiraz; May. 2016. p. 1088–1093.
[42] Chao K-H, Yang M-S. High step-up interleaved converter with soft-switching using a single auxiliary switch for a fuel cell system. IET Power Electron., 2014;7(11):2704–2716.
[43] Zhang L, Xu D, Shen G, et al. A high step-up dc to dc converter under alternating phase shift control for fuel cell power system. IEEE Trans Power Electron. 2015;30 (3):1694–1703.
[44] Li W, He X. Zero-voltage transition interleaved high step-up converter with built-in transformer. IET Power Electron. 2011;4(5):523–531.
[45] Sathyan S, Suryawanshi H, Ballal MS. Soft-switching dc–dc converter for distributed energy sources with high step-up voltage capability. IEEE Trans. Ind. Electron. 2015;62(11):7039–7050.