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Automatika

Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: 0005-1144 (Print) 1848-3380 (Online) Journal homepage: http://www.tandfonline.com/loi/taut20

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To cite this article: Naeem Maroof, Muhammad Sohail & Hyunchul Shin (2017) A fast and energy-efficient two-stage level shifter using the controlled Wilson current mirror, Automatika, 58:4, 473-478, DOI: 10.1080/00051144.2018.1456099

To link to this article: https://doi.org/10.1080/00051144.2018.1456099

Published online: 05 Jun 2018.

AUTOMATIKA, 2017
VOL. 58, NO. 4, 473–478
https://doi.org/10.1080/00051144.2018.1456099

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A fast and energy-efficient two-stage level shifter using the controlled Wilson current mirror

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ABSTRACT

Multiple voltage domains are commonplace in modern SoCs and level shifter (LS) circuits allow different voltage domains to be interfaced with each other. As the reduced supply voltages are extensively used in digital blocks for low-power operation, the conversion of sub-threshold voltage levels to full VDD signal becomes a particular problem. In this paper we present a new LS structure for the fast and energy-efficient conversion of extremely low voltage levels. The proposed LS is a two-stage structure consisting of a controlled Wilson current mirror and eliminates the negative feedback mechanism. Inverted output of the second stage controls the current through the first stage. If the input signal is logical high (VDDL) then the circuit will produce high output (VDDH) and the first stage is prepared to conduct the current for logical 0 input (0V). This improves the slew rate problem and enables fast and energy-efficient operation. Considering process corners at a 90-nm technology node, the proposed design reliably converts 150-mV input signal into 1 V output signal. Post-layout results show that the proposed LS exhibits a propagation delay of 16 ns, a total energy per transition of only 79 fJ, and a static power dissipation of 16.6 nW for a 200 mV input signal at 1-MHz, while loading 100 fF of capacitive load.

ARTICLE HISTORY
Received 15 December 2015
Accepted 14 November 2016

KEYWORDS
Level shifter; sub-threshold; energy-efficient; low-power; feedback control

1. Introduction

Modern system-on-chips (SoCs) are quite complex and require sophisticated power management units (PMU) for the delivery of different voltages to multiple domains. Also, many digital blocks are operated in the sub-threshold regime to achieve energy efficiency for battery constraint devices [1,2]. Furthermore, many blocks exploit the use of dynamic voltage and frequency scaling (DVFS) to balance the load/utilization and the power consumption [3,4]. Level shifter (LS) circuits are essential parts of such an SoC, interfacing different voltage domains. These circuit allow the low voltage domain (V_{DDL}) signal to be interpreted correctly into the higher voltage domain (V_{DDH}) and vice versa. Even if the whole core of a chip operates at sub-threshold voltage levels, a secondary above-threshold supply voltage will still be required for the digital I/O pad cells.

The conventional LS circuits do not fulfill design requirements at or below 100-nm technologies without inuring large area and power penalties [5]. Therefore, a reliable, fast and energy-efficient circuit design for signal level conversion is essential for robust low power design. Figure 1 shows an illustration of a low power SRAM array operating at the subthreshold voltage level and LS circuits converting signals from high to low and low to high voltage domains. The $M \times N$ bitcell array and the bitline read sensors (a.k.a sense amplifiers) all operate at very low voltage supply. A high performance processing core can operate at different voltage levels depending upon the workload demand, and thus the output of memory block will be converted to high levels. High to low voltage conversion can be easily done through inverters. However, conversion of subthreshold to above-threshold or full-V_{DD} level conversion is challenging in the sub-100nm regime.

An LS have complementary input signals, V_{IN} and V_{INB}, of the low voltage domain, and an output signal V_Z of the high voltage domain. A conventional LS (CLS) is a cross-coupled half-latch and is shown in Figure 2(a). In the case of $V_{IN} = V_{DDL}$, the M1 transistor pulls down the node V_A, and thus the node V_Z is charged to V_{DDH} by M4. The transistor M2 remains OFF as its V_{GS} is V_{INB} which is 0V in this case. However, there exists a large amount of contention between pull-up and pull-down network. When V_{INB} is high (V_{DDL}), M2 tries to pull down node V_Z which, however, is being charged by the transistor M4. This results in a higher dynamic power dissipation and an increased delay. It has been estimated that the CLS requires 2400× wider pull-up transistors than the pull-down transistors in a 90-nm technology to make a successful transition for a 200 mV of input [6]. This, of course, underpins the infeasibility of the conventional LS structure.

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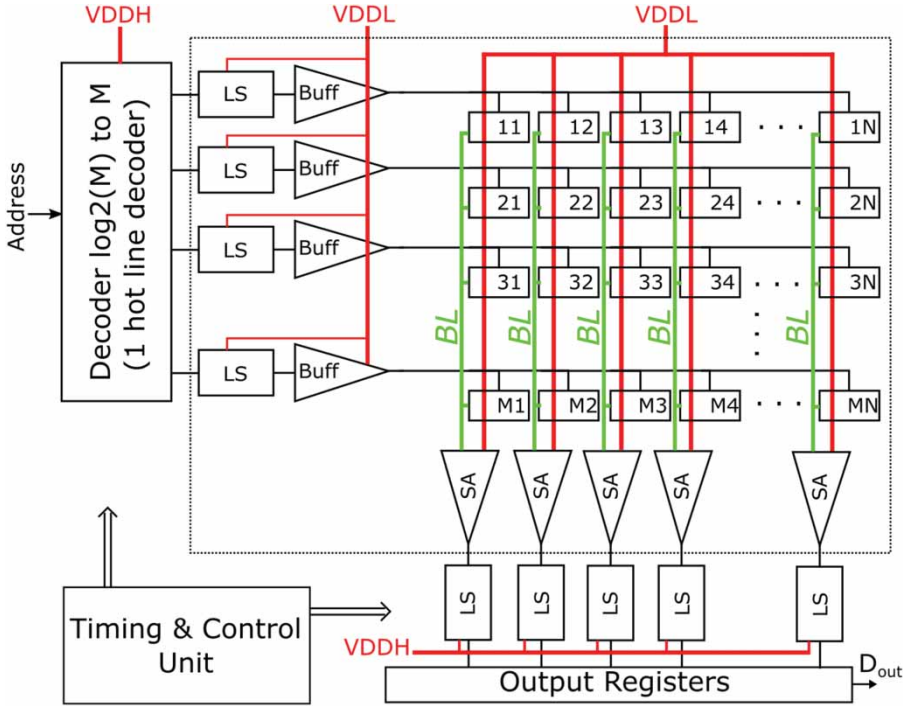

Figure 1. Illustration of low-power SRAM using level shifters as interface circuits.

Several works have been reported to overcome the limitations of CLS. A cascade of four stages of CLS is used in [2] to convert a 200 mV signal into a 1.2 V signal. Nevertheless, such an implementation requires voltage regulators which incur area and power penalty. Design presented in [7] used only two CLS stages connecting the first to higher voltage through a diode-connected NMOS, and thus avoids intermediate supply voltages. However, this design does not achieve high-speed performance. Use of multi-threshold technology has been proposed to strengthen the pull-up network and weaken the pull-down network [8,9]. As multi-V_{TH} technology is not mainstream, its use is quite complex and expensive. Chen et al. reduced the strength of the pull up network by limiting its currents by using a current-mirror [10]. This design achieves a wide operation range but dissipates a large amount of quiescent current. Sven et al. avoided this large static current by using a Wilson current-mirror based level shifter (WLS) [6]. Their design offers better energy efficiency as the current-path is cut off when the desired output level is achieved. However, the negative feedback mechanism slows down the charging of the output node, and hence affects the speed of operation and dynamic power dissipation. Also, the output node of the current-mirror floats for a high level of V_{IN}, which causes a significant detrimental effect on the output buffer. Modified Wilson current-mirror based designs have also been proposed which only marginally improve the delay and the power dissipation [11,12]. Osaki et al. used the current generators (CGs) which turn ON only when the input and output logic level differs [13]. Contention problem of [13] is discussed in [14], where they proposed a new design based on CGs and solved the problem through output feedback. Their design uses 14 transistors, and proper sizing is required to charge the internal nodes and reduce the power dissipations of the inverter (output of which is fed back to the CGs).

In this paper, we present our new level shifter design which is fast and very energy efficient. The proposed architecture is a two-stage design using a "controlled" Wilson current mirror. Rather than the direct output of the Wilson current mirror, the output of the second stage is inverted and used as a control signal for the Wilson current mirror. Hence, we eliminate the decreasing slew rate problem and achieve a very fast and energy-efficient operation. Our proposed level shifter is capable of converting a sub-threshold input signal, as low as 150 mV, into a 1 V signal. Extensive post-layout simulations, comparing and evaluating with a state-of-the-art reference level shifter (WLS) from [6] have been carried out to demonstrate the effectiveness of the proposed design. The rest of paper is organized as follows. Section 2 describes the operation of the reference and the proposed design. Thorough post-layout results, transient waveforms and comparative discussion are provided in Section 3. Effect of process variations and PVT corners is presented in 4, and finally Section 5 concludes the paper.

2. Proposed design

The reference and the proposed level shifter structures are shown in Figure 2(b) and 2(c), respectively. Reference LS is based on the Wilson current mirror and consists of five mosfet devices (MW1-MW5). When the input is V_{DDL}, and hence $V_{INB} = 0$ V, MW1 is ON and the current can pass through the left branch (assuming

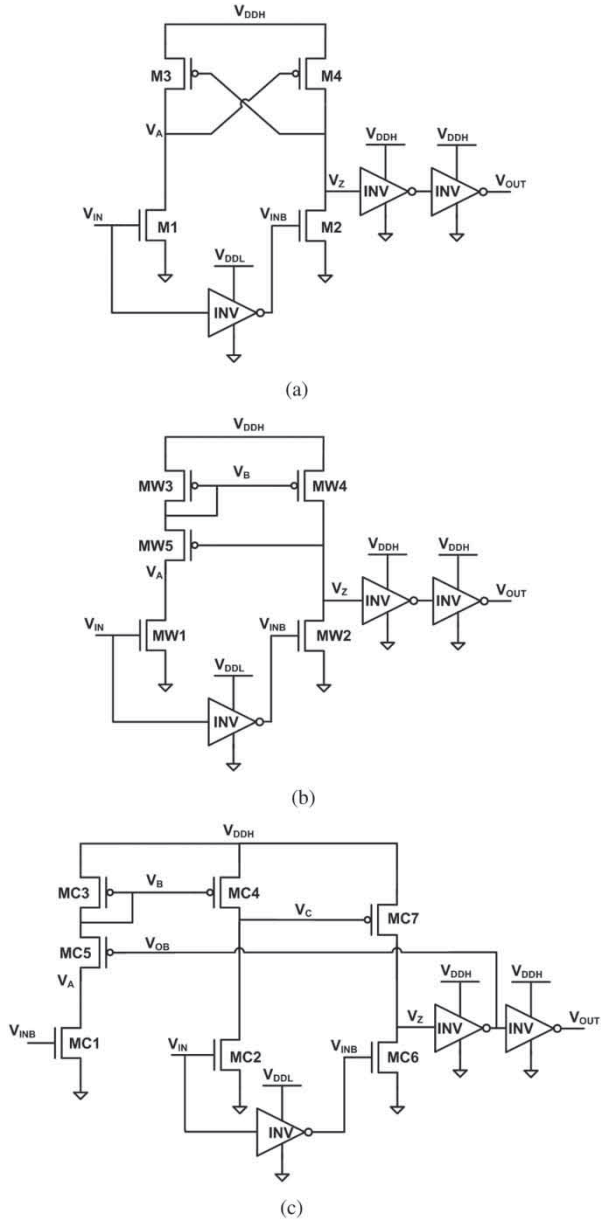

Figure 2. Level shifter circuit schematics: (a) conventional cross-coupled half latch; (b) Wilson current mirror (reference) and (c) the two-stage controlled Wilson current mirror (proposed) based level shifter designs. (a) Conventional design (CLS). (b) Reference design. (c) Proposed design (TSCWLS)

that previous output was 0 V for $V_{IN} = 0$ V). MW4 copies the current via current-mirror operation. This copied current in the right branch charges output node, as MW2 is OFF. However, as the node V_Z reaches a higher value, MW5 starts turning OFF as its gate voltage approaches its source voltage. This decrease in the current through MW5, creating a negative feedback, decreases the slew rate of the output node. When the input is low, assuming that the previous output was high, MW1 and MW5 are off and no current can flow through the left branch. MW2 easily discharges the output node, and hence effectively turns ON the MW5 transistor, which, for a short period of time, passes current to charge node V_A. After that, only leakage current flows through the left branch, and output node stays near 0 V.

Our proposed level shifter is a two-stage controlled Wilson current mirror level shifter (TSCWLS) and consists of seven mosfet devices (MC1-MC7). Output of the second stage is inverted and used to control the MC5 transistor. This eliminates the negative feedback mechanism. Transistor MC5 is turned OFF to avoid any quiescent current dissipation for logical low input, and is turned ON to conduct the current for the next input transition for logical high input level once the full level at the output of main stage is achieved. This solves the slew rate problem and achieves a very fast and energy-efficient operation. Transistors MC1 and MC6 are driven by V_{INB}. When $V_{IN} = V_{DDL}$, node V_C is discharged through MC2, because the current-mirror MC3-MC4 is OFF (as the MC1 transistor has input V_{INB}). Transistor MC6 is OFF (also driven by V_{INB}) and the output node V_Z is charged to V_{DDH} by MC7. Inverted output, V_{OB}, becomes 0 V, and turns ON the MC5 transistor for next transition. When $V_{INB} = V_{DDL}$, MC1 is ON and the current can flow through MC5 (as V_{OB} is 0 V initially). This turns ON the current mirror, and the current copied through MC4 charges the node V_C. This effectively turns OFF the MC7 transistor, and the node V_A is discharged through MC6 (which is also driven by V_{INB}). Thus, the output becomes 0 V and the inverted output becomes V_{DDH}, and the transistor MC5 turns OFF. No further current can pass, and thus the current mirror turns OFF. This controlled current mirror mechanism provides the fast and energy-efficient operation.

3. Post-layout results

Both of the reference and the proposed LS circuit designs are laid-out in a 90-nm technology and the finished layouts are shown in Figure 3. Each layout includes the main conversion stage and an output buffer. Transistors are realized using minimum-width fingers. Metal-1 layer is used for interconnects and power-rails. Metal-2 layer is used for input and output signals. Post-layout simulations are carried out in HSPICE, and the output of buffer is loaded with a 100 fF of capacitive load for both LSs.

The value of V_{DDH} is kept at 1 V and V_{DDL} is varied from sub-threshold levels. Input frequency is kept at 1 MHz with a duty cycle of 0.5 and 10 ns of rise and fall time. We evaluate both LSs on the basis of the propagation delay (τ_p) which is the average value of rising and falling delay, total energy-per-transition (E_{tr}) which is the average energy dissipation for high-to-low and low-to-high transitions of the output signal, energy-delay-product (EDP) which is the product of energy dissipation and the delay at specific operating point and is a useful metric, and the static power dissipation (Ps) which is average leakage power for low and high input

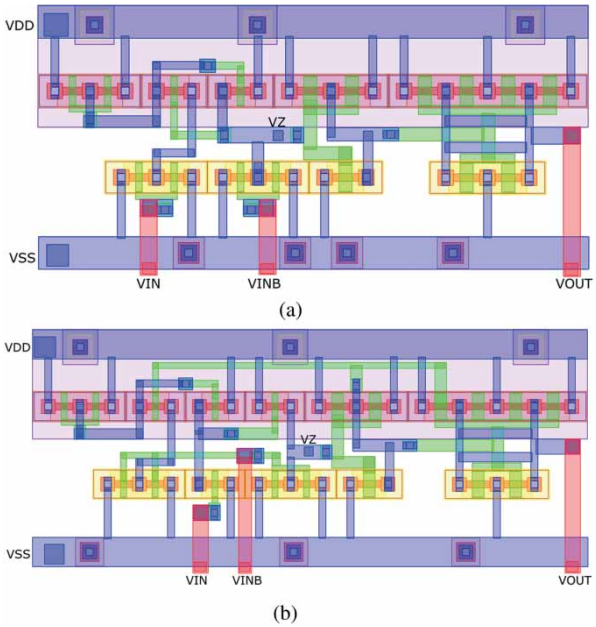

Figure 3. Layout of level shifter structures including the output buffer. (a) WLS and (b) TSCWLS.

levels. For the correctness of operation, the output duty cycle needs to be between 0.45 and 0.55, otherwise LS is considered to have failed for that specific input level.

Both of the LSs operate well below sub-threshold levels. The minimum input level for both LSs is 150 mV. In Figure 4, we show the output node voltage of the main conversion stage of both the LSs for a 200 mV of input. Output of the proposed LS achieves a higher value, and its slew rate is not affected as the output node is charged, while in the case of WLS, output slew rate decreases due to the negative feedback. As the output node of WLS rises, MW5 starts turning off, resulting in less current being supplied to the output node. A higher output value of TSCWLS and improved output slew provides the dynamic energy efficiency and the performance benefit as now the current through the circuit does not need to pass for a longer time and there is no contention as well. As shown by output voltage waveforms, the proposed LS achieves better performance for the rising and falling transitions. However, the proposed LS dissipates a higher amount of static power than the reference

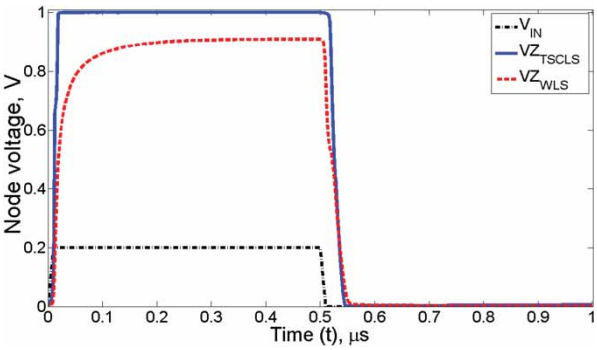

Figure 4. Output node voltage of the main stage of both (reference and proposed) designs.

design due to the fact that it has three branches. When $V_{IN} = 0$ V, node V_C is charged and the current mirror turns off when the output achieves the corresponding level. Static current through MC2 decreases node V_C, which lets MC7 pass a higher amount of current as the transistor MC6 is ON. Static power dissipation of TSCWLS and WLS is 16.6 and 10.2 nW respectively. Nevertheless, static power dissipation and speed can be traded by increasing the transistor channel length.

For different values of V_{DDL}, the propagation delay and the total energy per transition of both the LSs are shown on logarithmic scale in Figure 5(a) and 5(b), respectively. At the design target of 200 mV and 1 MHz input, TSCWLS has a propagation delay of 16 ns and an E_{tr} of 79 fJ, while WLS has a propagation delay of 18 ns and an E_{tr} of 97.1 fJ. The normalized EDP of the proposed LS is only 72.3% than that of the reference design for 200 mV of the input signal. TSCWLS offers 24% lower propagation delay, 10% lower E_{tr}, compared with WLS on average for $V_{DDL} = 0$ V to 600 mV. Average normalized EDP of TSCWLS (with respect to WLS) is only 69%.

Table 1 shows the results of the proposed design and comparison with other previously proposed designs from [6–10,13]. From the comparison, it can be seen that the proposed design exhibits best performance and

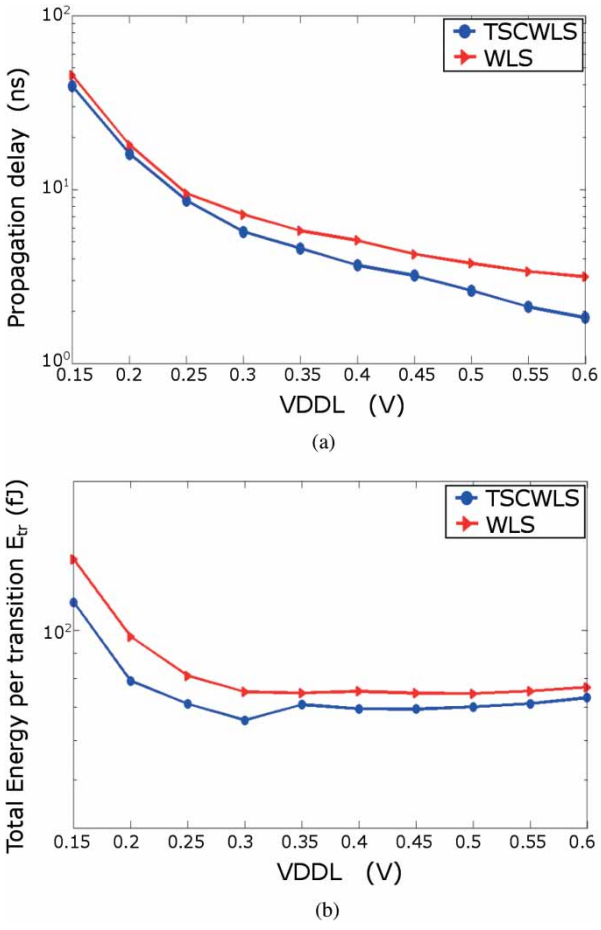

Figure 5. Evaluation of both LSs at different values of V_{DDL} (a) Propagation delay (ns) in log scale and (b) total energy per transition (fJ) in log scale.

Table 1. Energy, delay and static power comparison of different designs.

Design	Tech	V_{DDH}(V)	V_{DDLmin}(V)	Delay (ns)	E_{tr}(pJ)	P_s (nW)	Results
[10]	0.13 µm	1.2	0.1	50@0.2 V	25@0.2 V-50 kHz	8@0.2 V	Measured
[7]	0.13 µm	1.2	0.18	57.9@0.2 V	NA	NA	Measured
[13]	0.35 µm	3	0.23	10^4@0.4 V	5.8@0.4 V-10 kHz	0.23@0.4 V	Measured
[8]	90 nm	1	0.18	21.8@0.2 V	0.074@0.2 V-1 MHz	6.4@0.2 V	Post-layout
[9]	90 nm	1	0.1	16.6@0.2 V	0.077@0.2 V-1 MHz	8.7@0.2 V	Post-layout
[6]	90 nm	1	0.1	18.4@0.2 V	0.094@0.2 V-1 MHz	6.6@0.2 V	Pre-layout
[6][a]	90 nm	1	0.1	25.2@0.2 V	0.103@0.2 V-1 MHz	20.4@0.2 V	Post-layout
[6][b]	90 nm	1	0.15	18@0.2 V	0.097@0.2 V-1 MHz	10.2@0.2 V	Post-layout
This work	90 nm	1	0.15	16@0.2 V	0.079@0.2 V-1 MHz	16.6@0.2 V	Post-layout

[a] replicated in [9].
[b] replicated in this work.

competitive energy-efficient operation, though it has relatively a higher static power as the proposed design consists of two stages. For a 0.2 V input signal, the normalized energy-delay-product (EDP) of TSCWLS, WLS, LS from [8] and LS from [9] is 1, 1.38, 1.01 and 1.27, respectively. Only the LS from [9] comes near TSCWLS in terms of EDP with a penalty of 1%. The main conversion stage of [9] consists of 10 transistors, and it uses multi-threshold voltage technology. As the region of interest is the sub-threshold regime, strengthening the pull-down network and weakening the pull-up network can further improve the results of the proposed LS by using the multi-threshold voltage process.

4. Variability analysis

For integrated circuit design, no two devices are exactly similar after fabrication, though they might be designed the same. This is because of process variations, such that, for example, some devices might have a thicker oxide layer than others. There are two types of variations for ICs, one is global or die-to-die variations, and other is local or with-in-die variations. Global variations are typically handled using different process corners. Local variations need to be modelled according to the technology parameters. Most important sources of local variations, which impact the device threshold voltages, are random-dopant-fluctuations. These variations contribute upto 60% of total V_{TH} mismatches in sub-micron processes. These variations follow Gaussian distributions, and hence are modelled accordingly using Pelgrom's equation, which is inversely related to the square root of gate area of a transistor, and the constant of proportionality is defined by technology parameters. These calculations are scaled accordingly to account for extra variations due to other sources. 10,000-point Monte Carlo (MC) simulations were carried out at 200 mV input, and the histogram of propagation delay is shown in Figure 6 for both level shifters. The normalized variance of TSCWLS is 0.44 and of WLS is 0.47, which shows that the proposed design is more robust against process variations.

For the global process, voltage, and temperature (PVT) variations, corner analyses were carried out

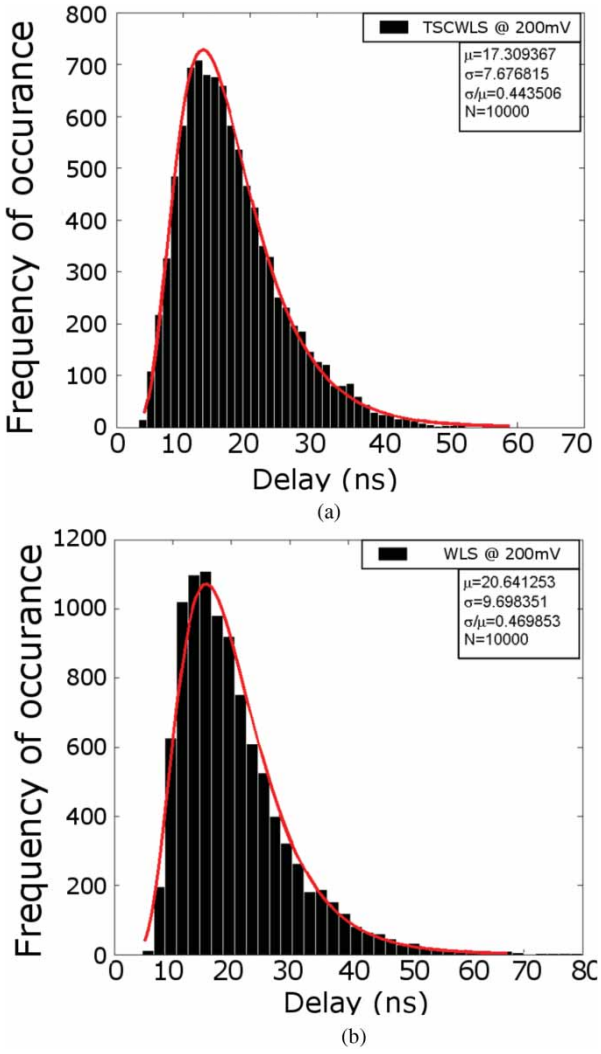

Figure 6. Propagation delay distribution using HSPICE Monte Carlo simulations at $V_{DDL} = 200$ mV.

for the best, worst and the typical PVT corners. The nominal case includes typical-NMOS, typical-PMOS, a 200 mV of low voltage supply, a 1 V of high voltage supply, and a temperature of 25°C. The second PVT corner was determined considering the worst-case operating conditions occurring for sub-threshold input signal levels. In such a condition, weakly driven NMOS transistors have to overpower the corresponding PMOS transistors. A decrease in lower supply and an increase in higher supply further worsen this situation, and finally low temperature is chosen as

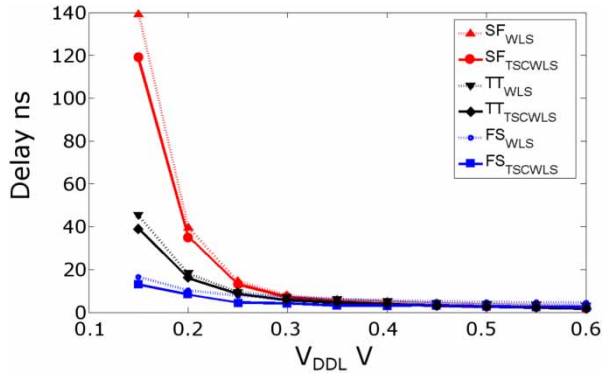

Figure 7. Propagation delay for different PVT corners.

it results in smaller currents in the sub-threshold regime. Thus, slow-NMOS, fast-PMOS, $-10\%V_{DDL}$, $+10\%V_{DDH}$, and a temperature of $-25^{\circ}C$ constitute a worst PVT corner. As opposite case, fast-NMOS, slow-PMOS, $+10\%V_{DDL}$, $-10\%V_{DDH}$, and a temperature of $125^{\circ}C$ is considered the best PVT corner. In Figure 7, propagation delay as a function of V_{DDL} is shown for both level shifters against all PVT corners discussed. For the typical corner at 150 mV, the propagation delay is 45.22 ns for WLS and 39.12 ns for TSCWLS. Worst case delay of TSCWLS and WLS at 200 mV is about $\sim 4.3\times$ and $\sim 3.9\times$ than their best case delay. Both level shifters operate correctly at the design target for all PVT corners. However, for 150 mV, although the correct output is achieved by both LS for all PVT corners, the output duty cycle of both LS shows more than 10% distortion for the worst case.

5. Conclusion

Level shifter circuits are necessary parts of modern system-on-chips. Conversion of a sub-threshold voltage level into full V_{DD} signal presents challenges in deep-sub-micron technologies for efficient operation. In this paper, we have presented a two-stage level shifter with the "controlled" Wilson current mirror. Output of the first stage is fed to the second stage. Inverted output of the second stage is fed back to control the Wilson current mirror of the first stage, and thus eliminating the negative impact. This mechanism provides fast and efficient charging and discharging of the output node. Post-layout evaluation results show that the proposed LS is fast, energy efficient and robust, and can convert the sub-threshold signal as low as 150 mV into full V_{DD}. Compared with a state-of-the-art LS, the proposed design offers considerable improvement in the EDP. At design target (200 mV, 1 MHz frequency), the design offers 16 ns of delay with only 79 fJ of total energy-per-transition.

Acknowledgments

VLSI CAD tools for this work were provided by IC Design Education Center, South Korea.

Disclosure statement

No potential conflict of interest was reported by the authors.

Funding

Authors are thankful to Samsung, South Korea for supporting the research work at Digital Systems Lab. The first two authors would like to thank Higher Education Commission of Pakistan (hec.gov.pk) for scholarship support.

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