A ΔΣ Modulator Automated Synthesis Tool for Wireless Standards

Houda DAOUD, Samir Ben SALEM, Sawssan LAHIANI, Mourad LOULOU

Abstract: This paper presents the prediction of single-bit discrete-time feed-forward Delta-Sigma (DT FF ΔΣ) modulators performance for wireless standards with the use of two methods. The presented work uses the MAPLE tool and a new design automation tool to estimate the performance of different DT FF ΔΣ modulators topologies intended for low power consumption systems. The proposed tool is based on synthesis algorithm, which takes advantage of analytical models of both FF ΔΣ modulator and operational transconductance amplifier (OTA) performance. By defining the required specifications, the proposed synthesis tool is capable to find the predictive performance of both the modulator topology and the required OTA building block for future process. A Graphical User Interface is programmed to easily present some designed circuits examples.

Keywords: DT FF ΔΣ modulators performance prediction; ΔΣ modulator and OTA performance modelling; design automation; programmed Graphical User Interface; wireless standards

1 INTRODUCTION

Among the diversity of Delta-Sigma (ΔΣ) modulators architectures, feed-forward Delta-Sigma (FF ΔΣ) modulators have become the most used architectures to meet the requirements of wireless communication systems [1]. In fact, it has recently become very popular to feedforward the input signal in wideband ΔΣ modulators, so that the integrators only process quantization errors, the advantage being that the actual signal is not distorted by operational amplifier and integrator nonlinearities [2]. In addition, the benefits of these topologies are their abilities to achieve high resolutions with a decrease in power consumption [3]. The trend of designing low power ΔΣ modulators using upcoming CMOS Nano-process has been growing rapidly in recent years [4]. Designers usually require much time to select the best ΔΣ modulator architecture with the appropriate process node, to determine its performance and to acquire the desired operational transconductance amplifier (OTA) circuits. The time spent for designing is very long and needs a lot of experience. Thus, new tools for ΔΣ modulators are required for unskilled designers.

In front of the increasing complexity of ΔΣ modulators, several studies proposed many tools [5, 6]. Medeiro proposed a high-level specifications tool. His tool has used an equation-based approach at the modulator level and a simulation-based approach at the cell level. It has only supported single-loop ΔΣ modulators and the simulation has taken a lot of time [7]. Tang and Doboli presented a topology-synthesis methodology which gives all possible topologies under various design considerations for single-loop single-bit ΔΣ modulators [8]. However, the ΔΣ modulator topology performance is strongly affected by the non-idealities of building blocks, therefore, the implementation is even more difficult in nanometer CMOS technologies. For this reason, it is recommended to ameliorate or to present other ΔΣ modulators structures with high performances that satisfy the specifications of new standards.

Given the frequent use of submicron CMOS process for low power ΔΣ modulators design, the aim of this work is focused on the prediction of different structures of DT FF ΔΣ modulators performance with process scaling for various mobile telecommunications standards.

In this context, this paper proposes a novel helpful approach for the synthesis of low power FF ΔΣ modulators with Nanometric CMOS process. Some equations models linking the FF ΔΣ modulator performance to the design and the technological parameters are developed. Then, a Graphical User Interface (GUI) is programmed in which the user can get access to additional interfaces for different tasks. The next Section details the procedure of NanoCMOS ΔΣ modulators performance prediction including the modeling of ΔΣ modulator and OTA performance and the use of the MAPLE tool. The following Section presents the design automation approach and the proposed synthesis algorithm. Some design examples are provided afterwards in order to show the operation of the system. Finally, the conclusions drawn from this work and possible future works are presented.
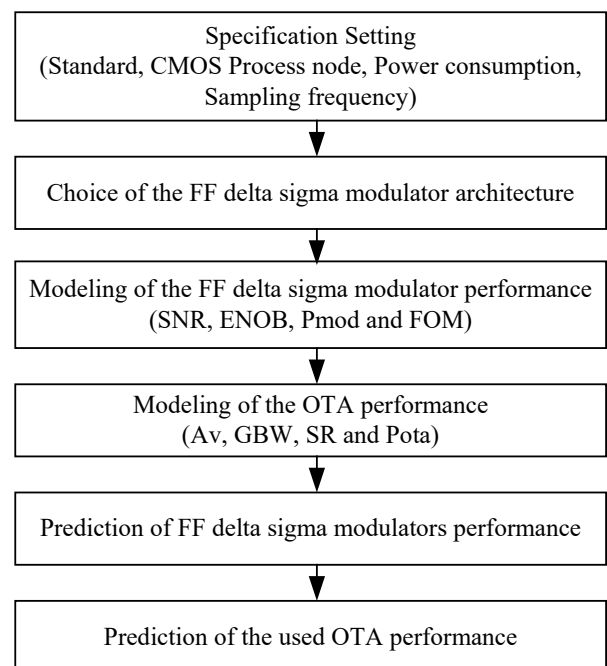
Specification Setting (Standard, CMOS Process node, Power consumption, Sampling frequency)
↓
Choice of the FF delta sigma modulator architecture
↓
Modeling of the FF delta sigma modulator performance (SNR, ENOB, Pmod and FOM)
↓
Modeling of the OTA performance (Av, GBW, SR and Pota)
↓
Prediction of FF delta sigma modulators performance
↓
Prediction of the used OTA performance

Figure 1 Prediction flowchart of FF ΔΣ modulators performance

2 PROCEDURE OF NANOCMOS FF ΔΣ MODULATORS PERFORMANCE PREDICTION

In this Section, a prediction flowchart is introduced to detail the different steps to acquire predictive FF ΔΣ modulators performance. As it can be seen from Fig. 1, firstly, we fix the specifications including the wireless standard, the CMOS process node, the power consumption and the F_S. Secondly, by varying the order of the FF ΔΣ modulator, we opt for its architecture. Taking both design and technological parameters into consideration, some equations models related to FF ΔΣ modulator and OTA performance could be developed. Finally, the performance of FF ΔΣ modulators architectures and the required OTA circuit performance are predicted for future process.

2.1 Modelling of FF Δ Σ Modulator Performance

Currently, designers focus on DT FF ΔΣ modulators design for submicron process to meet the requirements of new wireless communications systems [9]. Our objective consists of predicting the performance of several single-bits DT FF ΔΣ modulators structures namely the signal-to-noise ratio (*SNR*), the resolution (*ENOB*), the power consumption (P_{mod}) and the figure of merit (*FOM*) for wireless standards. To estimate this performance, the selected FF ΔΣ modulator architecture should be modelled accurately. When modelling, we suppose that the errors caused by non idealities affecting the analog building blocks are neglected.

2.1.1 Signal to Noise Ratio (*SNR*)

The SNR is the most used criterion to characterize the modulator performance. In fact, the *SNR* which represents the ratio between the input signal power (P_S) and the quantization noise power (P_Q) is defined by the following equation:

$$SNR = 10 \cdot \log\left(\frac{P_S}{P_Q}\right) = 10 \cdot \log\left(\frac{U_{max}^2}{2P_Q}\right), \tag{1}$$

U_{max} presents the maximum voltage of the signal applied to the modulator input. It is given by Eq. (2):

$$U_{max} = V_{ref} \cdot OL, \tag{2}$$

OL and V_{ref} represent respectively the overload and the reference voltage. The quantization noise power is given by the following relationship [10]:

$$P_Q = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12F_S} |NTF(f)|^2 \, df, \tag{3}$$

where Δ, F_S and *NTF* are respectively the quantization step, the F_S and the noise transfer function. P_Q varies from one modulator architecture to another. If we use a Lth-order ΔΣ modulator architecture where its *NTF* is in the form of $(1 - z^{-1})^L$, Eq. (3) is approximately rewritten as follows:

$$P_Q \approx \frac{\Delta^2}{12}\left(\frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}}\right), \tag{4}$$

where *L* and *OSR* are respectively the order and the over sampling ratio. The quantization step Δ is given by:

$$\Delta = \frac{V_{fs}}{2^B - 1}, \tag{5}$$

where V_{fs} and *B* are the full scale voltage and the quantizer bits number. For a *N*-stage cascaded ΔΣ modulator architecture, the quantization noise power can be approximated to Eq. (6):

$$P_Q \approx d_{2N-3}^2\left(\frac{\Delta_N^2}{12}\right)\left(\frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}}\right), \tag{6}$$

with d_{2N-3} being the digital coefficient of the Nth-stage ΔΣ modulator.

2.1.2 Effective Number of Bits (*ENOB*)

The quantization levels number of a conversion system is defined by the effective number of bits (*ENOB*) or resolution. The resolution is expressed as [11]:

$$ENOB = \frac{SNR(\text{dB}) - 1,76}{6,02}. \tag{7}$$

2.1.3 Power Consumption

Given the increasing number of both the portable equipment and the functional blocks integrated on the same chip, low power consumption of a ΔΣ modulator is an important property. In this work, we aim to design a modulator structure where the power consumption of the used comparator is very low. In [12], Feldman assumes that the power dissipated in a switched capacitor integrator is that which is required to charge and discharge the sampling capacitor C_S. Then, the required power consumption of the modulator can be approximated to Eq. (8):

$$P_{mod} \gg \sum P_{integ} \gg \sum\left(V_{dd}^2 \cdot C_S \cdot F_S\right), \tag{8}$$

V_{dd}, C_S and F_S are respectively the supply voltage, the sampling capacitor and the F_S.

2.1.4 Signal bandwidth (BS)

It is the frequency band on which the ΔΣ modulator may be used. It can be written in the following form [11]:

$$BS = \frac{F_S}{2 \cdot OSR} \tag{9}$$

2.1.5 Figure of Merit (*FOM*)

The FOM compares the performance of various ΔΣ modulators. It is given by the following expression [13]:

$$FOM = \frac{P_{\text{mod}}}{2^{ENOB} \cdot 2BS}, \tag{10}$$

where BS is the signal bandwidth.

2.2 Modelling of OTA Performance

The most important block in the DT FF $\Delta\Sigma$ modulator structure is the OTA circuit which has a great impact on modulators performance. Thus, the designer should use a suitable OTA topology to realize robust $\Delta\Sigma$ modulators. In this work, we focus on finding a relationship between $\Delta\Sigma$ modulator and OTA performance. The main OTA performance which may directly affect the operation of $\Delta\Sigma$ modulator are the DC gain (A_{dc}), the gain-bandwidth product (GBW) and the Slew Rate (SR).

2.2.1 DC Gain Requirement

The settling error at the output of the OTA circuit, resulting from the finite open loop DC gain A_{dc} is approximately given by [14-15]:

$$e_0 = \frac{1}{1 + (\beta_i \cdot A_{\text{dc}})} \approx \frac{1}{\beta_i \cdot A_{\text{dc}}}, \tag{11}$$

where β_i is the feedback factor.

The OTA circuit will be used in a data converter with *ENOB* bits accuracy and it must amplify signals to within half least significant bits (LSB) of the ideal value [14]. Therefore, the required OTA DC gain can be obtained to meet the accuracy requirement of the ADC circuit. It is given by the following expression:

$$A_{\text{dc}} \geq \frac{2^{(ENOB+1)}}{\beta_i}. \tag{12}$$

The minimum required DC open loop gain can be expressed as:

$$A_{\text{dc}} = \frac{2^{(ENOB+1)}}{\beta_i}. \tag{13}$$

2.2.2 Gain-Bandwidth Product Requirement

For a single pole system, where the OTA settling requirement is *ENOB* bits, the output settles to *ENOB* in the sampling time period T_S if [16]:

$$e^{-\frac{T_S}{\tau}} \prec 2^{-ENOB}, \tag{14}$$

where τ and T_S are respectively the settling time constant and the T_S. Eq. (15) describes the settling time constant where C_f is the integration capacitor and β_i is the feedback factor which is detailed in Eq. (16) [17].

$$\tau = \frac{1}{\beta_i \cdot GBW}, \tag{15}$$

$$\beta_i = \frac{C_f}{C_S + C_f}. \tag{16}$$

It leads to the following requirement for the GBW using Eq. (14) and Eq. (15):

$$GBW \geq ENOB\left(\frac{\ln(2)}{\beta_i \cdot T_S}\right). \tag{17}$$

The minimum required OTA GBW is given by Eq. (18):

$$GBW_{\text{min}} = F_S \cdot ENOB\left(\frac{\ln(2)}{\beta_i}\right). \tag{18}$$

2.2.3 Slew Rate Requirement

It is assumed that the OTA integrator is a first order system, the maximum variation of the circuit response is given by the following expression [18]:

$$\frac{d}{dt}(V_0(t))\Big|_{t=0} = g_1\left(\frac{V_{\text{in, max}}}{\tau}\right) \quad \text{where} \quad g_1 = \frac{C_S}{C_f}, \tag{19}$$

g_1 and $V_{\text{in, max}}$ are respectively the integrator gain and the maximum input voltage. Regarding the settling error, in the case of:

$$SR \geq \frac{C_S}{C_f} \cdot \frac{V_{\text{in, max}}}{\tau}, \tag{20}$$

there is no Slew Rate limitation and the integrator output will be linearly settled. From Eq. (20), the minimum required OTA SR is obtained:

$$SR_{\text{min}} = \frac{C_S}{C_f} \cdot \frac{V_{\text{in, max}}}{\tau}. \tag{21}$$

Using Eq. (14), the minimum required Slew Rate is rewritten as:

$$SR_{\text{min}} = F_S \cdot ENOB \cdot \frac{C_S}{C_f} \cdot V_{\text{in, max}} \cdot \ln(2), \tag{22}$$

where $V_{\text{in, max}} = V_{\text{ref}} \cdot OL$. The V_{ref} voltage value is chosen very close to the OTA circuit output swing in order to increase the $\Sigma\Delta$ modulator input swing.

Referring to Eq. (13), Eq. (18) and Eq. (22), it can be noted that the OTA performance depends on the $\Delta\Sigma$ modulator performance (*ENOB*, OL, analog coefficient), the selected F_S and the CMOS process node (V_{dd}). The prediction of the required OTA circuit performance for each provided $\Delta\Sigma$ modulator architecture can be an important key to success.

2.3 Prediction of FF Δ Σ Modulator Performance through Maple Tool

The presented work aims to estimate different FF ΔΣ modulators structures used for low and high-speed applications. The prediction is limited to single-bit FF ΔΣ modulator topology whose quantizer is a single-bit one ($B = 1$). Therefore, according to the literature, we fix some standards summarized in Tab. 1 [19-21]. During this phase, to project some FF ΔΣ modulators performance predictions for low power systems, we choose a decreasing power consumption estimated less than 1mW and a variable F_S using future CMOS process (Tab. 2). Tab. 2 presents supply voltages predicted for each process node using the Bisquare Weights method described in [22].

Table 1 ADC specifications for mobile telecommunications standards

Standards	Signal bandwidth (MHz)	Resolution (Bits)
GSM	0.1	13
Bluetooth	1	10-12
UMTS	2	10
WCDMA	3.84	9-12
DVB-H	7.6	9-10
WLAN	10	8-10
WIMAX	20	7-10

Table 2 Specifications

Process nodes (nm) /Supply voltage (V)	Power consumption (mW)	Sampling frequency (MHz)
22/0.68	0.1	
32/0.76	0.2	
45/0.86	0.3	
65/1.2	0.4	
90/1.2	0.5	$20 \leq F_S \leq 520$
130/1.4	0.6	
180/1.8	0.7	
250/2.5	0.8	
350/3.3	0.9	

Constants initialization
(BS, FS, L, Vdd, ai,ei, OL, B, estimated Pmod value)

↓

Performance models
-Equations from Eq.(1) to Eq.(10)
-Eq.(23) and Eq.(24)

↓

Predicted FF delta sigma modulators performance (SNR, ENOB, Pmod and FOM)

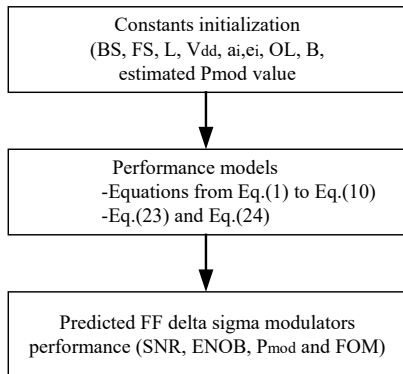**Figure 2** Prediction method of FF ΔΣ modulators performance through maple tool

Aiming at the implementation in Nanometer CMOS technologies, many efforts have been devoted to choose the ΔΣ topology suitable for the ΔΣ ADC design. A detailed analysis has been presented in [23], leading to optimized loop coefficients and performance for various FF ΔΣ modulators architectures. Optimized loop coefficients have been developed from behavioral simulations to stabilize high performance ΔΣ modulator. The loop coefficients represent the analog coefficients (a_i), the feedforward coefficients (c_j) and the digital coefficients (e_k). The adopted prediction method is based on the following steps given by Fig. 2. In fact, we start with introducing some

constants such as the signal bandwidth (BS), the F_S, the supply voltage (V_{dd}), the analog and digital coefficients (a_i and e_k), the order (L), the OverLoad (OL), the quantizer bits number (B) and the estimated value of the FF ΔΣ modulator power consumption (P_{mod}), taking Tab. 1 and Tab. 2 into consideration. After that, the equations models related to FF ΔΣ modulator performance (equations from Eq. (1) to Eq. (10)) are used to present the trend of different single-bit FF ΔΣ modulators performance scaling from 350nm to 22nm process nodes. As an example, we are looking for designing the 2-2 cascaded FF ΔΣ modulator for DVB-H, WLAN and WIMAX standards. Thus, the loop coefficients introduced in the prediction method are taken from Tab. 3 [23].

The analog and the digital coefficients are respectively given by Eq. (23) and Eq. (24):

$$a_i = \frac{C_S}{C_f} \quad \text{where} \ 1 \leq i \leq 4, \tag{23}$$

$$e_2 = \frac{1}{e_1 \cdot a_1 \cdot a_2}. \tag{24}$$

Table 3 Optimized loop coefficients and performance for the single-bit cascaded 2-2 FF ΔΣ modulator

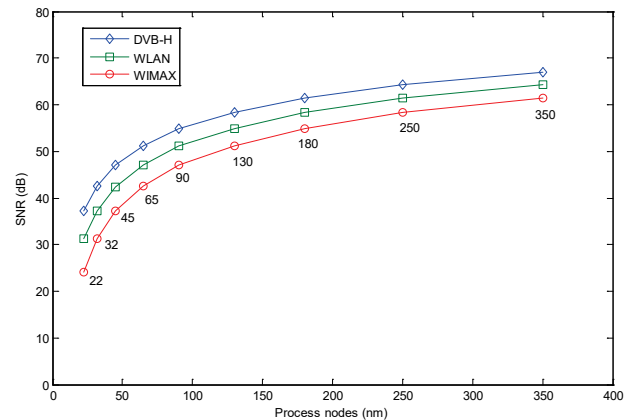| Loop coefficients and performance	(a_1, a_2, a_3, a_4, c_1, c_2, c_3, c_4, e_1, e_2) (0.4, 0.8, 0.4, 0.8, 2, 1, 2, 1, 1, 3.125)	
OSR	*SNR*$_p$	*OL*
16	65	0.95
32	92	0.89
64	121	0.88
128	149	0.85

Figure 3 The scaling of *SNR*

Figs. 3, 4, 5 and 6 show respectively the *SNR*, the ENOB, the power consumption and the FOM scaling of the 2-2 cascaded FF ΔΣ modulator for DVB-H, WLAN and WIMAX standards. Fig. 3 shows that the *SNR* has been scaled from 67 dB to 37 dB when process node is scaling for DVB-H standard. From this figure, it has been remarked that the decrease of *SNR* is due to the F_S reduction when scaling the device sizes. We notice a trade-off between a higher bandwidth and a lower *SNR*. In Fig. 4, due to the *SNR* reduction, the value of the resolution decreases from 11bits. Fig. 6 shows that the *FOM* remains less than 0.26 pJ/conversion when the channel length becomes shorter. Regarding the required human effort for the ΔΣ modulator performance prediction, the time spent is very large. This prompted us to propose a novel method that permits a fast ΔΣ modulator automatic design.

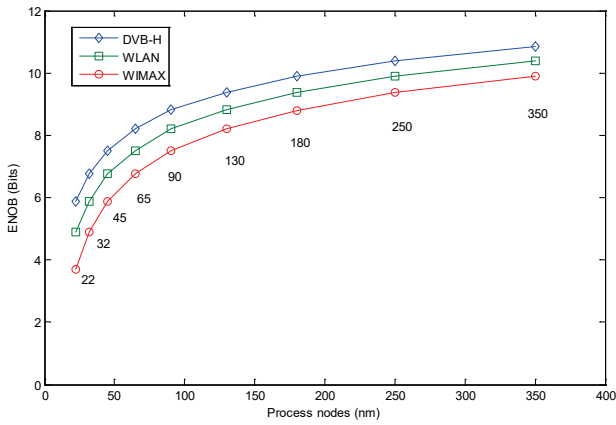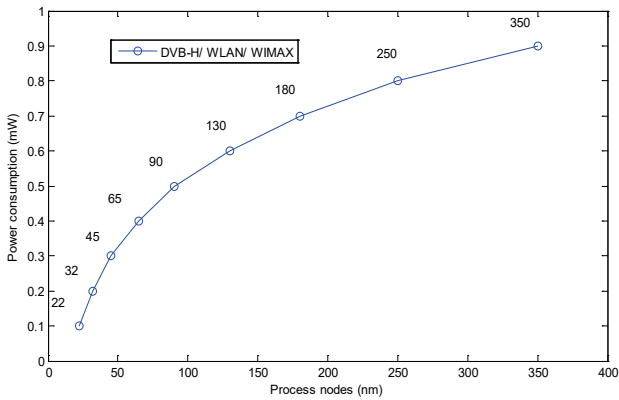**Figure 4** The scaling of *ENOB*
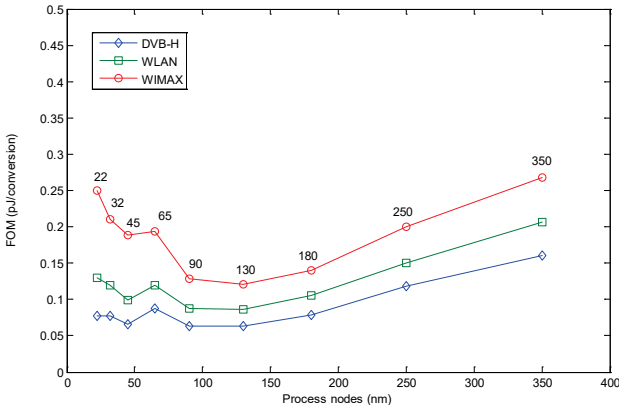

Figure 5 The scaling of power consumption

Figure 6 The scaling of *FOM*

3 AUTOMATED SYNTHESIS TOOL

Our objective is to design different ΔΣ modulators topologies using future process without losing time. For this, we propose a new approach which is based on an algorithm to synthesize low power DT FF ΔΣ modulators.

3.1 Proposed Synthesis Algorithm

This algorithm is developed with "ActionScript 3" language while considering steps listed in Fig. 7. First, we start by setting the wireless standard and the F_S variations ranges listed in Tab. 1 and 2. Then, we choose power consumption less than a maximum default value of 1 mW.
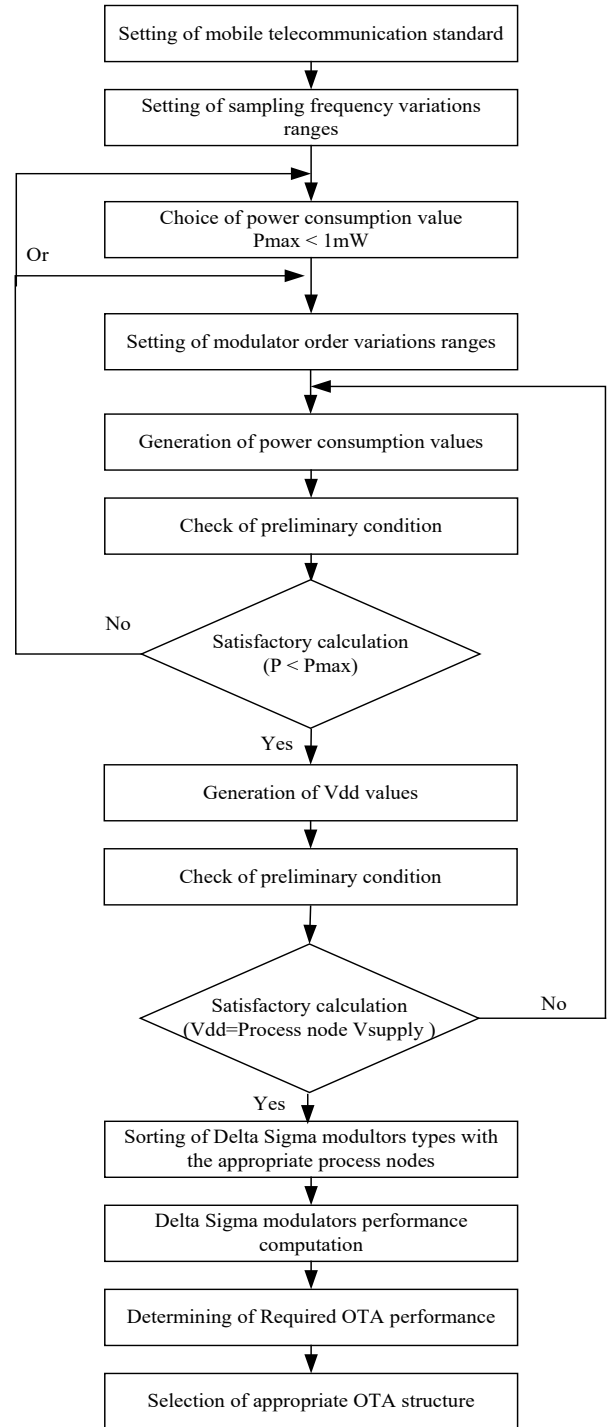

Figure 7 Proposed algorithm for FF ΔΣ modulators automatic design

Next, we indicate the modulator order "*L*" variations ranges. In this case, we choose to predict single loop (SL) 2nd order modulators (*L* = 2), 2-1 and 2-1-1 cascaded modulators (*L* = 3, 4). By using the Eq. (8), all possible values of power consumption are generated followed by a verification of preliminary conditions. This condition consists of checking whether the calculated power consumption of the modulator is less than the maximum power value P_{max} which is initially selected. After that, the generation of possible power consumption values yields to possible generated supply voltages values followed by a verification of preliminary conditions. These conditions are imposed to ensure that the generated supply voltage is equal to the process node supply voltage given by Tab. 2.

If these conditions are fulfilled, the supply voltage is saved and it is a candidate for the following steps, otherwise we do another choice. For each power consumption and process node, a FF ΔΣ modulator type is then defined. The computation of its performance according to their developed equations models (Eq. (1) to Eq. (10)) yields to projected predictions. The characterization of OTA circuit depending on ΔΣ modulator performance is used to calculate the required performance for each designed modulator structure and to find the best adopted OTA architecture (Eq. (13)- Eq. (18)- Eq. (22)).

3.2 FF Δ Σ Modulators Design Examples via Programming GUI

Designing a good User Interface encourages an easy and natural interaction between a user and a system. A graphical application tool is a software program that graphically provides a user with a set of commands and icons with which he can graphically manipulate to generate or modify a design product in a work space area.

The proposed tool provides a wide design environment for designing different FF ΔΣ modulators. In fact, a GUI is programmed with "ActionScript 3" language where the user can easily include the data and display the results. In this subsection, we illustrate the design automation approach with some examples. Tab. 4 lists some required input parameters that the user should define at the beginning. In these examples, we are looking for designing FF ΔΣ modulators structures projected for UMTS, WLAN and WIMAX standards. From Fig. 8, it is seen that the user of the tool can select which standard to take into account during the prediction and set values for their lower and upper bounds.

After defining the design specification, the user waits for possible FF ΔΣ modulators architectures. In fact, the algorithm looks for candidate architectures with the given specifications. Fig. 9 displays various FF ΔΣ modulators topologies predicted for WIMAX standard. For each designed topology, the ΔΣ modulator performance is then computed. Among the availability of many structures, Tab. 5 presents predicted performance of the candidates architectures solutions for each given standard. Fig. 10 presents the corresponding required OTA performance for the provided 2-1 cascaded FF ΔΣ modulator given by Fig. 9. From Tab. 5, it can be concluded that the larger the value of modulator order, the higher the *SNR* is. In fact, the highest *SNR* value is achieved for 2-1-1 cascaded configuration. One of the important features of the design automation tool is the ability to find the best OTA structure for the provided FF ΔΣ modulators (Tab. 6). From Tab. 6, it is clear that for a given set of performance specifications, more than one topology is often feasible. In addition, the required type of OTA circuit can be provided for each calculated OTA performance.
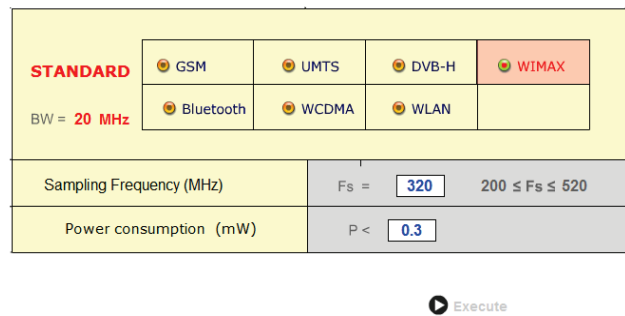

Figure 8 GUI: specifications design

Due to the higher constraint on DC gain, the tool selects an OTA gain-boosted for 2-1-1 cascaded configuration for UMTS standard and a telescopic OTA for the rest.
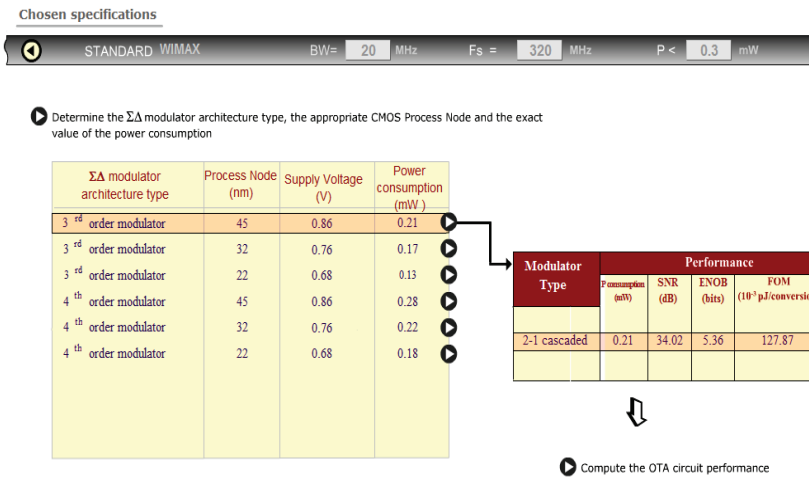
Table 4 Input parameters to the design examples

Standard	BS (MHz)	F_S (MHz)	P_{mod} (mW)
UMTS	2	100	< 0.7
WLAN	10	200	< 0.4
WIMAX	20	320	< 0.3

Table 5 Designed single bit FF ΔΣ modulators structures projected for different standards

Standard	Configuration	Process node (nm)/ Supply voltage (V)	P_{mod} (mW)	Predicted performance		
				SNR (dB)	$ENOB$ (Bits)	FOM (pJ/conv)
UMTS	SL 2nd order	90/1.2	0.52	57.86	9.32	0.203
	2-1-1	45/0.86	0.25	92.54	15.08	0.018
WLAN	2-1	65/1.2	0.39	40.81	6.49	0.217
	2-2	32/0.76	0.21	51.17	8.21	0.035
WIMAX	2-1	45/0.86	0.21	34.02	5.36	0.127
	2-1-1	22/0.68	0.18	48	7.68	0.021

Table 6 Required OTA performance for the provided FF ΔΣ modulators

Standard	Provided configuration Process node (nm)/Supply voltage (V)	Required OTA performance				Selected OTA
		$A_{dc,min}$ (dB)	GBW_{min} (GHz)	SR_{min} (V/µs)	P_{OTA} (mW)	
UMTS	SL 2nd order 90/1.2	64.4	0.84	104.6	0.26	Telescopic
	2-1-1 Cascaded 45/0.86	99.7	1.46	143.8	0.063	Gain-boosted
WLAN	2-1 Cascaded 65/1.2	48.6	1.35	256.4	0.13	Telescopic
	2-2 Cascaded 32/0.76	58.3	1.59	164.3	0.053	Telescopic
WIMAX	2-1 Cascaded 45/0.86	41.8	1.78	242.8	0.07	Telescopic
	2-1-1 Cascaded 22/0.68	55.18	2.38	185.3	0.045	Telescopic

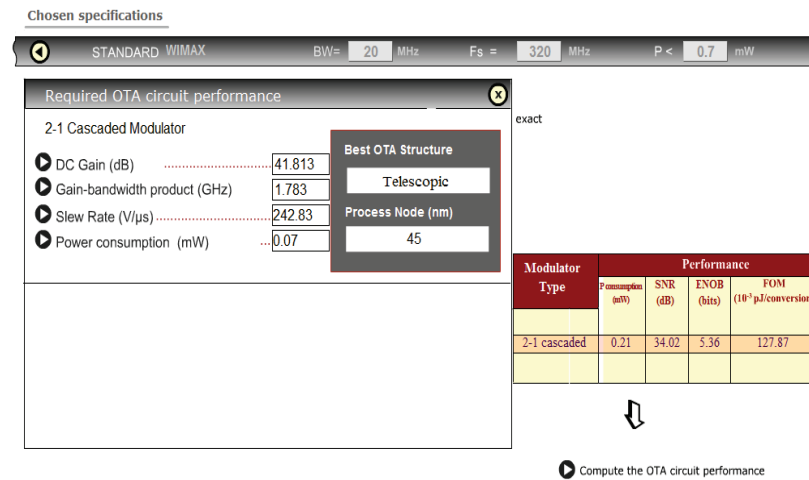**Figure 9** GUI: predicted performance of different modulators architectures for WIMAX standard

Figure 10 GUI: predicted performance of required OTA for WIMAX standard

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4 CONCLUSION AND FUTURE EXTENSIONS

This paper proposed a novel helpful approach for the synthesis of low power FF ΔΣ modulators with process scaling for various mobile telecommunications standards. The procedure of NanoCMOS ΔΣ modulators performance prediction and the use of the MAPLE tool have been presented. Automation of predicting ΔΣ modulators performance is a very challenging and time-consuming task. Thus, a novel automated synthesis tool, which includes FF ΔΣ modulators performance synthesis and OTA performance modeling, has been proposed. A new algorithm has been suggested to provide the prediction of single-bit FF ΔΣ modulators performance for wireless standards. The presented approach proves that the design

effort is reduced with the assistance of an automated tool. Some design examples have been presented through a programmed Graphical User Interface. This GUI was designed allowing convenient and fast access to all functionality. These examples showed that the proposed tool may be used to generate different FF ΔΣ modulators structures types for desired specifications. It has shown that higher SNR can be reached for high order low power modulator topology. This tool reveals the link between both the design and the technological parameters and structures performance to provide an insight to the ΔΣ modulator design problem and lightens up the design environment for the designer. The outcome of the synthesis tool is not only the projected ΔΣ modulator performance, but also the required building block specifications. The

proposed tool is beneficial in predicting the FF ΔΣ modulators performance and the required OTA specifications. It can further shorten the design time for inexperienced designers. The automated synthesis tool can be used to predict the performance of a wide variety of analog circuits and topologies.

In the future, to raise the efficiency of design automation systems, developed analytical models incorporating circuit non-idealities will be introduced further in the proposed synthesis tool. In addition, an extension of this research might be the prediction of transistor sizes of analog circuits for upcoming process using a Nano-CMOS device-level tool to increase its usability

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