

ULTRA LOW POWER MIXER WITH OUT-OF-BAND RF ENERGY HARVESTING FOR WIRELESS SENSOR NETWORKS APPLICATIONS

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Abstract:

An ultra low power mixer with out-of-band radio frequency (RF) energy harvesting suitable for the wireless sensors network (WSN) application is proposed in this paper. The presented mixer is able to harvest the out-of-band RF energy and keep it working in ultra low power condition and extend the battery life of the WSN. The mixer is designed and simulated with Global Foundries' 0.18 μm CMOS RF process, and it operates at 2.4GHz industrial, scientific, and medical (ISM) band. The Cadence IC Design Tools post-layout simulation results demonstrate that the proposed mixer consumes 248 μW from a 1V supply voltage. Furthermore, the power consumption can be reduced to 120.8 μW by the out-of-band RF energy harvesting rectifier.

1 Introduction

Since the WSN has advantages of low cost, flexible, and wide range of applications, it has attracted much attention in recent years. The WSN node is a very important device of the WSN systems, and it can be used as information collector of the wearable devices, temperature, and pressure monitoring, and so on. However, once the WSN node is placed, it should stay there and work as long as possible without frequent maintenance such as the battery replacement. Therefore, the best choice is to make the WSN node work at ultra low power consumption [1]. Fig. 1 is the RF transceiver block diagram of a WSN node. The mixers, filters [2] and oscillator [3] are very important parts of the transceiver, which are one of the most power-hungry blocks of the transceiver system. Designing

of ultra low power consumption mixers could reduce the whole power consumption of the transceiver, which will extend the battery life of the WSN node.

Two important methods are presented to reduce the power consumption of the RF circuits: the forward body bias technique [4-5] and the subthreshold technique [6-7]. However, as the feature size of the CMOS technology scaled down to nanoscale, the short channel effect becomes more and more serious, which results in more complicated current leakage. Furthermore, the leakage power becomes more susceptible to process and temperature fluctuations. As a result, the performance of traditional forward body bias technique is limited [8]. The MOS transistors are not working in their saturation region in the subthreshold technique, although the power consumption could be greatly

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reduced, as well as the circuits with subthreshold technique work at ultra low power. However, also due to the MOS transistors that don't work in their saturation region, the circuits with subthreshold technique have lower voltage gain and poor noise performance.

As we know, there are many RF radio waves in our surroundings, and too many radio waves in the limited wireless frequency spectrum. This is just like having too many people in a crowded room. More people talk, the greater noise is generated, harder is to hear the words of a particular person. Therefore, everybody raises their voice to convey their message. Just like this analogy, the RF transceivers raise their power to transmit their messages, which results in larger out-of-band RF energy in our surroundings. The RF energy harvesting technology is proposed by J. F. Dickson in 1976 and Q. He in 2009 [9-10]. The purpose of this work is to use the RF energy harvesting technology to generate an auxiliary power supply for the mixer with the large out-of-band RF energy and to make the mixer working at ultra low power consumption.

2 Ultra low power mixer design

Figure 2 is the block diagram of the proposed ultra low power mixer. The proposed ultra low power mixer consists of two main parts: the out-of-band RF energy harvesting circuit and the mixer core. The antenna receives the in-band small RF signals and the large out-of-band RF signals simultaneously. The large out-of-band RF signals get into the out-of-band RF energy harvesting circuit, and the energy harvesting circuit is used as an AC to DC rectifier. The energy harvesting circuit converts the large out-of-band RF signals into a DC supply voltage, which provides another auxiliary power supply for the mixer core. Actually, the output of the energy harvesting circuit ($V_{\text{auxiliary}}$) is not always connected to the mixer core. When $V_{\text{auxiliary}} \cong V_{\text{cc}}$, $V_{\text{auxiliary}}$ is connected to the mixer

core as an auxiliary power supply; when $V_{\text{auxiliary}} < V_{\text{cc}}$, V_{cc} is the only supply voltage of the mixer.

The proposed ultra low power mixer is presented in Fig. 3. The proposed mixer consists of the out-of-band RF energy harvesting circuit [11] and the mixer core.

The out-of-band RF energy harvesting circuit includes four NMOS transistors (M_{a1} - M_{a4}) and four PMOS transistors (M_{b1} - M_{b4}), and it is actually a passive rectifier. The RF energy harvesting circuit converts the out out-of-band RF signals into DC supply voltage and provides an auxiliary power supply for the mixer core. The transistors M_{a1} , M_{a2} , M_{a3} , M_{a4} , M_{b1} , M_{b2} , M_{b3} and M_{b4} consist of a small rectifier. The more rectifiers cascaded, the higher is the output DC voltage, and the output DC voltage ($V_{\text{auxiliary}}$) can be adjusted by the number of cascaded rectifiers.

The second part of the ultra low power mixer is the mixer core. M_1 , R_1 , M_2 , M_{2a} and M_3 , R_2 , M_4 , M_{4a} consist of two self-bias current reuse amplifiers, and they are in the transconductance stage of the mixer core. The two self-bias currents reuse amplifiers and have the advantage of higher transconductance gain [12], and they realize the function of converting the intermediate frequency (IF) voltage signals into the currents. The transistors M_5 - M_8 consist of the switching stage of the mixer core. The IF signals and the local oscillation (LO) signal are mixed at the switching stage, and the spectrum shifting of the IF signal is realized. M_{2a} and M_{4a} are the supplementary transistors of M_2 and M_4 , respectively. When the DC supply is provided by the RF energy harvesting circuit $V_{\text{auxiliary}} \cong V_{\text{cc}}$, the drains of the transistors M_{2a} and M_{4a} are connected to $V_{\text{auxiliary}}$; when $V_{\text{auxiliary}} < V_{\text{cc}}$, the drains of M_{2a} and M_{4a} are connected to V_{cc} . There is a switch that controls whether $V_{\text{auxiliary}}$ is connected to V_{cc} . The switch is controlled by a comparator that compares the rectifier output ($V_{\text{auxiliary}}$) with a pre-set threshold voltage (V_{th}).

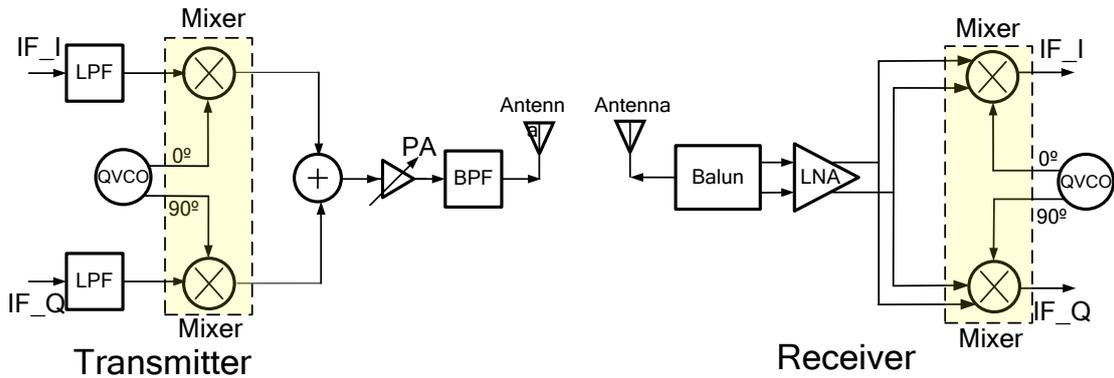


Figure 1. RF transceiver block diagram of WSN node

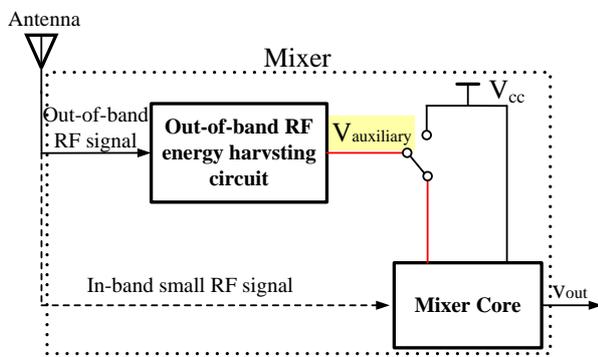


Figure 2. The block diagram of the proposed ultra low power mixer

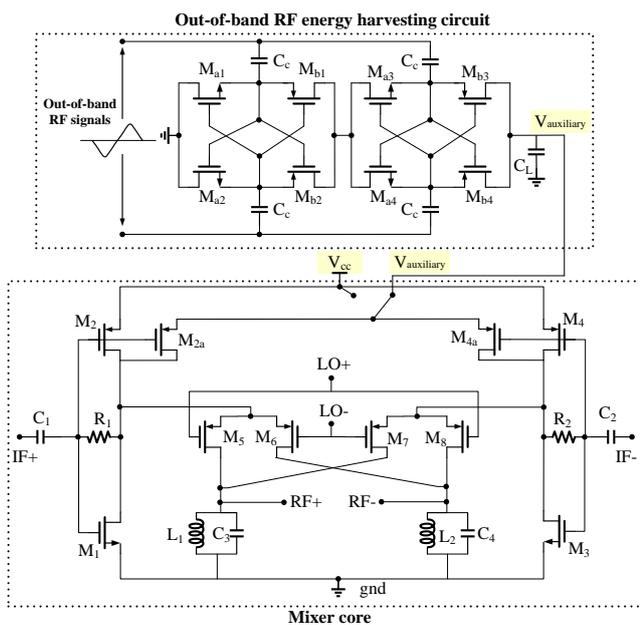


Figure 3. The proposed ultra low power mixer

3 Simulation Results

The proposed ultra low power mixer is designed and simulated with Global Foundries' 0.18 μm CMOS RF process. The proposed mixer consumes 248 μW from a 1 V supply voltage (V_{cc}); however, the power consumption can be reduced to 120.8 μW by using the out-of-band RF energy harvesting rectifier.

Fig. 4 shows the physical chip layout of the proposed mixer, and the Mentor Calibre software is used for its design rule check (DRC) layout versus schematic (LVS) and parasitic extraction (PEX) verification. The active chip area including the bond pads of the mixer is approximately $0.85 \times 1.14 \text{ mm}^2$. After extracting the parasitics and connecting them to the schematic of the mixer, the post-layout simulation results of the mixer are presented in Fig. 5 - Fig. 8.

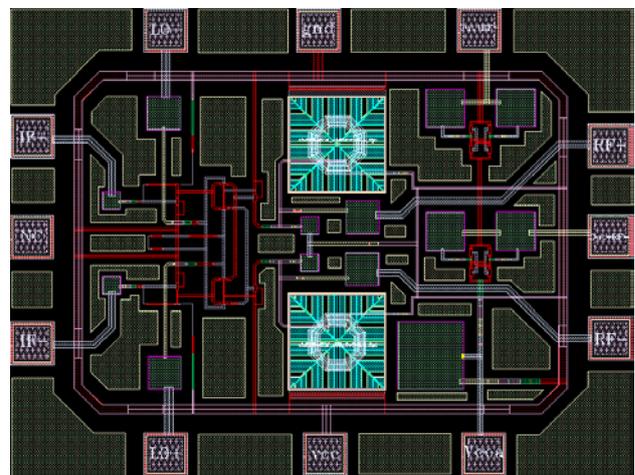


Figure 4. The physical chip layout of the mixer ($0.85 \times 1.1 \text{ mm}^2$)

Figure 5 shows the simulated DC output of the energy harvesting circuit, and the received out-of-band RF signal is set to be 1 dBm and 900 MHz. As we can see from Fig. 4, the output DC voltage of the energy harvesting circuit is about 1.02 V.

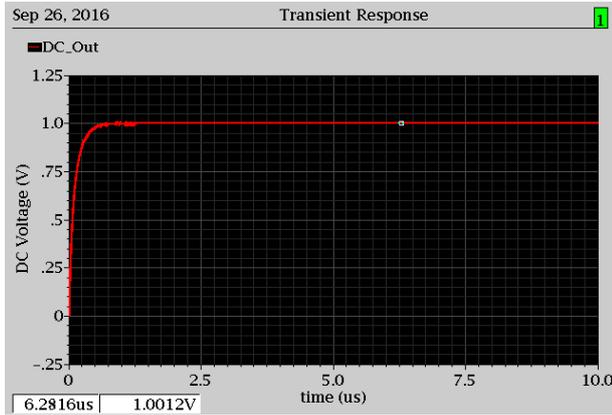


Figure 5. The DC output of energy harvesting circuit

The rising time of the DC voltage to 1.02 V is about 0.75 μ s, and it provides a good auxiliary power supply for the ultra low power mixer. Fig. 6 is the

transient analysis of the proposed ultra low power mixer. The frequency of the IF signal is chosen to be 100 MHz, and its signal level is -30 dBm.

Figure 7 shows the simulated third order intermodulation (IIP3) point of the ultra low power mixer, and the IIP3 of the mixer is about -3.5 dBm. Fig. 8 represents the voltage conversion gain versus LO power of the proposed mixer. From Fig. 8, it is clear that the proposed ultra low power mixer provides relatively large conversion gain when the input LO power changed from -2 to 2 dBm. Moreover, when the input LO power is 1.5 dBm, the largest conversion gain is about 8.2 dB.

A performance summary and comparison with the other related works are presented in Table 1. As we can see from Table 1, the proposed ultra low power mixer has advantages which include lower voltage and better linearity. In particular, the proposed mixer has the lowest power consumption than all the other recently reported works by using the out-of-band RF energy harvesting circuit. Due to its high linearity and ultra low power consumption, the mixer is very attractive for the WSN applications.

Table 1. Comparisons of the proposed mixer with other related works

References	[13]	[14]	[15]	[16]	Proposed
Technology (nm)	180	65	350	130	180
Supply voltage (V)	1.8	1	3.3	0.35	1
Power (mW)	17	6	50	0.52	0.25/0.12
Conversion gain (dB)	8	11	43	16	8.2
IIP3 (dBm)	>4.9	~	~	-7.45	-3.5
LO power (dBm)	5	-9	~	-4	1.5
Frequency (GHz)	2.5	120	2.7	2.4	2.4
Chip area (mm ²)	~	0.12	13	1.03	0.93

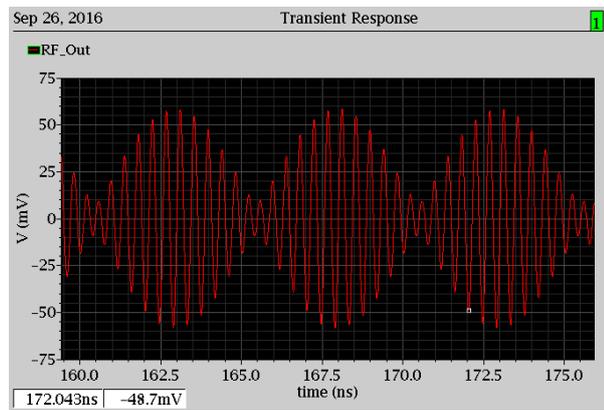


Figure 6. The transient response of the mixer

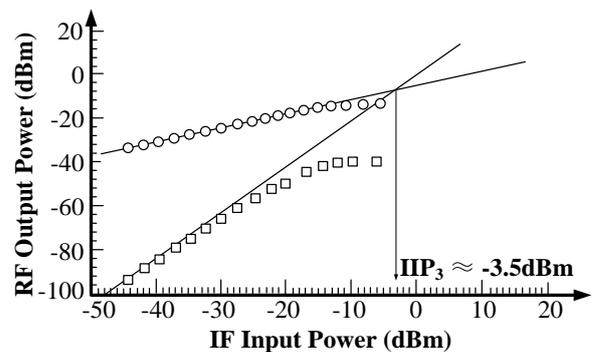


Figure 7. The IIP3 of the ultra low power mixer

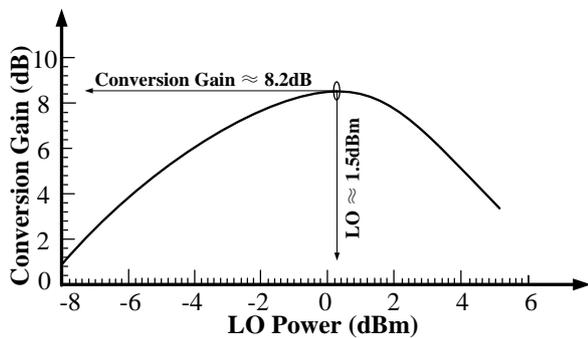


Figure 8. Conversion gain of the ultra low power mixer

4 Conclusion

An ultra low power mixer is presented in this paper. The mixer operates at 2.4 GHz ISM band, and by using the out-of-band RF energy harvesting circuit, the power consumption of the mixer is reduced from 248 μ W to 120.8 μ W, which greatly reduces the power consumption of the transceiver of the WSN node.

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References

- [1] Siminiati, D.: *Energy saving with close circuit pneumatic system*, Engineering Review, 30 (2010), 2, 111-116.
- [2] Zhu S., Hu B.: *Key technologies of active power filter for aircraft: a review*, Engineering Review, 36 (2016), 3, 221-237.
- [3] Jin J., Xiao L., Yang X., Liao B., Li S.: *Dual-mode multi-phase sinusoidal oscillator with equal amplitudes*, Engineering Review, 36 (2016), 3, 211-220.
- [4] Wu, D., Huang, R., Wong, W., Wang, Y.: *A 0.4-V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application*. IEEE Microw. Wirel. Compon. Lett., 17 (2007), 7, 543-545.
- [5] Hsieh, H. H., Wang, J. H., Lu, L.H.: *Gain-Enhancement Techniques for CMOS Folded Cascode LNAs at Low-Voltage Operations*, IEEE Trans. Microw. Theory Tech., 56 (2008), 8, 1807-1816.
- [6] Kim, S.: *A Subthreshold CMOS RF Front-End Design for Low-Power Band-III T-DMB/DAB Receivers*, ETRI Journal, 33 (2011), 6, 969-972.
- [7] He, S., Saavedra, C. E.: *An Ultra-Low-Voltage and Low-Power $\times 2$ Subharmonic Downconverter Mixer*, IEEE Trans. Microw. Theory Tech., 60 (2012), 2, 311-317.
- [8] Agarwal, S. Mukhopadhyay, A. Raychowdhury, K. Roy, C. H. Kim: *Leakage Power Analysis and Reduction for Nanoscale Circuits*, IEEE Micro, 26 (2006), 2, 68-80.
- [9] Dickson, J. F: *On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique*, IEEE J. Solid-State Circuits, SC-11 (1976), 3, 374-378.
- [10] He, Q., Huang, K., Liu, C.: *A Compact 5.8GHz Rectifying Circuit Design and Experiments*, PIERS Proceedings, 2009, 23-27.
- [11] Vamsi, N., Priya, V., Dutta, A., Singh, S. G.: *A 1V, -26dBm sensitive auto configurable mixed converter mode RF energy harvesting with wide input range*, 2016 IEEE ISCAS, 2016, 1534 - 1537.
- [12] Wang, J. Jin, F. Yu.: *A CMOS 2-11 GHz Continuous Variable Gain UWB LNA*, IETE Journal of research, 56 (2010), 6, 367-372, 2010.
- [13] Priyanka, A. K. Singh, N. Pandey: *Implementation of Ultra Low Power Diode load based Gilbert cell mixer for wireless applications*, 2015 Annual IEEE India Conference (INDICON), 2015, 1-5.
- [14] Lee, J.: *A D-Band Gain-Boosted Current Bleeding Down Conversion Mixer in 65 nm CMOS for Chip-to-Chip Communication*, IEEE Microw. Wirel. Compon. Lett., 26 (2016), 2, 143-145.
- [15] Jung, H.B., Jung, W.J., Lim, S., Lim, J. Lee, K.H. Nam, N.P. Hong, J.E. Jang, J.S. Park; *A low power and high linearity dual path up-down converter for wireless telecommunication*

repeater system, 2014 IEEE Radio Frequency Integrated Circuits Symposium, 2014, 377-380.

- [16] Tan, G. H., Sidek, R. M., Isa, M. M.: *Design of Ultra-Low Voltage and Low-Power CMOS*

Current Bleeding Mixer, Circuits and Systems IEEE, 2015, 344-347.