

ENERGY TRANSFORMATION WITHOUT USING FILTER ON HIGH RESISTIVE LOAD

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Abstract:

In this paper, 9-level, 17-level, 19-level, 21-level, 27-level, and 39-level inverters with SPWM are presented. According to a switching function, the high-multilevel inverter design has been described since a new multi-level inverter structure is considered. The multilevel inverter structure is designed with placing switches and sources on levels. Pulse width modulation, controlling switches in the inverter structure, is also produced by comparison between triangles and sinus signals. Operating sequences of the switches are given in the table in order to demonstrate the inverter operation characteristic with the produced signals. Then, mathematical equations are formed by considering an operation of switches on the load. In simulations and experiments, the 9-level, 17-level, 19-level, 21-level, 27-level, and 39-level inverters are performed on the resistance (R) and inductance (L) loads with different resistance, because it is difficult to generate current and voltage with an acceptable harmonic distortion on the impedances which have high ohmic values. After applications of experimentation and simulation, the obtained results are compared with other published papers of results and the international IEEE standard, which is 5% for harmonic distortions of creating currents and voltages.

1 Introduction

Usage of power electronic circuits in modern electrical systems is increasing because multilevel inverters have provided a strong contribution in power energy conversion. In multilevel inverter topologies, an H-bridge inverter is important for energy providing technology in the industry and agriculture works [1-3]. So, inverters have been widely used in power compensation, solar energy power converting, energy storage systems, and electric machine drives [4-5]. However, they also can produce serious power quality problems such as

harmonic pollution [6, 7]. While harmonic distortions in generating current can be reduced to an accepted level on impedances which have a low resistance value, the harmonic distortions of converting voltage cannot be reduced to an accepted level. Hence, while analyzing harmonics of generating current in the inverter applications, harmonic analysis of generating voltage cannot even be encouraged. This affects the performance of the whole system. It is necessary to use a new high-level inverter to get rid of undesirable effects and increase a quality of energy. In this study, a new high multi-level inverter is implemented with

SPWM. Therefore, the 9-level, 17-level, 19-level, 21-level, 27-level, and 39-level high multilevel inverters are studied with SPWM for the first time in literature because new circuit structure of 39-level inverter has only been applied in the study. The multi-level inverter in this study is composed of a single source on a single H full bridge while the other multi-level inverter uses multiple H bridges and multiple sources. So, the inverter levels in old studies are not increased too much [14-17]. Therefore, the switching scheme and the operation algorithm of the proposed inverter differ from those of other inverter operations.

Pulse width modulations for system control are produced after the inverter switch structure is designed with IGBTs and source. While a sinus signal and 8-triangle signals are compared to control switches of the 9-level inverter, a sinus signal and 38-triangle signals are compared to control switches of the 39-level inverter.

According to operation order of switches given, mathematical equations are formed. The proposed inverters are tested on the resistance and inductance loads that have impedances from 0.1ohm to 9ohm while 0.001 Henry of inductance is constant in impedance. It is difficult to cause a distortion in the desired standard levels in loads with high reactance and resistive values. To test the performance of an inverter on the load that will cause more distortion; the reactance values of R, L loads can be increased by increasing the frequency. Therefore, while generating an alternating voltage on the load, a frequency value of 80 Hz is used to increase the reactance value of the R, L load, unlike the 50 and 60 Hz frequency values used in country power line systems. In experimentation and simulation, the voltage generated by the 27 and 39-level inverters on load are obtained. So, it is possible to compare experimented and simulated images of the generated voltage. The quality of powers is analyzed by calculating power when the proposed inverters are operating on different loads. After that, the obtained results are evaluated. According to the evaluation results, there were some contributions. The voltage generated by the high-level inverter was too close to a sinusoid although the voltage was not applied to a filter process. Harmonic values on the generated voltage in this work were quite acceptable when the harmonic distortion of the generated voltage was very high and unacceptable in other studies [14, 15]. In addition, the generated power varied from 63 KVA to 3.447 KVA, while for a creating voltage the harmonic distortion, which reduces power quality

was less than 5%, which is the value allowed by the international IEEE standards. According to the results, the distortion of the creating voltage was also 2.45% that is lower than the permissible distortion of upper value in the IEEE standards. Harmonic distortions on voltage decreased to a low level while the inverters were being built by raising levels in an easy and intelligible manner. So, the proposed system provided a significant contribution to this field by showing a superior performance.

2 Inverter structure and generation of PWMs

PWMs were widely used to control power switches [8-13]. Although there are applications of sinus pulse width modulation (SPWM) for inverters, the SPWM are adopted from the 9-level inverter to the 39-level inverter for the first time. Fig. 1 shows how to generate PWMs for the 9-level inverter.

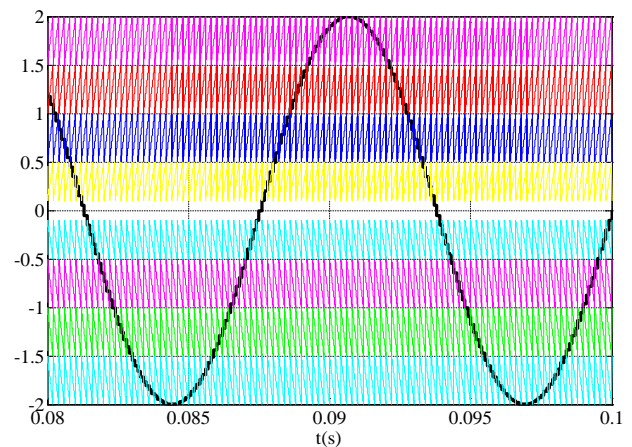


Figure 1. generation of PWM for 9-level inverter

Figure 2 shows how to generate PWMs for the 17-level inverter. For the 9-level inverter, a sinusoidal signal is compared to eight triangle signals in Fig. 1.

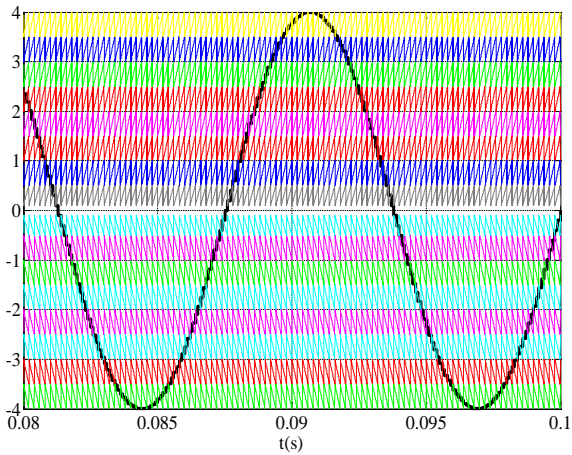


Figure 2. generation of PWM for 17-level inverter

For the 17-level inverter, a sinusoidal signal is compared to sixteen triangle signals in Fig 2. Fig. 3 shows the 21-level inverter. Twenty-IGBT switches and nine-piece source voltage divider are built into the 21-level inverter structure. In order to control the switches of the 21-level inverter, one sinus signal is compared with ten triangle signals. A number of switches on the negative side of the inverter increase two while the numbers of switches on the negative side of the inverter remain constant. This makes it possible to use a lower number of IGBTs for multilevel inverters. Thus, twenty-two switches are used for the 21-level inverter, while forty switches are used for the 39-level inverter. The operating characteristic of the switches with generated PWM signals is given in level in Table 1.

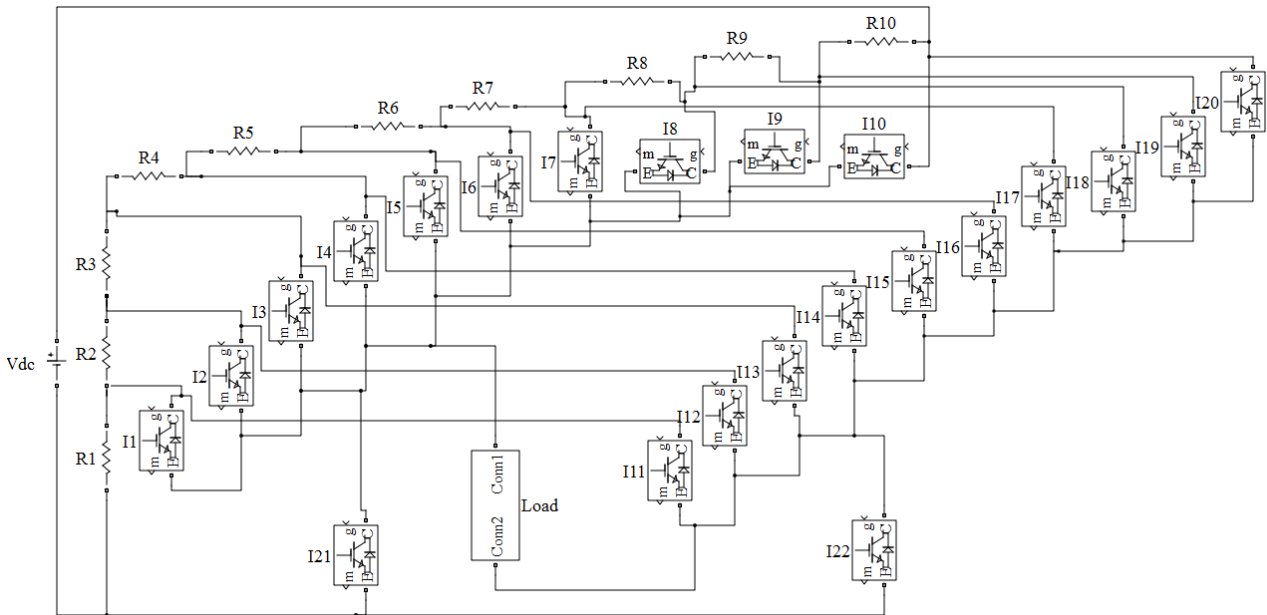


Figure 3. The 21-level inverter

Eq. (1) and Eq. (2) are obtained when I_1 - I_{11} - I_{21} - I_{22} operating on R and L loads at level-2 and level-12. α is phase shift. wt is electrical angle as radians. V_m is maximum voltage. i is load current. While the first level voltage, which depends on the current on the R and L load, is given on the right side of the equation, the first level voltage is calculated with using the phase angles of sinus on the left side of equation. At other levels, the voltage values formed by the shifting phase angles relative to the level state, and the voltage equation created according to the current formed on the R, L load at these levels are equalized. V_{L1} is level-1 voltage.

$$V_{L1} = V_m \cdot \sin wt - 9 \frac{V_m}{10} \cdot \sin(wt_1 + \alpha_1) \quad (1)$$

$$V_m \cdot \sin wt - 9 \frac{V_m}{10} \cdot \sin(wt_1 + \alpha_1) = i_1 R + \frac{di_1}{dt_1} L \quad (2)$$

Eq. (3) is created when I_2 - I_{12} - I_{21} - I_{22} operating on R and L loads at level-3 and level-13.

$$9 \frac{V_m}{10} \cdot \sin wt_1 - 8 \frac{V_m}{10} \cdot \sin(wt_2 + \alpha_2) = i_2 R + \frac{di_2}{dt_2} L \quad (3)$$

3 Inverter simulations and experimentation results

The proposed circuit is simulated by MATLAB/Simulink software. Then, for validating the practicability and the high performance of the suggested High Multilevel Inverter, experimental results are obtained. To ensure the DC voltage, the adjustable DC sources in the laboratory are used. First, when the 9-level inverter is tested on resistance and inductance loads, the forming load voltage is as given in Fig. 4(a). For the 9-level inverter, the harmonic distortion of the voltage on the load is as given in Fig. 4(b). $R=9\text{ Ohm}$, $L=1\text{mH}$.

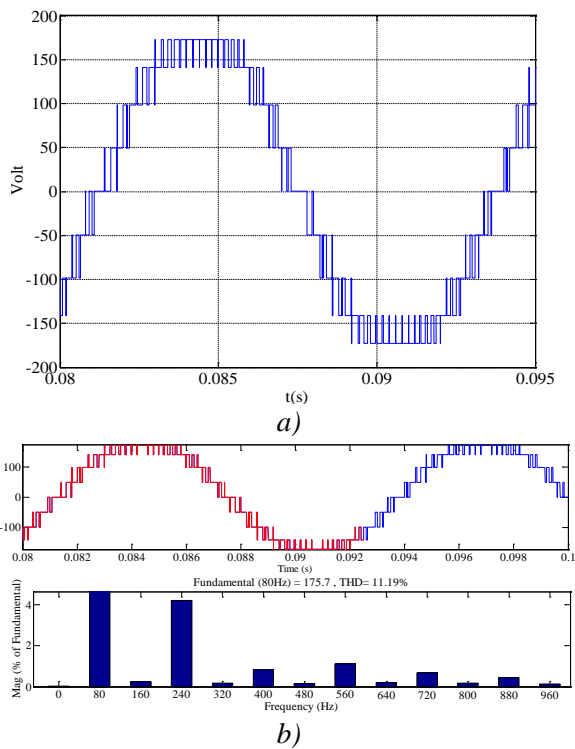


Figure 4. a) the forming load voltage for the 9-level inverter b) The harmonic distortion of the voltage

The harmonic distortion of voltage on load for the 9-level inverter is 11.19%, while the harmonic distortion of the generated current is 2.1%. The voltage generated on load is similar to a sinusoid with the negative and positive periods equal. The sum of these periods equals zero. When the 17-level inverter is performed on resistive and inductive load, the forming load voltage is as given in Fig. 5(a). For a 17-level inverter, the harmonic distortion

of the voltage on the load is as given in Fig. 5(b). $R=9\text{ ohm}$, $L=1\text{mH}$, switching time = $1\mu\text{s}$.

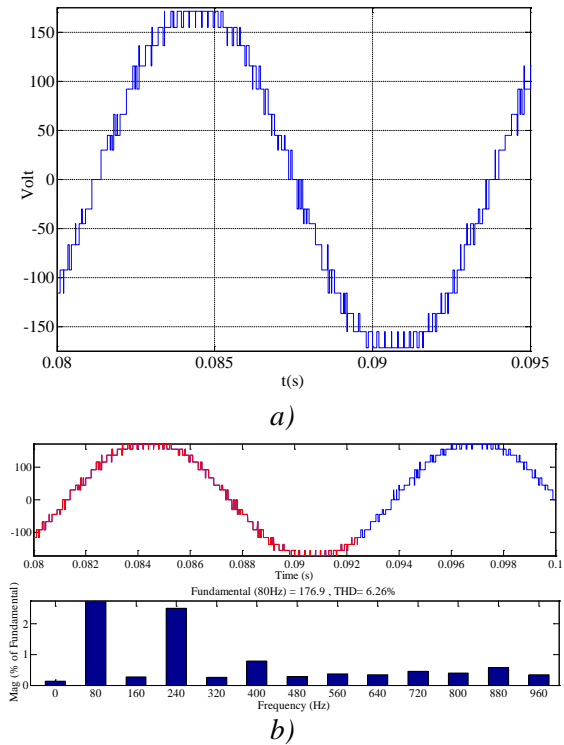


Figure 5. a) the forming load voltage for the 17-level inverter b) the harmonic distortion of the voltage

Table 2. Experimental System Parameters for the prototype

Source voltage Vdc	175Volt
Loads R	0.1, 1, 3, 6, 9 Ohm
Load L	0.001 Henry
Controller	dspace 1104
IGBT Switches	IRGB4055PbF
Switching time T_s	100 microsecond
owon oscilloscope	

The harmonic distortion of voltage on load for the 17-level inverter is 6.26 %, while the harmonic distortion on generating current is 0.92 %. The voltage generated on load is similar to a sinusoid with the negative and positive periods equal. The sum of these periods equals zero. When the 17-level inverter is running at resistive and inductive loads, the created voltage is as given in Fig. 6(a). For a 19-level inverter, the harmonic distortion of voltage on the load is as given in Fig. 6(b).

The harmonic distortion of the voltage on the load of the 19-level inverter is 5.23 %, while the harmonic distortion of the generated current is 0.66 %. The voltage generated on the load is similar to the sinusoid with the negative and positive periods. The sum of these periods equals zero. These results are acceptable for energy converting.

When the 21-level inverter is performed on resistive and inductive loads, the forming load voltage is as given in Fig. 7(a). For a 21-level inverter, the harmonic distortion of the voltage on the load is as given in Fig. 7(b). $R=9\text{ Ohm}$, $L=1\text{mH}$. Switching time = $1\mu\text{s}$.

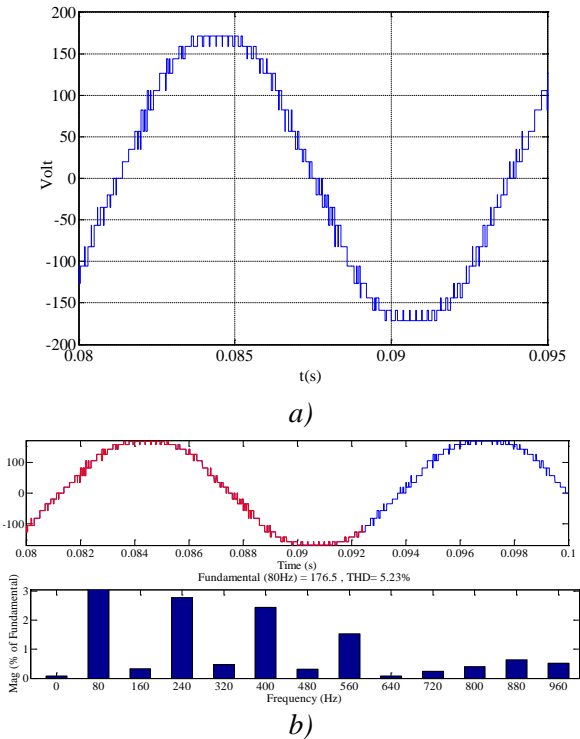


Figure 6. a) the forming load voltage for the 19-level inverter b) the harmonic distortion of the voltage

The harmonic distortion of voltage on load for the 21-level inverter was 4.11 %, while the harmonic distortion on generating current was 0.32 %. The voltage generated on the load was similar to the sinusoid with the negative and positive periods equal. The sum of these periods equaled zero. When the 27-level inverter was performed on resistive and inductive loads, the load voltage was formed with simulation in Fig. 8(a). For a 27-level inverter, the harmonic distortion and the voltage of experimentation on load are as given in Fig. 8(b). It

is possible to compare the experimented and simulated images of the generated voltage. $R=9\text{ohm}$, $L=1\text{mH}$, switching time = $1\mu\text{s}$.

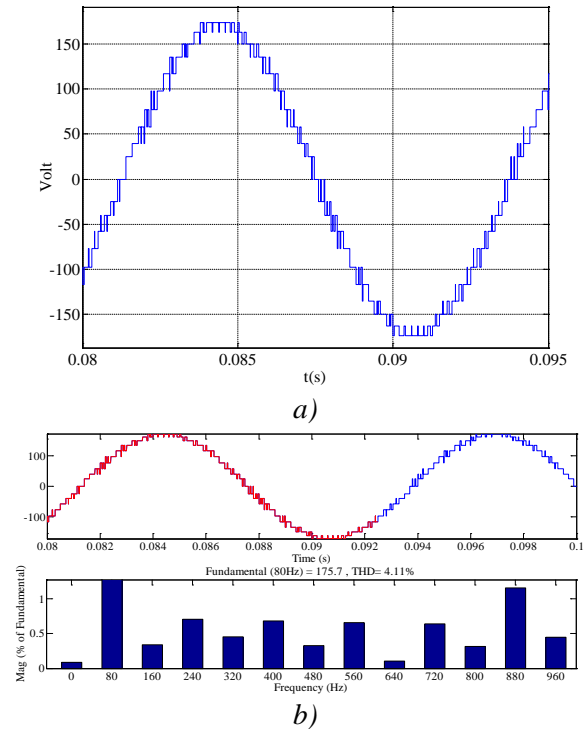
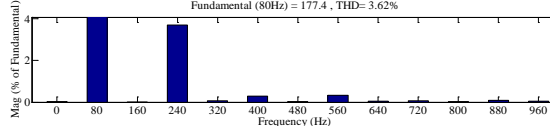
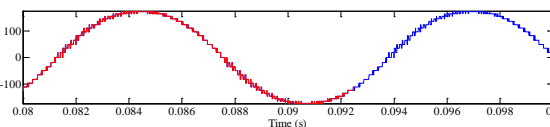
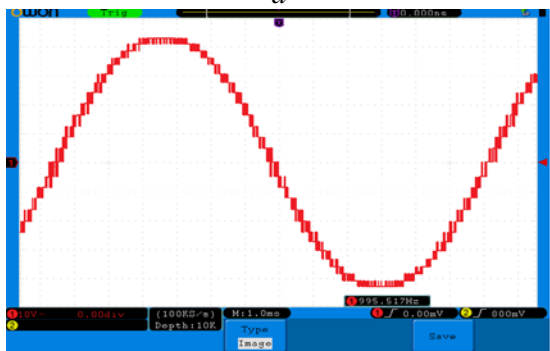
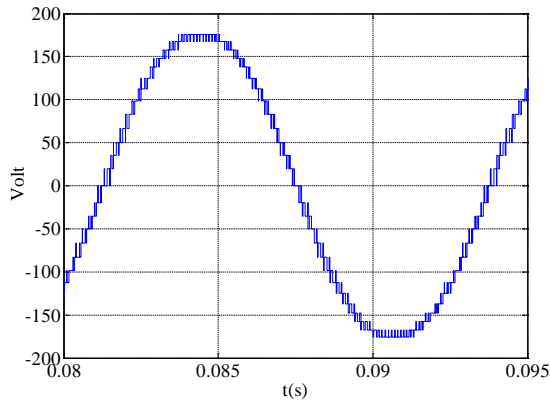


Figure 7. a) the forming load voltage for the 21-level inverter b) the harmonic distortion of voltage

The harmonic distortion of the voltage on the load of the 27-level inverter was 3.62 %, while the harmonic distortion on generating current is 0.29 %. The voltage generated on load was similar to a sinusoid at simulation and experimentation in Fig. 8. The sum of positive and negative parts of voltage was zero. The voltage simulated for the 35-level inverter on load is shown in Fig. 9(a). Fig. 9(b) gives the harmonic distortion and the generated voltage of experimentation. $R=9\text{ Ohm}$, $L=1\text{mH}$, switching time = $50\mu\text{s}$.

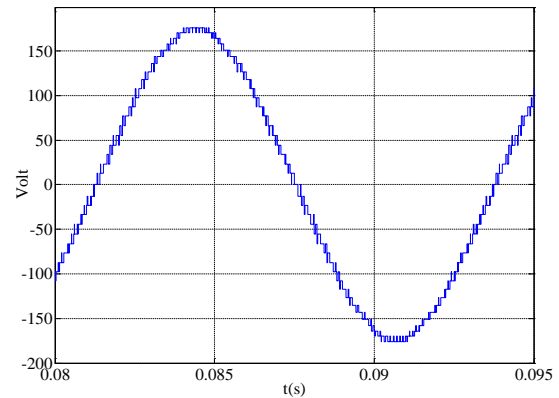
The voltage generated by the 39-level inverter is much closed to a sinusoid in simulation and experimentation while the harmonic distortion of converting voltage was 2.65 %, proving the quality sinus. The harmonic values on the voltage generated in this work were the acceptable level, while the harmonic distortion of the generated voltage was very high in some other studies [12- 13]. In addition, these results were very acceptable for energy converting. For impedances with low resistance loads as 0.1ohms , the harmonic distortion

of the current can be at acceptable levels, but this is very difficult for impedance with high resistance loads which are from 1ohm to Infinite ohm. Hence, when the inductance of impedance is 0.001 Henry, resistance of impedance from 0.1ohms to 9ohm has been tried in Matlab Simulink. U is alternating voltage on 39- level while U max is 175volt.

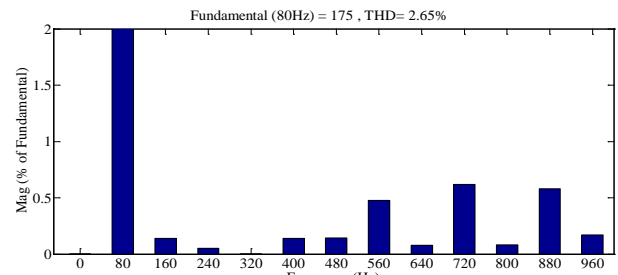


b)

Figure 8. a) the forming load voltage for the 27-level inverter, b) The harmonic distortion of the voltage and experimentation from oscilloscope



a)



b)

Figure 9. a) the forming load voltage for the 39-level inverter b) The harmonic distortion of the voltage and experimentation from own oscilloscope

I1, I2, I3, I4 and I5 are currents in Fig. 10(a). Z1 is impedance for I1 while $Z1 = 0.1+j0.001$. Z2 is impedance for I2 while $Z2 = 1+j0.001$. Z3 is impedance for I3 while $Z3 = 3+j0.001$. Z4 is impedance for I4 while $Z4 = 6+j0.001$. Z5 is impedance for I5 while $Z5 = 9+j0.001$.
 $I1 = 175/0.1+j0.001$. $I2 = 175/1+j0.001$.
 $I3 = 175/3+j0.001$. $I4 = 175/6+j0.001$.
 $I5 = 175/9+j0.001$. The harmonic distortion of 39-level and 27-level inverters for different power values is given in Fig. 10(b).

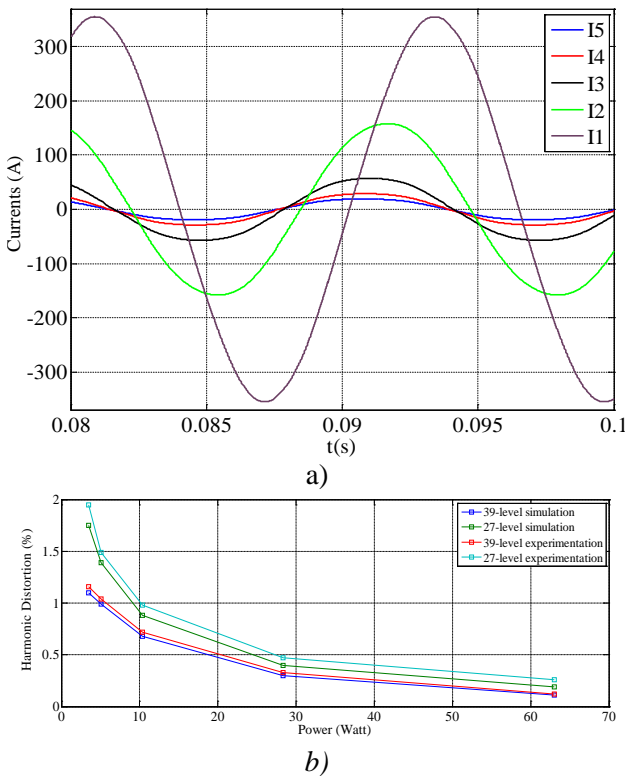


Figure 10. a) currents for different impedances b) harmonic distortions for different power

Powers produced by 39-level inverter were S1, S2, S3, S4, and S5. $S1 = 175 \times 360 = 63 \text{ KVA}$ (Kilo Volt Ampere). The current of S1 included 0.11% for harmonic distortion while the voltage of S1 included 2.65% of harmonic. $S2 = 175 \times 162 = 28.35 \text{ KVA}$. The current of S2 had 0.3% for harmonic distortion while the voltage of S2 had 2.65% of harmonic. $S3 = 175 \times 59 = 10.375 \text{ KVA}$. Current harmonic distortion of S1 was 0.68% and voltage harmonic of S3 was % 2.66 as in S1, S2. $S4 = 175 \times 29 = 5.075 \text{ KVA}$. Distortion was 0.99% for the current of S4. $S5 = 175 \times 19.75 = 3.447 \text{ KVA}$. Distortion was 1.1% for the current of S5. The generated power varied from 63 KVA to 3.447 KVA, while the harmonic distortion, which reduces power quality, was less than 5%, which is the value allowed by the international IEEE standards. So the proposed system provided a significant contribution to this field by showing a superior performance. The current generated in the five impedance values formed exactly as a sinus shape, while the sum of the positive and negative periods was zero. Fig. 11 shows the harmonic distortion curves of the generated current on impedances having five different resistance values.

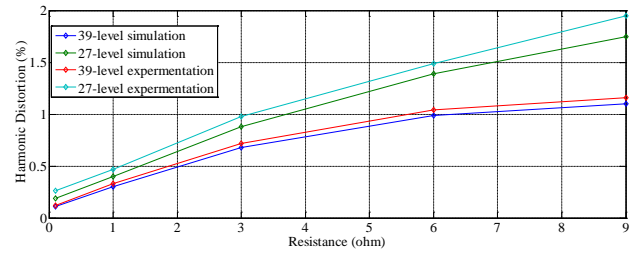


Figure 11. The harmonic distortion curves of the current generated on five impedances for 27-level and 39-level inverters

The 27-level inverters run five different impedances. While the harmonic distortion of generating currents extended from 0.29% to 1.43%. These values were considerably lower than the acceptable level, which is 5%. If the 35-level inverter run five different the impedances, while the harmonic distortion of the generated currents extended from 0.11% to 1.1%. These values were considerably lower than the acceptable level and the results of other multilevel inverter applications.

4 Conclusion

The SPWM was applied to the high-level inverter topology. Therefore, the 9-level, 17-level, 19-level, 21-level, 27-level, 39-level High Multilevel Inverters were performed for the first time in the literature. The results were obtained by observing the voltages and currents generated while simulation results were validated with experimentation works. Despite of that there was no a filter system, the voltages generated on the load were similar to sinusoid with the negative and positive periods. The sum of these periods equaled zero. It is very difficult (It was difficult to find?) that the harmonic distortion of alternating voltage in inverter application was at an acceptable level. However, the proposed inverter application provided a low harmonic distortion with satisfactory values on the converted voltage and currents, although loads included from a low resistance value to a high value. According to the harmonic distortion analysis of the voltages, the harmonic values of the voltage decreased from 11.26% to 2.65 % by increasing inverter level. These results were very low and acceptable levels while compared with previous studies and the international IEEE standards for a converted energy and an inverter application.

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