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Simulation and experiment of algorithm and circuit design for UPQC

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ABSTRACT

Power quality issues have become one of the most important issue for researchers to concern. In this paper, simulation and experiment of algorithm and circuit design of Unified Power Quality Conditioner (UPQC) are provided. Control algorithm and topology design of one UPQC which includes active power filter (APF) and dynamic voltage restorer (DVR) are introduced. Stability condition of the filter unit is deduced and proved by Routh stability criterion. Simulation for APF and DVR is carried out in PSCAD to show the proposed control strategy. Experiments such as current tracking, harmonic detection and compensation and voltage drop compensation are provided in details. Experimental results show that the proposed control method and the designed topology are effective and practical.

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KEYWORDS
Voltage sag; harmonic current; DVR; APF

1. Introduction

The introduction of distributed energy and renewable energy to our daily lives makes it an inevitable tendency for us to concern power quality issues more than ever. Different roles, such as power generation, transmission and distribution, along with the value chain must now cooperate and interact with each other by shared interfaces or eventually a customized network for secure and reliable delivery of energy, this can be called as energy internet [1]. This new form of energy supply has the following new characteristics: (i) structure features: power grid topology has more complex structure types (tree or mesh), flow types (unidirectional or bidirectional) and energy consumption programs (on demand or dynamic balance); (ii) environmental characteristics: most distributed energy have characteristics of instability (solar energy, wind energy and tide are influenced by environmental factors); (iii) functional features: plug and play puts forward higher requirements for the power quality management ability as dynamic change exists in both sources and loads. So stability and reliability would be of paramount importance for the coming form of power supply system [2–5]. For instance, due to the intermittent nature of the PV energy sources or wind turbine sources, considerable complexity and variability are introduced into the micro grid [6–8]. Furthermore, in the coming energy internet, more and more plug and play units such as new energy power generation would be introduced to the grid, then so many types of energy input are integrated together, higher challenges are presented for the maintenance and enhancement of power quality of power grid [1, 9–12]. Research on power quality conditioner has been carried out extensively [13–16]. Key units such as DC support unit and filtering unit have been deeply studied by researchers as well [17–19]. In this paper, we focus on topology design and simulation and experiment of the designed UPQC (Unified Power Quality Conditioner) system.

Based on the above requirements, we proposed a LAN-based UPQC system for maintaining power quality for the mentioned coming energy internet. Figure 1 shows the control diagram of the designed UPQC.

The main feature of this LAN-based UPQC is that it can adjust compensation strategy by using feedback information from users. The recorder is installed on user side; it sends start up time or shut down time or any other key information to LAN-Controller for UPQC to prepare compensation action. Besides, it can collect user equipment's electrical performance data and by which the UPQC can get a better understanding of its compensation target. This warning information can provide UPQC with short but decisive time to prepare for the coming voltage sag or harmonics. By doing this, the response time and the support time can be effectively improved. The design of UPQC is shown in Figure 2. In this system, UPQC controls APF (active power filter) as a controlled current source. The APF is responsible for compensating the harmonic current, negative sequence current and zero sequence current generated by the load. For this reason, APF adopts four-arm structure. APF is also responsible for stabilizing DC capacitor voltage and charging

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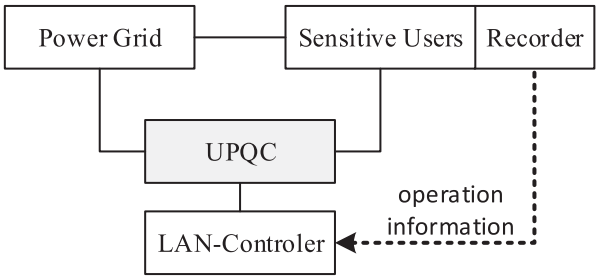


Figure 1. Block diagram of LAN-based UPQC system.

DC super capacitors. Dynamic voltage restorer (DVR) is responsible for compensating the system voltage sag, so that the load voltage is kept as the rated three-phase symmetrical positive sequence voltage. The negative sequence and zero sequence voltage that may occur during the system sag can be compensated. So three single phase DVR structures are adopted.

The simulation and experiment of the designed system are provided in detail. The compensation algorithm in APF and DVR is briefly introduced. Then, filter design is given, and stability analysis of feedback-inverter-filter link is provided. Simulation and experiment for current tracking, harmonic detection and compensation, voltage sag compensation are provided.

2. Compensation control algorithm

2.1. Control algorithm of DVR unit

In series side (DVR unit), the control unit must be able to track the instructions quickly and accurately within the acceptable range of error. According to the equivalent block diagram of DVR series compensator in Figure 3(a), we can get the closed loop control method of DVR output voltage as is shown in Figure 3(b).

In Figure 3(b), V_S is the system voltage, V_{dvr} is the output voltage of DVR setup. V_{lref} is the instruction voltage. $G_V(s)$ is the controller of voltage outer loop, $G_i(s)$ is the controller of current inner loop, V_{tri}/V_{dc} is the voltage transformation, $G_{inv}(s)$ is the inverter bridge modulation model which is in relationship with V_{dc}/V_{tri}. In order to improve the dynamic performance of the system, instantaneous value feedback of capacitor voltage structure is used as voltage outer loop of control system. After adjustment of proportional integral block, error signal of voltage outer loop can be used as the reference signal of the inner loop of inductance current. In this capacitor voltage outer loop and inductor current inner loop control strategy, controller of inductor current inner loop is $G_i(s)$ and it is designed with PI controller; controller of capacitor voltage outer loop is $G_v(s)$ and it is made up of G_v with PI controller. The modulation of inverter bridge is $G_{inv} = v_{dc}/v_{tri}$ and it is affected by DC bus voltage V_{dc}. During the running time of the DVR, fluctuating of current and voltage is inevitable. In order to eliminate the influence of DC voltage fluctuation on the whole system, proportion link is introduced to the output side of inductor current inner loop. By doing this, the influence of DC bus voltage fluctuation on system can be eliminated effectively. By using fast voltage detection algorithm and phase locked algorithm, the voltage amplitude and phase of the PCC point are obtained. The voltage of PCC is compared with the instruction voltage V_{lref}, then we can get DVR's output command voltage $V_{DVR\text{-}ref}$ which is concluded in the first summation unit. Through capacitor voltage outer loop and inductor current inner loop, the output command voltage $V_{DVR\text{-}ref}$ can be transformed

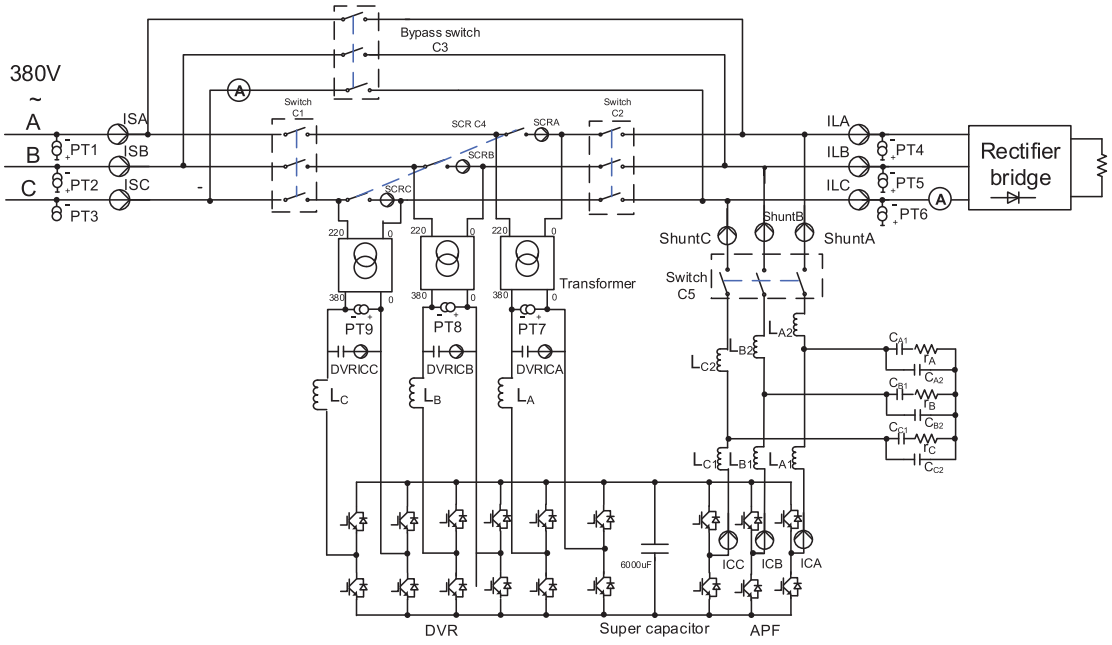


Figure 2. UPQC system.

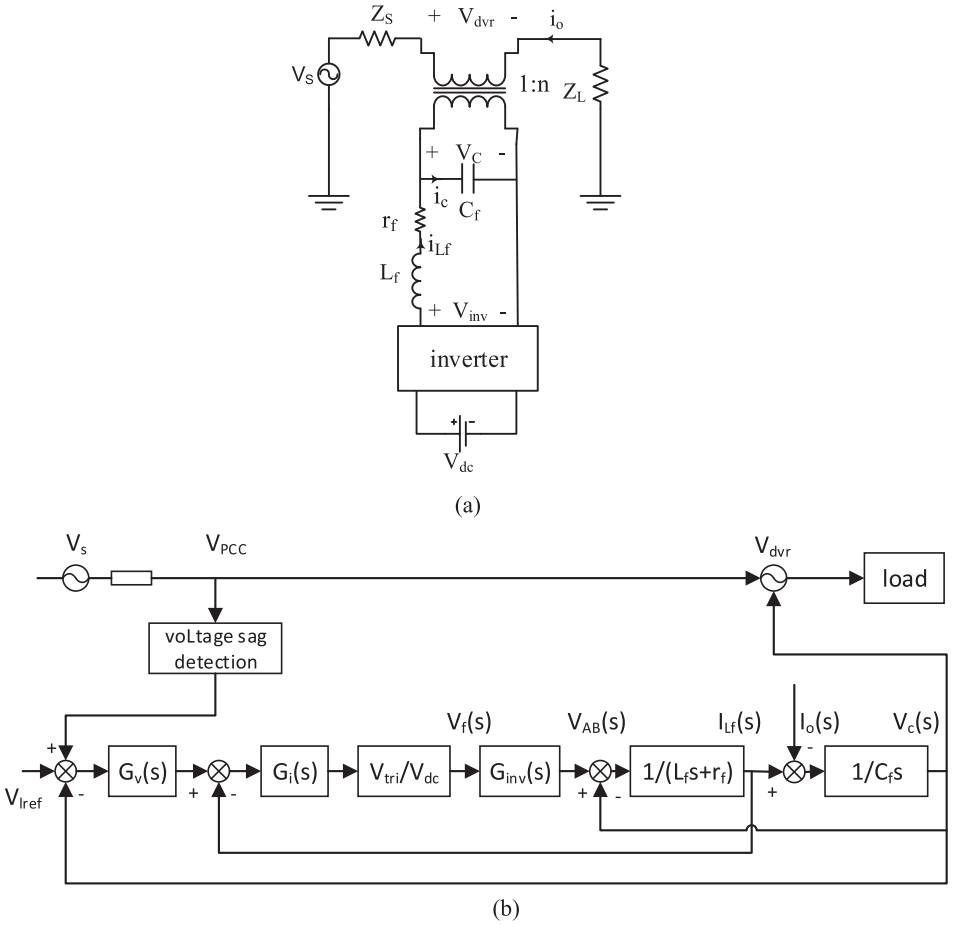


Figure 3. Double closed loop control strategy. (a) Equivalent block diagram of DVR output filter (b) Control block diagram of DVR.

to control voltage V_c, then we can get the output voltage V_{dvr}, the V_{dvr} and PCC voltage are connected on the load in series to ensure the load voltage to be a stable sinusoidal voltage.

2.2. Control algorithm of APF unit

Shunt active power filter (APF unit) should be controlled as a current source, so the compensation current generated by APF should follow the reference current as quick as possible. This is always achieved by real-time current tracking algorithm. According to the deviation between the actual compensation current and the output compensation current of the APF, control signals of PWM can be calculated out. Triangular wave comparison method is applied as main inverter control algorithm in the APF unit. As shown in Figure 4, es denotes the system voltage, $u(t)$ denotes the output voltage of inverter, i_c denotes the output current of the device, i_c^* is the command current.

3. Stability analysis of feedback-inverter-filter link

On resonance frequency, the resistance of the filter network is zero. In order to prevent the occurrence of resonance, resistance–capacitance network is applied

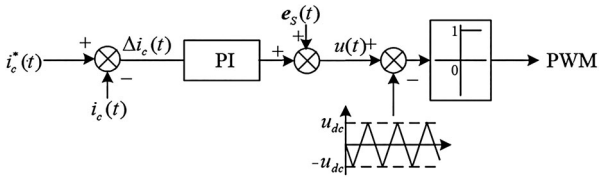


Figure 4. Triangular wave comparison method for static coordinate system with voltage feed forward.

to increase damping of resonant current. In addition, improved filter topology is applied and the switching frequency threshold range is increased. The control diagram of the designed filter is shown in Figure 5.

The mathematical model of the structure is established as is shown by formula (1), C here represents the capacitance of DC capacitor:

$$\begin{cases} (i_{\text{ref}} - i_{\text{L1}} - i_{\text{L2}}) * (k_{\text{p}} + k_{\text{i}}/s) * k_{\text{PWM}} = U_{\text{inv}} \\ (U_{\text{inv}} - i_{\text{c}} * 1/s)/L_1 s = i_{\text{L1}} \\ i_{\text{L1}} - (i_{\text{L2}} * s * L_2 - V_{\text{s}}) * s * \text{C} = i_{\text{L2}} \end{cases} \tag{1}$$

Transfer function of i_{L2} can be deduced as is shown by formula (2):

$$i_{\text{L2}} = \frac{(b_0 s + b_1) * i_{\text{ref}} + (n_0 s^3 + n_1 s^2 + n_2 s) * V_{\text{s}}}{a_0 * s^4 + a_1 * s^3 + a_2 * s^2 + a_3 * s + a_4} \tag{2}$$

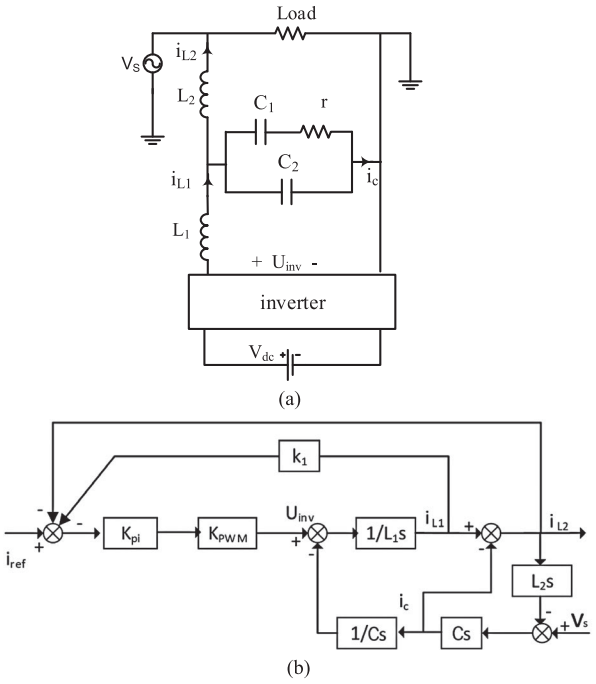


Figure 5. Equivalent block and control diagram of filter unit. (a) Equivalent block diagram of APF output filter (b) Control diagram of APF.

where

$$\begin{cases} b_0 = k_p k_{pwm}(C_1 + C_2 + R) \\ b_1 = k_i k_{pwm}(C_1 + C_2 + R) \\ n_0 = (L_1 R C_2 + L_1 C_1 C_2) \\ n_1 = (R + C_1) C_2 k_p k_{pwm} \\ n_2 = (R + C_1 + C_2 + R C_2 k_i k_{pwm} + C_1 C_2 k_i k_{pwm}) \end{cases} \tag{3}$$

$$\begin{cases} a_0 = (L_1 L_2 R c_2 + L_1 L_2 C_1 C_2) \\ a_1 = (L_2 R C_2 k_p k_{pwm} + L_2 C_1 C_2 k_p k_{pwm}) \\ a_2 = (L_1 + L_2)(C_1 + C_2 + R) \\ \quad + (C_1 + R) L_2 C_2 k_i k_{pwm}) \\ a_3 = 2(C_1 + C_2 + R) k_p k_{pwm} \\ a_4 = 2(C_1 + C_2 + R) k_i k_{pwm} \end{cases} \tag{4}$$

The system would be disturbed by V_s at runtime, under this situation, the reference current is used as input to control the output current of the filter network. Then, according to the Routh stability criterion, stability condition of the system could be deduced as formula (5)

$$L_1 < L_2 * \left[1 + \frac{(C_1 + R) C_2 k_i k_{pwm}}{(C_1 + C_2 + R)} \right] \tag{5}$$

Based on the above analysis, LCL topology is applied to the system where L_1, L_2, C_1, C_2 are parameters of inductors and capacitances. Details of parameter design are shown in Table 1 (more details are provided in Appendix A):

Amplitude frequency characteristic and phase frequency characteristic curve of the transfer function for

Table 1. Parameters of the LCL model.

Categories	Values
Inductance of inverter side L_1	0.8 mH
Inductance on the grid side L_2	0.2 mH
Compensation capacitor C_1	2.5 μF
Compensation capacitor C_2	2.5 μF
Filter resistance R	2 Ω
Proportionality coefficient k_p	2
Integral coefficient k_i	0.1
PWM Ratio k_{PWM}	1

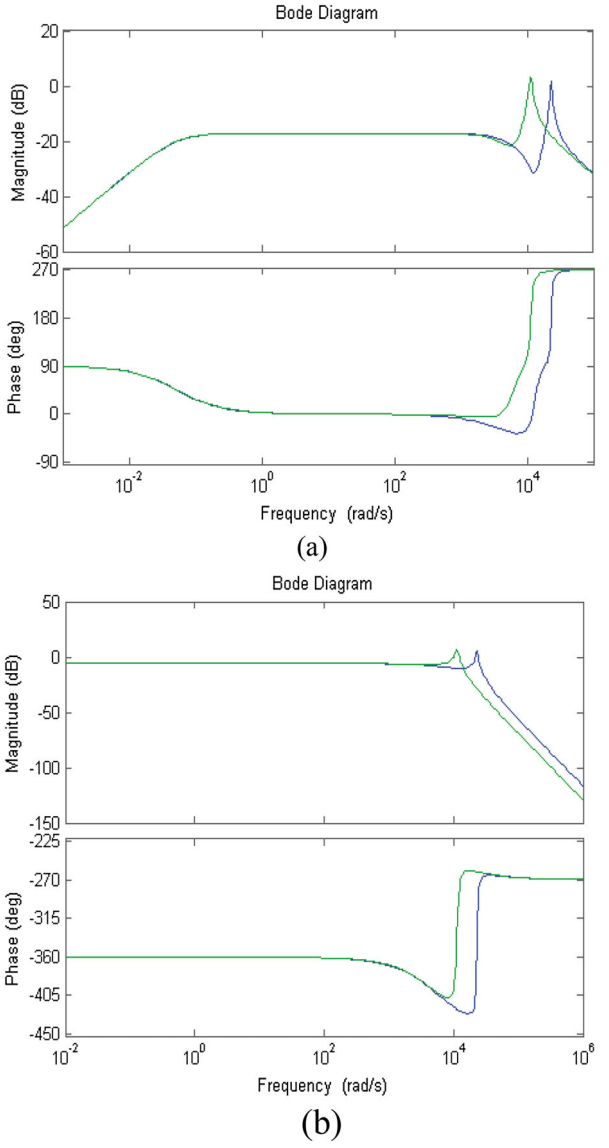


Figure 6. Frequency characteristic of the compensation filter. a). ordinary filter vs. compensation filter (input item is reference current, output item is output current) b). ordinary filter vs. compensation filter (input item is system voltage, output item is output current).

output current versus reference current is shown in Figure 6(a). One of the tasks of APF is filtering harmonic current generated by high frequency switching. It can be seen that the two stage enhancement filter has better harmonic attenuation effect, and it can increase the ability of restraining high order harmonics to a certain extent.

Amplitude frequency characteristic and phase frequency characteristic curve of the transfer function for output current versus system voltage is shown in Figure 6(b). Under this situation, APF restrains the disturbance from system voltage on output current. It can be seen that by using compensated LCL filter circuit topology, the suppression of the system voltage disturbance does not decrease, there is still the attenuation characteristic of −20 db at switched off frequency. The anti-jamming capacity for high frequency is enhanced.

4. Simulation and experiments of the system

4.1. Simulation of APF filter

1) Filtering characteristics simulation

The simulation of the designed filter shows its effectiveness on filtering primary odd harmonics. Current waves of load after the designed filter are shown in Figure 7, which shows that the filtering effect of the enhanced LCL filter(right figure) is better than that of the ordinary filter (left figure), the filtering effect of 5 times, 7 times,11 times, 13 times and 17 times harmonic are enhanced obviously. The left figure shows the filtering result of ordinary filter while the right figure shows the filtering result of the designed LCL filter. Different line shows nth harmonic where n is in range of 5, 7, 11, 13, 17, the amplitude of total harmonics is obviously reduced from 0.4% to 0.15%.

2) Harmonic suppression simulation

Harmonic compensating simulation is carried out in PSCAD. The time domain diagram of load current, harmonic compensation current and system side current is shown in Figure 8(a)–(c). Compensating of reactive power is shown in Figure 8(b).

In Figure 8(a)–(c), I_{La} represents load current, I_{ref} represents harmonic compensating current, I_{Sa} represents system current after compensation. In (a), at the time point 1.25 s in time domain, frequency analysis is carried out respectively for load side current (I_{La}), compensation current (I_{ref}) and system side current (I_{Sa}). I_{La} has obvious wave distortion and after harmonic compensating, the system current (as is shown by curve I_{Sa}) is improved obviously, the harmonic component is reduced significantly.

In Figure 8(c), the blue, red and green bars respectively represent the ratio of harmonic in load current, reference current and system current. It is obvious that harmonic components in systems are supressed effectively.

In Figure 8(b), Q_L represents the reactive power absorbed by load, Q_S represents the reactive power flowing into the system. After APF is applied in 0.1 s, Q_S is reduced by two stages which shows that the designed APF can effectively compensate reactive power for the system.

4.2. Experiment of APF

1) Current tracking experiment

The experiment setup for current tracking experiment is shown in Figure 9. The value of load resistance is 38 Ω, value of DC capacitor is 6800 μf, value of reactor is 10.6 mH, the load resistance is in form of delta connection. This part of the experimental device should only be used to test the performance of current tracking algorithm. So it is not a complete UPQC. Only one three-phase full-bridge inverter with passive load is used. Its DC side capacitance voltage is supplied by three-phase uncontrolled rectifier bridge. The input AC voltage of three-phase uncontrolled rectifier bridge is controlled by three-phase autotransformer (Continuous change from 0 to 380 V). During the experiment, the inverter bridge is controlled as a controlled current source. Track the given instruction current signal, where the instruction current signal is given.

In Figure 10(a), the yellow curve represents the open loop voltage waveform on the resistor, and the blue curve represents the current waveform while the DC voltage is set 80 V; in Figure 10(b), the yellow curve is the closed loop voltage waveform on the resistor, and the blue curve is the current waveform while the DC voltage is 160 V. In the experiment, reference current to track is set to 1 A. As shown in (b), voltage on load resistance is 25.7 V which shows that the designed APF is able to track 1 A current.

2) Harmonic detection and compensation experiment

The experiment setup for current tracking experiment is shown in Figure 11.

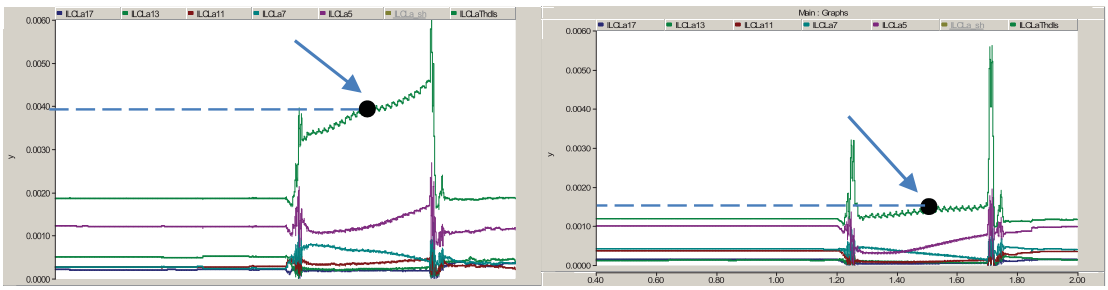


Figure 7. Filtering characteristics comparison between LCL and LC filters.

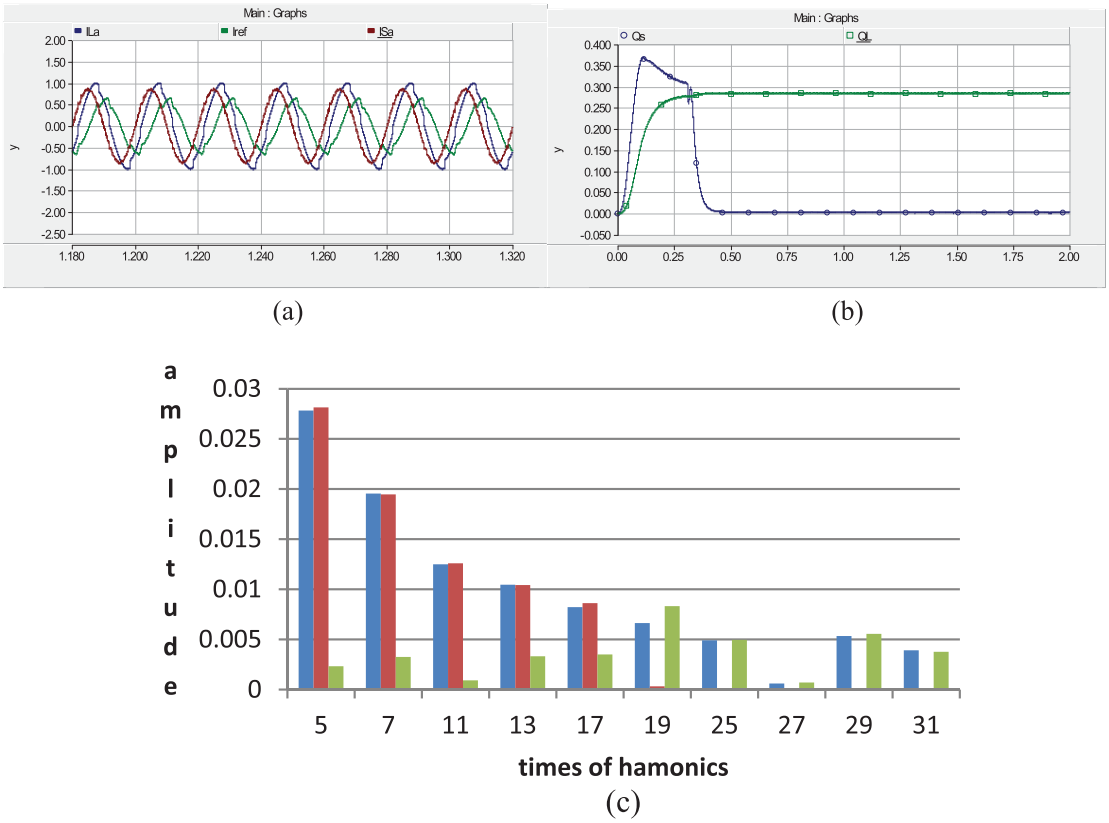


Figure 8. Simulation results of harmonic current compensation. (a) Current waves (b) Reactive power compensation (c) comparision of harmonic component in between load current, reference current and system current.

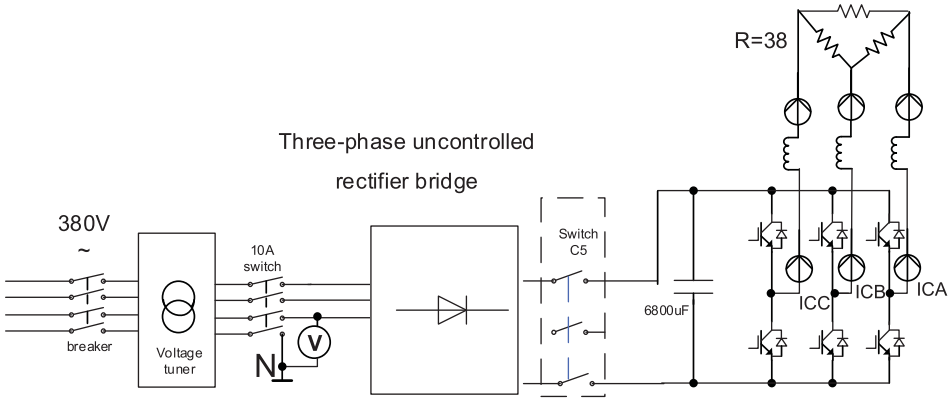


Figure 9. Experiment setup for current tracking test.

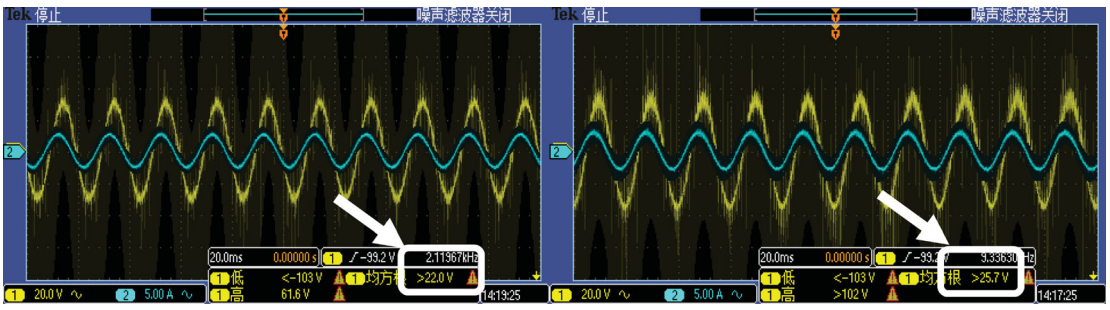


Figure 10. Result of current tracking experiment. (a). Open loop test, load voltage 22V (b). Closed loop test, load voltage25.7V.

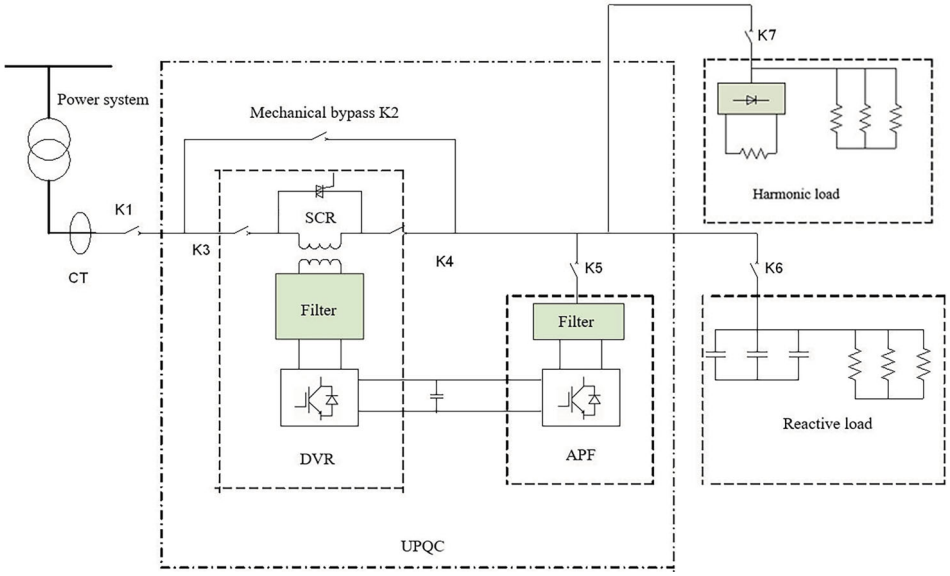


Figure 11. APF experiment setup for reactive power compensation test and harmonics compensation test.

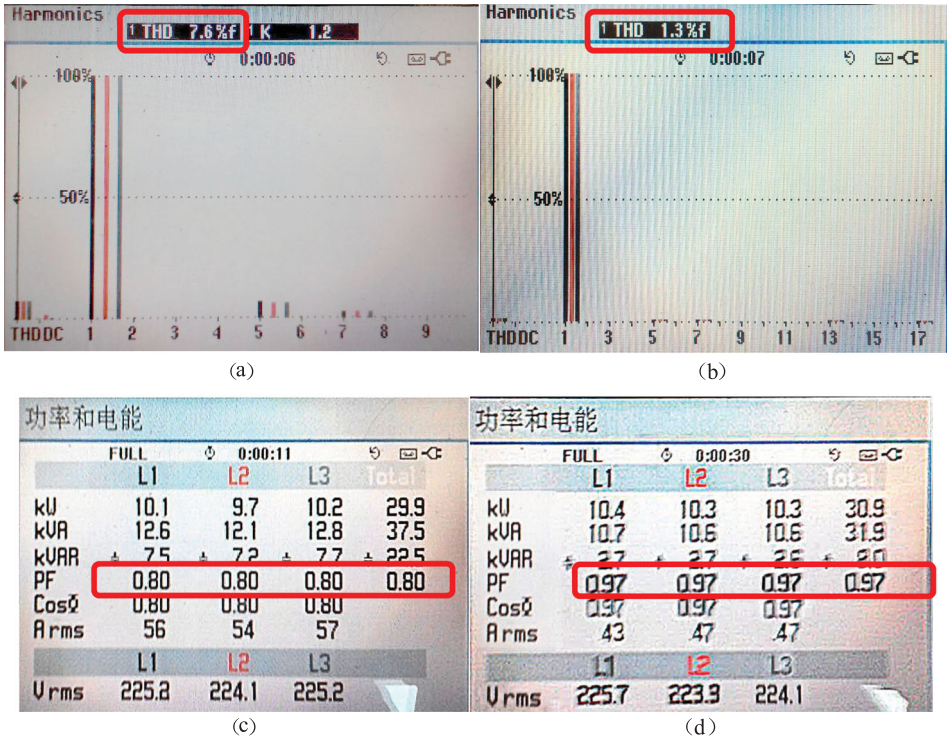


Figure 12. Current and reactive power compensation result on FLUKE analyser. (a) harmonics before APF switched in (b) PF before APF switched in (c) harmonics After APF switched in (d) PF after APF switched in

APF compensation is carried out according to harmonic frequency. Figure 12 shows the compensation results of reactive power compensation and harmonic compensation.

In Figure 12, (a) shows the harmonics analysis result before APF is switched in. (b) shows the improved system testing result after APF is switched in. (c) shows the reactive power analysis result before APF is switched in. (d) shows the improved power factor after APF is switched in. It can be seen that the compensation effect of 5th and 7th harmonic is obvious. Total THD is improved from 7.6% to 1.3%. Power factor is improved from 0.8 to 0.97. The detection and compensating algorithm works well.

4.3. Voltage sag compensation simulation for DVR

The simulation of voltage sag and compensation results of the designed system is shown in Figure 13. The voltage sag for detection test was designed to last 1.2 s, drop depth is set to 50% grid voltage.

From the compensation effect diagram in Figure 13, it can be seen that by using the capacitor voltage outer

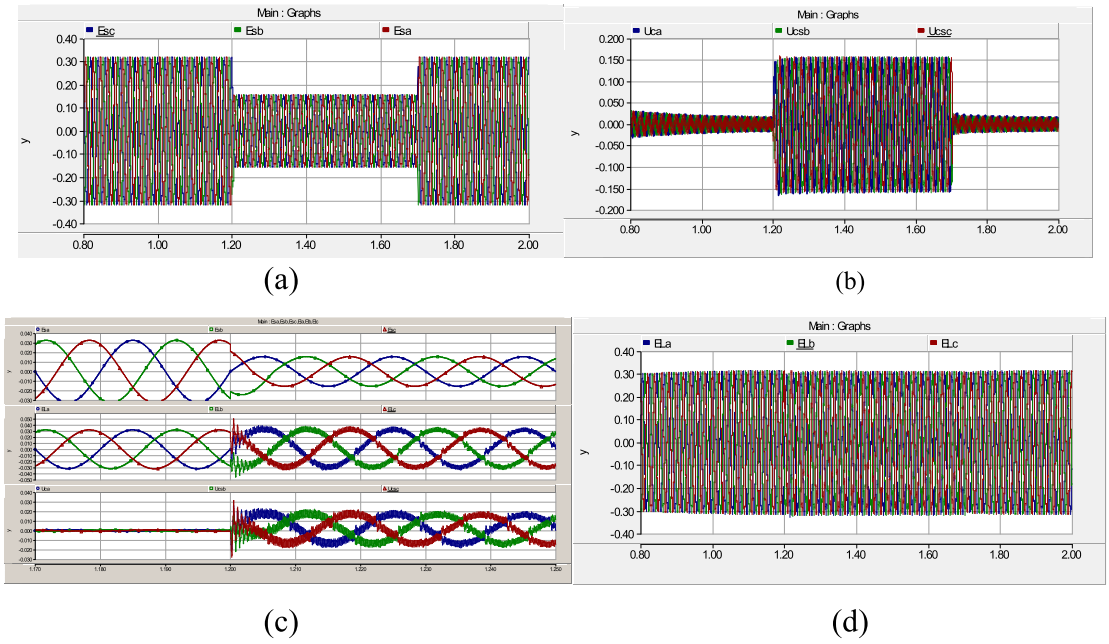


Figure 13. Waveform of voltage sag, compensation voltage and compensated system voltage. (a) voltage sag appears (b) compensating voltage output (c) details of voltage sag (d) compensated system voltage.

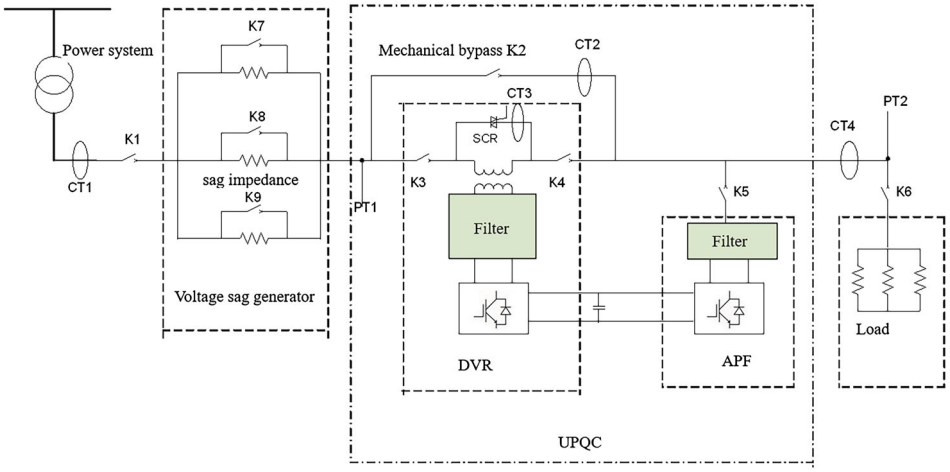


Figure 14. Schematic diagram of DVR compensation experiment.

loop and inductor current inner loop control strategy, the output voltage can track the instruction signal accurately and rapidly. The dynamic and steady-state performance of DVR system is improved, the dynamic response speed is improved and the steady-state error of the system is reduced obviously. The designed DVR can meet the output characteristics requirement of most sensitive loads.

4.4. DVR experiments

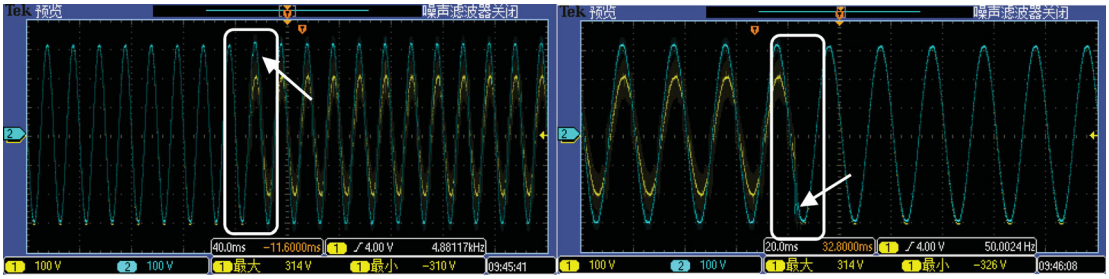
The experimental setup of DVR is shown in Figure 14.

1) Single phase voltage drop compensation experiment

Single phase and double phase voltage sag experiments were carried out. The single phase voltage compensation experiment is shown in Figure 15. The yellow line shows A phase voltage, blue line shows the system voltage. In (a), A phase voltage (yellow wave) sag appears as is pointed out by rounded rectangle, at the same time, the load voltage wave (blue wave) goes almost unaffected due to DVR's series compensation voltage. (b) shows A phase voltage's recovery and load voltage still goes almost unaffected. It shows that the DVR output is switched out smoothly instead of over compensation.

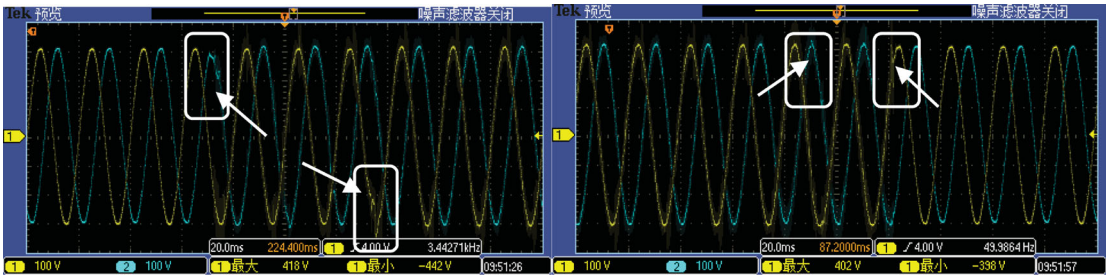
2) Two phase voltage drop compensation experiment

Furthermore, A–B phase voltage sag experiment was carried out. In Figure 16, the yellow waves show load voltage of A phase; the blue waves show load voltage of B phase. In (a), when phase voltage sag appears, compensated load voltage (with wave distortion) is captured as is respectively pointed out by the two rounded rectangle. So, the compensation of two phase voltage



(a) (b)

Figure 15. Single phase voltage drop compensation experiment. (a) Voltage sag happens and DVR switched in (b) Compensation and DVR switched out.



(a) (b)

Figure 16. Two phase voltage drop compensation experiment. (a) Voltage sag happens and DVR switched in (b) Compensation and DVR switched out.

sags is realized although there was a slight distortion. (b) shows the A phase and B phase voltage's recovery and loads' voltage still keep almost unaffected. It shows that the DVR output is switched out smoothly instead of over compensation in two phase voltage sag compensation process.

If depth of sag is acceptable or magnetizing inrush current is controlled well or using an anti-inrush transformer, the DVR's start up delay would be controlled to very short time which is no more than 2 ms.

5. Conclusion

Double loop control algorithm and experiment design for UPQC are introduced. The simulation of compensation strategy for voltage sag and harmonic current is provided by which the effectiveness of the double loop strategy is proved. Harmonic suppression and voltage sag compensation simulation are provided and furthermore, to testify the correctness of the designed system, harmonic compensation experiment, single phase voltage drop experiment and two phase voltage drop compensation experiment are provided in detail. Experimental results prove the validity and correctness of the method and theory provided in this paper.

Disclosure statement

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Appendix A

The design methods of output filters for DVR and APF are different. First, DVR does not compensate for harmonics. Therefore, its cut-off frequency is lower. APF output filters need to output harmonics. The cut-off frequency is relatively high and more difficult to design. In addition, APF is connected to the system in parallel. So seen from the output port of APF, the system impedance and load impedance are parallel. Because the system impedance is very small. So the final equivalent impedance is approximately equal to the system impedance. DVR is connected in series. So, seen from the output port of DVR, the system impedance and load impedance are in series. So the equivalent total impedance is a large load impedance. This also makes it easier to design the output filter. In addition, DVR is coupled through transformers. Therefore, the inductance near the load side in the LCL output filter can be replaced by the leakage reactance of the coupling transformer.

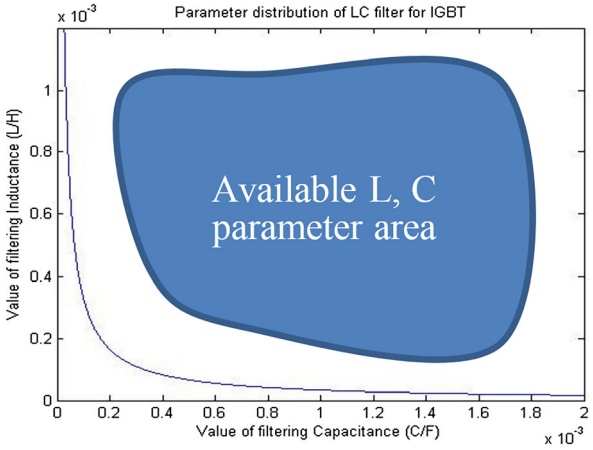

Figure A1. Area of available LC parameters which meet harmonic content criteria.

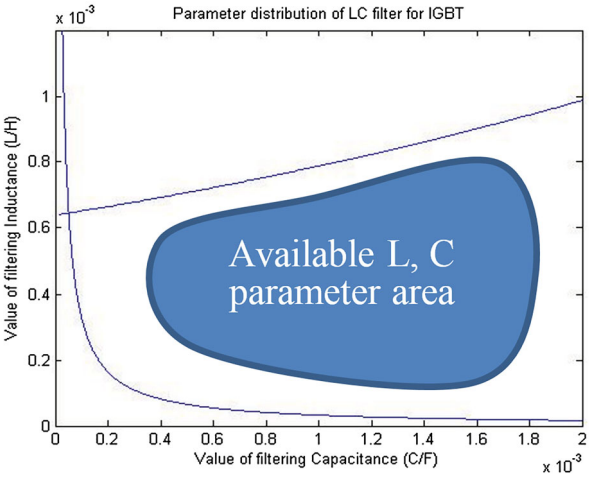

Figure A2. Area of available LC parameters which meet voltage gain criteria.

The parameters of output filter in APF and DVR were calculated according to references and adjusted and determined according to PSCAD simulation and experiment results finally. Many papers have studied passive damped output filter topology in theory, and most results are applicable under specific conditions (that's what it should be because filter should be designed for specific application situation to achieve optimum filtering effect), we have calculated filter parameters in our topology according to the published methods as is shown below and ideal values can be calculated. But at last, we should still do verification in PSCAD simulation and adjust some of these parameters. So we choose parameters by building UPQC model in PSCAD which includes almost all details of the system, and through the simulation, satisfactory results have been achieved.

The parameters of the filter in UPQC were calculated according to [20], and the part of the calculation and deduction according to our designed system is as follows.

According to the formula [20]:

$$\mathrm{HF}_0(2\omega_s - \omega_0) = \frac{2}{\pi b} * \frac{1}{|N^2\beta - 1|} * J_1(a\pi) \leq \mathrm{HF}_0 \quad \text{(A1)}$$

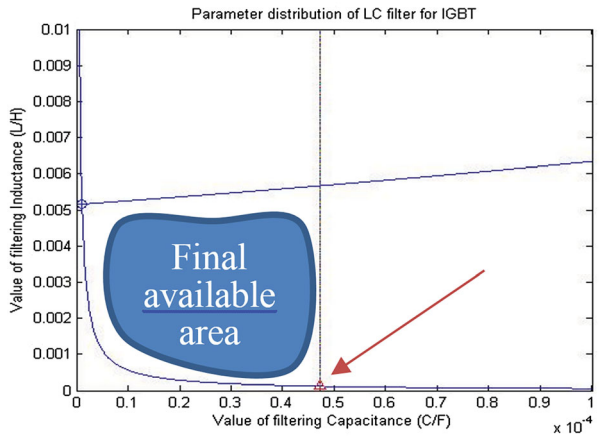

Figure A3. Area of available LC parameters which meet no-load current criteria.

where

$$\begin{cases} \mathrm{HF}_0 = 0.05 \text{ (Harmonic content index of output voltage)} \\ \omega_0 = 2\pi f_0, f_0 = 50\,\mathrm{Hz}\ (f_0 : \text{fundamental frequency}) \\ \omega_s = 2\pi f_s, f_s = 10\,\mathrm{kHz}\ (f_s : \text{sampling frequency}) \\ \beta_0 = {\omega_0}^2 LC = 1/N^2 \\ N = (2f_s - f_0)\, f = 199 \\ b = \sqrt{2}U_0\ E_{\max} = \sqrt{2} * 566/(800 * 1.05 * 1.25) = 0.7622 \\ a = b|1-\beta| \end{cases} \tag{A2}$$

we could find β_0 by (the mentioned b_0 is this β_0)

$$\begin{cases} \mathrm{HF}_0(2\omega_s - \omega_0) = \dfrac{2}{\pi b} * \dfrac{1}{N^2\beta - 1} * \\ J_1(a\pi) \le \mathrm{HF}_0 = 0.05 \\ \dfrac{2}{3.14 * 0.7622} * \dfrac{1}{199^2\beta - 1} * \\ J_1(0.7622 * |1-\beta| * 3.14) = 0.05 \end{cases} \tag{A3}$$

Then $\beta_0 = 0.000554$, accordint to the formula $\beta_0 = {\omega_0}^2 LC$, relation of L and C can be plot as Figure 2-1, this is critical curve of harmonic content index. The right-hand area of the curve in the graph satisfies harmonic content index of output voltage.

The red triangle shows the final selected parameter of L and C according to the following formula:

$$\begin{cases} C_{\text{find}} = C_{\max} \\ L_{\text{find}} = \dfrac{\beta_0}{\omega^2 C_{\text{find}}} \end{cases} \tag{A4}$$

where β_0 was calculated before, in our experiment situation, its value is 0.000554.