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Original scientific paper

A Flexible Rung Ladder Structured Multilevel Inverter

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Abstract: The tenet of the multilevel inverter (MLI) is a peculiar kind in the voltage source inverter (VSI) family, which offers a prudent solution to prevailing issues of conventional two levels VSI, higher d*v*/d*t* and harmonic distortion, through a staircase/stepped output voltage from multiple separate dc sources (SDCs). The incessant research effort in the last four decades has bestowed a host of MLI topologies with different concepts, structures, component requirements and application appropriateness. The main issue with the MLI structures is the objectionable component count while upping the number of levels in the output staircase waveform. This paper suggests a new MLI structure, a flexible rung ladder structured multilevel inverter (FRLSMLI), with a savvy to operate both in symmetrical and asymmetrical modes involving only fewer component counts. The proposed FRLSMLI is basically a ladder structured bridge (H-bridge with additional rungs) and the rungs comprise either source inclusion-bypass cell (SIBC) or four level creator cell (FLCC). The FRLSMLI can synthesize fifteen levels with three SDCs. The simulation and experimental results are projected to validate the viability of proposed MLI in real time applications.

Keywords: flexible rung ladder structured MLI; source inclusion-bypass cell; tenet multilevel inverter

1 INTRODUCTION

The multilevel inverter (MLI) is a breed of voltage source inverter (VSI), which can synthesize a high quality ac output voltage of required frequency from multiple separate dc sources (SDCs) [1-3]. The MLIs strikingly outperform the conventional two level inverters (TLIs) with the apparent merits such as lower d*v*/d*t* and device stress, a waned output distortion, minimal switching losses, a gagged electro-magnetic interference (EMI), a low common mode voltage and an ability to operate at higher voltage [4-6]. Since its supersession in 1975, many topologies have been readied, which are bizarre in topology, tenet, number of components etc. [7-9]. In the wake of above facts, the MLI has become an amenable solution to prevailing issues of the two level inverter [10-11], through which the integration of SDCs like batteries, super capacitors and solar panels has become doable. The evolution of the MLI family started when its first pristine structure, series connection/addition of H-bridges, was introduced by R. H. Baker [12]. As a sequel, in 1980, Nabae A et.al. introduced neutral point clamped (NPC) inverter, which is five level version of the diode clamped MLI [13]. The diode clamped MLI structure employs a specified number ((*m*−1)/2, where, *m* is the number of levels) of capacitors to split the single dc voltage source, while the clamping is eventually triumphed by the diodes. This topology curtails the voltage across individual devices with the help of diodes. The successor, capacitor clamped MLI (which is also called flying capacitor), replaced the diodes by floating capacitors [14]. After thirteen years, Gui-Jia Su has suggested an innovative idea of engraving the stair case ac output in dual stage, namely, a first stage to synthesize multilevel dc (a pulsating dc which could result if MLI output is fed to a diode rectifier) and a second stage to fold into ac (conventional H-bridge inverter). Gui-Jia Su has exploited all the three earlier MLI structures and designed three structures of multilevel dc link MLI, respectively [7]. Hitherto, many such proposals have been reported in this ambit [15-18].

A modified cascaded MLI topology to produce a high number of output steps with fewer switches has been indicated [19]. Additionally, formulaic steps to compute the SDC values have been suggested. A switch sharing strategy has been the crux tenet in the suggestion given by Hew Wooi Ping et al. [20]. It has been demonstrated successfully that a considerable reduction in switch count is possible in the switch sharing. In a dual boost MLI structure, which is a perfect juxtaposition of the L-Z source inverter and the switched capacitor MLI, the first stage of boosting is performed by an impedance network and the second stage is through switched capacitor [21]. J.Venkataramanaiaha et al. have categorized the MLI structures into four clusters, viz. symmetric, asymmetric, hybrid and single dc source topologies [22]. The main drawback of two stage switched capacitor based MLI, higher stress in the second stage devices, has been resolved in the single stage switched capacitor module (S3CM) topology [23]. The S3CM structure asserts the peak inverse voltage (PIV) across all the switches lesser than dc source value.

A topology for reduction of both switching losses and voltage stress has been coined [24], with a voltage balancing tactic. The suggested symmetrical sub-module based MLI, the hybrid cascaded MLI, is the amalgamation of 'n' sub-modules and the H-bridge [25]. A comprehensive comparative study revealed that this topology demands lesser number of components.

Regrettably, even the MLI has few issues. The first one is the requirement of higher number of component count, in particular, more numbers of power semiconductor switches. Despite the fact that the individual switch rating is lesser than in the case of TLIs, the increase in the count also increases the associated gate drivers. Another noticeable issue is number of active devices in the conduction path, which can deduce both the output voltage and increase the conduction losses. This paper develops a MLI structure with dual mode capability (both symmetrical and asymmetrical modes), which paves the solution to the above mentioned problems. The suggested flexible rung ladder structured multilevel inverter (FRLSMLI) is the extended H-bridge structure, wherein special kind of cells are connected in place of the load and hence forms the ladder shape. The rung can include either source inclusion and bypass cell (SIBC) or four level creator cell (FLCC). A rigorous MATLAB R2017b based simulation study is performed for both symmetrical and asymmetrical modes. The result of simulation study is validated in the laboratory prototype supported by field programmable gate array (FPGA) processor.

2 PROPOSED TOPOLOGY

The generalized structure of the proposed topology pictured in Fig. 1 comprises voltage modules/cells, SIBC and FLCC, which are arranged in rungs of the ladder structure. The ladder structure is resulted while extending the conventional H-bridge with supplementary rungs. The inventive cells are placed in positions of the load that is between two vertical arms. The FLCC contains two SDCs (V_1 and V_2), which can create four different dc levels (V_1, V_2, (V_1 + V_2) and (V_1 ~ V_2)). S_1 and S_2 are cascading switches while S_1' and S_2' are bypassing switches. S_r is the reverse connector switch, which is responsible for the last level (V_1 ~ V_2) and hence acts as a subtraction facilitator. That is, the S_r is a bidirectional switch used to subtract the voltage source (V_2) from (V_1). The SIBC is a simple cell having one source, where S_3 is the cascading switch and S_3' is the bypassing switch. Required number of these cells can be subsumed to attain desired number of voltage levels (m). Fig. 2 to Fig. 8 illustrate the operating modes to extract various levels of the output voltage. For the sake of easy understanding, the asymmetrical combination of SDCs values may be considered as V_1:V_2:V_3 = 1:3:3 =1 00 V:300 V:300 V. Fig. 2 depicts the path for obtaining 100 V. Similarly Fig. 3 shows the switching combination for 200 V, which is actually feasible by two ways, either ±(V_2−V_1) or ±(V_3−V_1). The mode diagrams and the different options in achieving certain level are understood by referring to respective figures. Thus with the three SDCs 15 level output is obtained.

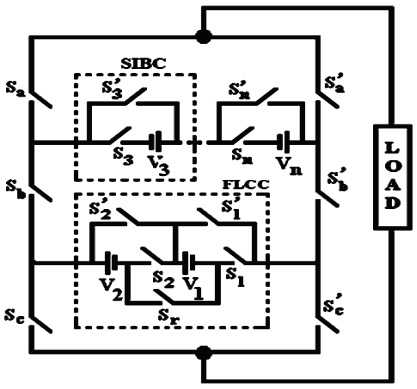

Figure 1 Generalized structure of proposed topology

The clue to the required number of SIBC and FLCC will be more useful. A topology with l number of FLCC will offer a number of voltage levels (m) as (3 × ((4 × l) − 1); a topology with k number of SIBC can offer ((4 × k) − 1) output levels; and a topology with both 'l' number of FLCC and k number of SIBC will give (6 × ((2 × l) + k) − 3) levels. The representative asymmetrical topology, with l = 1 and k = 1, discussed above can offer (6 × ((2 × 1) + 1) − 3) = (6 × (2 + 1) − 3) = (6 × 3 − 3) = 15 levels. Fig. 9 shows a single rung ladder MLI (SRLMLI), which is constituted using either of SIBC and FLCC or both. Using this SRLMLI any number of levels in the output voltage can be obtained. The SRLMLI can be treated as a basic cell to formulate higher levels. A structure involving 0 z number of SRLMLI can generate, m = ((2 (z + 1) − 1) if FLCC alone is used while m = (9 × z) if SIBC is used, where respective switch count will be (6 × z) and (9 × z).

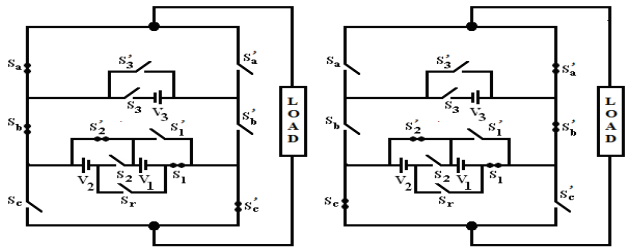

Figure 2 Operating mode: ±V_1

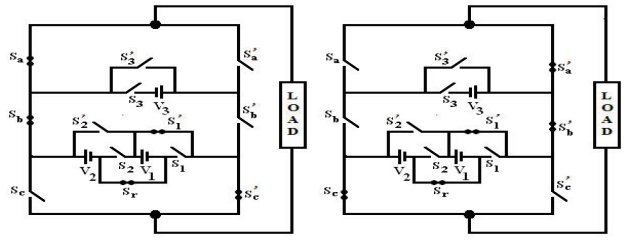

Figure 3 Operating mode: ±(V_2 − V_1)

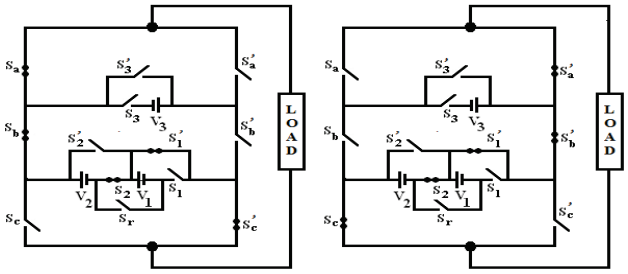

Figure 4 Operating mode: ±(V_2)

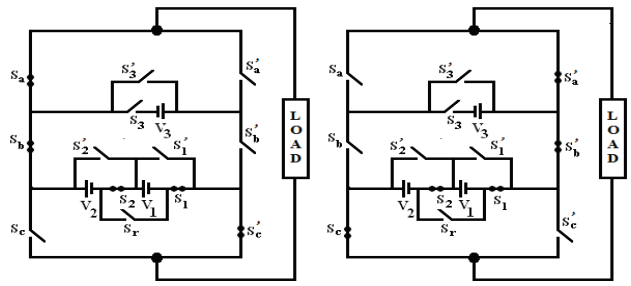

Figure 5 Operating mode: ±(V_1 + V_2)

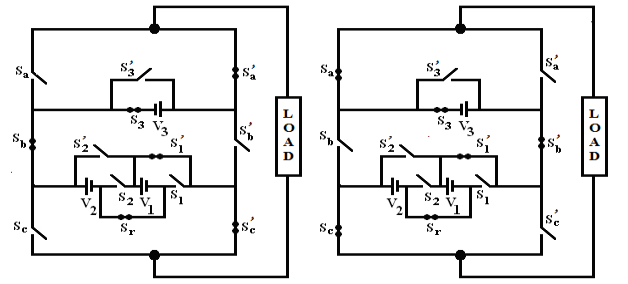

Figure 6 Operating mode: ±(V_2 + V_3 − V_1)

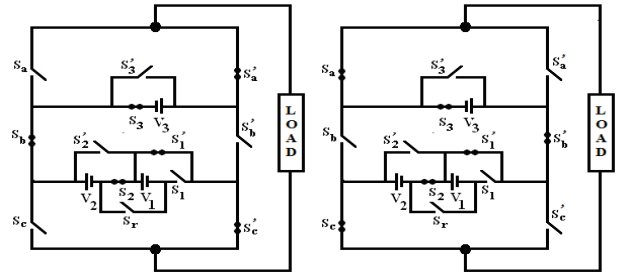

Figure 7 Operating mode: ±(V_2 + V_3)

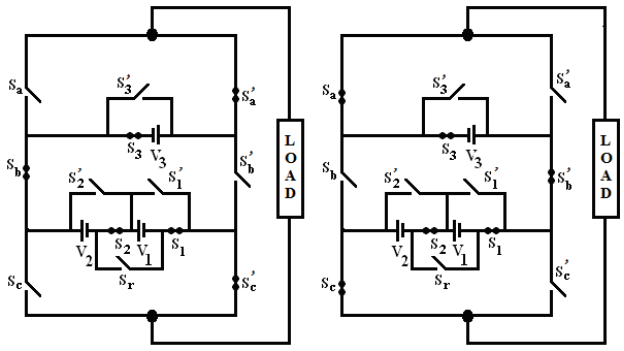

Figure 8 Operating mode: ± ($V_1 + V_2 + V_3$)

Tab. 1 enlists the comparison between the proposed and prevailing topologies while operating in symmetrical mode at m level. Tab. 2 explains the relation between number of DC sources (n) in SRLMLI, number of SRIMLI if SIBC is used. Akin to that when FLCC is used the relations are listed in Tab. 3.

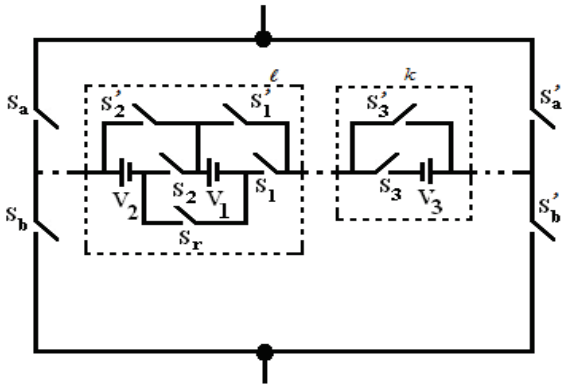

Figure 9 Single rung ladder MLI

Table 1 Comparison of FRLSMLI and existing MLI topologies

MLI Structure / Components	Cascaded H-bridge	Diode clamped	Flying Capacitor	Series parallel switched MLDCLI [26]	FRLSMLI	
					FLCC	SIBC
Main switches	$2(m-1)$	$2(m-1)$	$2(m-1)$	$(3m-1)/2$	$(5m+11)/4$	$(m+5)$
Bypass diodes	-	-	-	1	-	-
Clamping diodes	-	$2(m-3)$	-	-	-	-
DC split capacitors	-	$(m-1)/2$	-	-	-	-
Clamping capacitors	-	-	$(2m-6)/2$	-	-	-
DC sources	$(m-1)/2$	1	1	$(m-1)/2$	$(m-1)/2$	$(m-1)/2$

Table 2 Key relations of FRLSMLI when SIBC used

Parameters	Symmetrical	Asymmetrical	
		Binary 1:2:4:8:16	Geometric sequence with common ratio 2 1:2, 4 8 16,
Peak output voltage	$V_{dc} \times (3 \times z)$	$V_{dc} \times (((6 \times z) - 1)$	$V_{dc} \times (2\,(3 \times z) - 1)$
Number of voltage levels	$((6 \times z) + 1)$	$((12 \times z) - 1)$	$(2\,((3 \times z) + 1) - 1)$
Number of SDCs and capacitors	$(3 \times z)$	$(3 \times z)$	$(3 \times z)$
Number of switches and gate drivers	$(10 \times z)$	$(10 \times z)$	$(10 \times z)$
Standing voltages on all switches in the supplementary inverter	$3 \times V_{dc}$	$(5 \times V_{dc})$ for $z = 1$ $(6 \times V_{dc})$ for $z > 1$	$(7 \times 8\,(z-1))V_{dc}$

Table 3 Key relations of FRLSMLI when FLCC used

Parameters	Symmetrical	Asymmetrical	
		Binary	Geometric sequence with common ratio 3
Peak output voltage	$V_{dc} \times (2 \times z)$	$V_{dc} \times (((4 \times z) - 1)$	$V_{dc} \times (((9 \times z) - 1)/2)$
Number of voltage levels	$((4 \times z) + 1)$	$((8 \times z) - 1)$	$(9 \times z)$
Number of SDCs and capacitors	$(2 \times z)$	$(2 \times z)$	$(2 \times z)$
Number of switches and gate drivers	$(9 \times z)$	$(9 \times z)$	$(9 \times z)$
Standing voltages on all switches in the supplementary inverter	$2 \times V_{dc}$	$(3 \times V_{dc})$ for $z = 1$ $(4 \times V_{dc})$ for $z > 1$	$(4 \times 9(z-1))V_{dc}$

3 SIMULATION AND EXPERIMENTAL INVESTIGATIONS

For understanding the functioning of the suggested MLI in symmetric and asymmetric modes, a detailed simulation study is carried out in MATLAB R2017b. The simulation parameters are as follows, $V_1 = V_2 = 150$ V for symmetrical ($2 - k$); $V_1 = 43$ V, $V_2 = 86$ V, $V_3 = 172$ V (for 1:2:4 ratio) and $V_1 = 23$V, $V_2 = 69$ V, $V_3 = 207$ V (for 1:3:9 ratio) for asymmetrical modes with binary and ternary schemes respectively, to produce 300 V (peak) in the output voltage. Values of the RL load used in simulation study is $R = 100\ \Omega$ and $L = 100$ mH. The switching frequency is 2 kHz [27-29]. Fig. 10, Fig. 11 and Fig. 12 depict output voltage waveform for symmetric and asymmetric configurations of the proposed topology. Fig. 13 and Fig. 14 charter output voltage spectra and inductive load current waveform for asymmetrical configuration. The simulation results evidence that the proposed topology is capable of giving high number of voltage levels with a minimum number of power components [30-32].

The proposed topology is experimentally tested for both symmetrical and asymmetric operations with an identical simulation specification. The experimental setup makes use of Xilinx Spartan 3E FG 320 FPGA controller for generating gating pulses to trigger the switches to synthesize five levels in the output voltage. Fig. 15 and Fig. 16 represent the output voltage waveform for symmetric and asymmetric conditions. Fig. 17 illustrates the inductive load current waveform for the asymmetrical configuration. It is evident from Fig. 15 and Fig. 16 that the proposed topology works well for both operating conditions/ configurations.

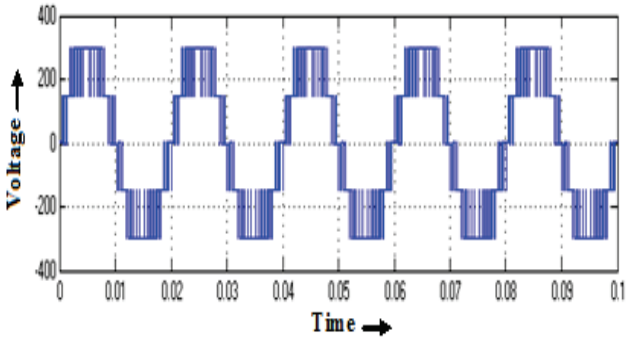

Figure 10 Output voltage waveform- symmetrical configuration

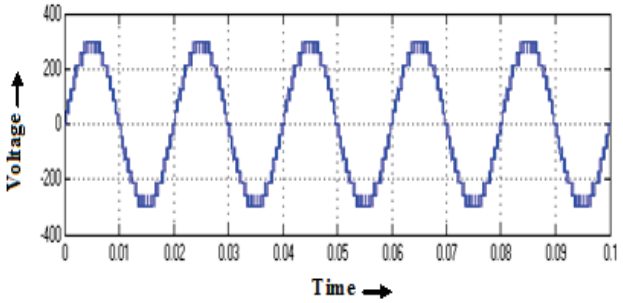

Figure 11 Output voltage waveform - asymmetrical configuration with binary voltage ratio

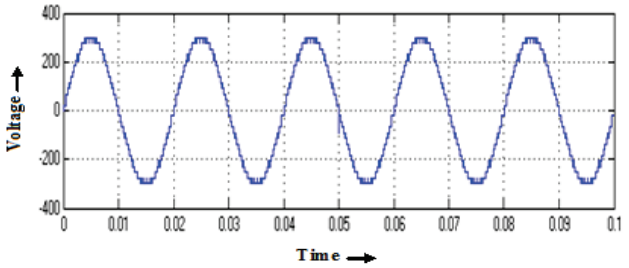

Figure 12 Output voltage waveform - asymmetrical configuration with ternary voltage ratio

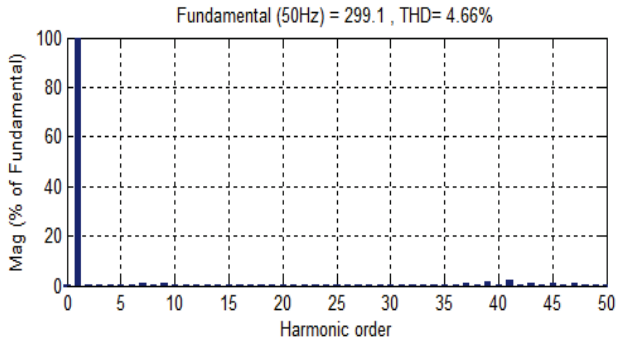

Figure 13 Harmonic spectrum of output voltage-Asymmetrical configuration (ternary ratio)

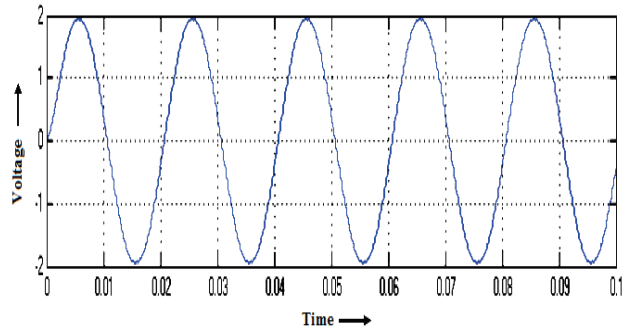

Figure 14 Inductive load current waveform

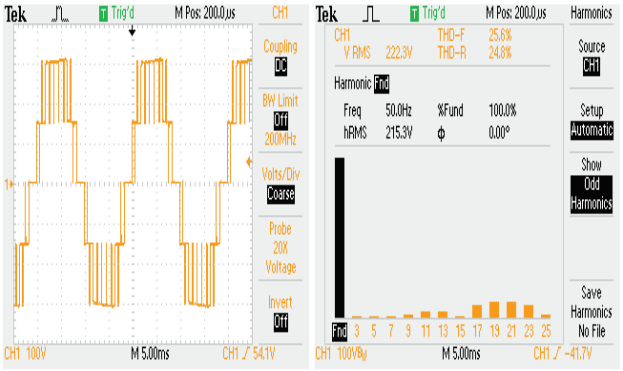

Figure 15 Output voltage waveform with harmonic spectrum for symmetric configuration

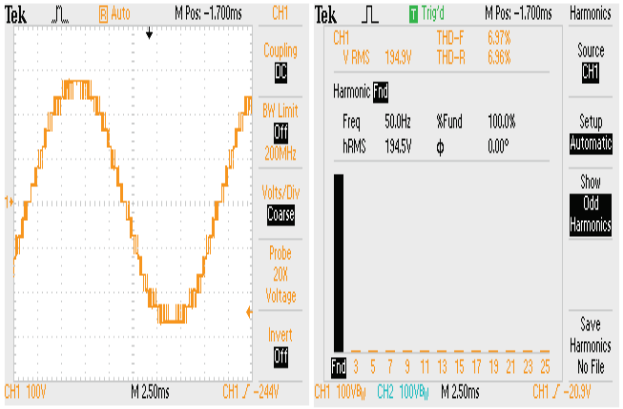

Figure 16 Output voltage waveform with harmonic spectrum for asymmetric configuration

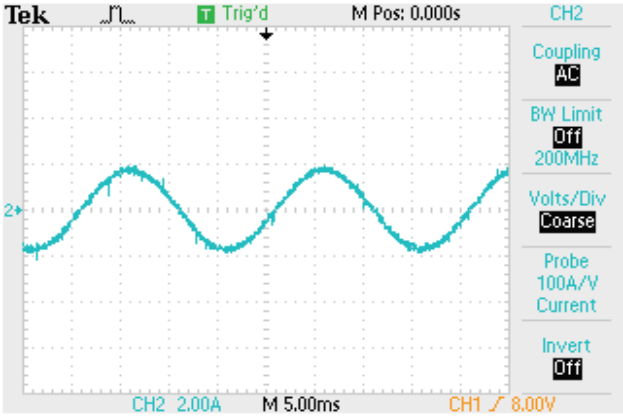

Figure 17 Inductive load current waveform

4 CONCLUSION

A new topology in the cascaded breed of the multilevel inverter (MLI) is developed with a view to offer a reduced number of devices in the conduction path while increasing the number of voltage levels. Authors could successfully explore the control degree of freedom available in the MLI structure and suggest an extended H-bridge based cascaded type MLI. The proposed topology has the flexibility of having different voltage ratios and positioning of voltage source modules to offer more voltage levels with a waned count of power switches. The FRLSMLI has been studied well theoretically with mode diagrams and switching tables first, then simulated for symmetrical and asymmetrical modes in MATLAB R2017b. Finally, tested on the designed a laboratory prototype. The study brings a suggestion to use the FRLSMLI for non-conventional

energy applications, particularly solar applications. Further, analysis in induction motor drive [33], fault determination [34], transient process [35] etc. can be subsumed for future study.

5 REFERENCES

[1] See http://www.bibme.org/citation-guide/apa/

[2] Khomfoi, S. & Tolbert, L. M. (2007). Multilevel power converters. *Power electronics handbook*. Elsevier; ISBN 978-0-12-088479-7, 451-482. https://doi.org/10.1016/B978-012088479-7/50035-3

[3] Lu, S., Corzine, K. A., & Fikse, T. K. (2005). Advanced control of cascaded multilevel drives based on P-Q theory. *Proceedings of IEEE International Conference on Electric Machines and Drives*, 1415-1422.

[4] Du, Z., Tolbert, L. M., & Chiasson, J. N. (2006). Active harmonic elimination for multilevel converters. *IEEE Trans Power Electronics*, *21*(2), 459-469. https://doi.org/10.1109/TPEL.2005.869757

[5] Anup, K. P. & Sushree, S. P. (2015). Analysis of cascaded multilevel inverters for active harmonic filtering in distribution networks. *Electrical Power and Energy Systems*, *66*, 216-226. https://doi.org/10.1016/j.ijepes.2014.10.034

[6] Surendra, B. N. N. V. & Fernandes, B. G. (2014). Cascaded Two-Level Inverter-Based Multilevel STATCOM for High-Power Applications. *IEEE Transactions on Power Delivery*, *29*(3), 993-1001. https://doi.org/10.1109/TPWRD.2014.2305692

[7] Lai, J. S, Peng, F. Z., & Rodriguez, J. (2002). Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions on Power Electronics*, *49*(4), 724-738. https://doi.org/10.1109/TIE.2002.801052

[8] Su, G. J. (2005). Multilevel dc-link inverter. *IEEE Transactions on Industrial Applications*, *41*(3), 848-854. https://doi.org/10.1109/TIA.2005.847306

[9] Akagi, H., Nabae, T., & Takahashi, I. (1981). A new neutral-point clamped PWM inverter. *IEEE Transactions on Industrial Applications*, *IA-17*, 518-523. https://doi.org/10.1109/TIA.1981.4503992

[10] Edwin, S. J. & Titus, S. (2016). A level Dependent Sources Concoction Multilevel Inverter Topology with Reduced Number of Power. *Journal of Power Electronics*, *16*(4), 1316-1323. https://doi.org/10.6113/JPE.2016.16.4.1316

[11] Al-Judi, A. & Nowicki, E. (2013). Cascading of diode bypassed transistor-voltage-source units in multilevel inverters. *IET Power Electronics*, *6*(3), 554-560. https://doi.org/10.1049/iet-pel.2011.0499

[12] Jagabar, S. M. A. & Vijayakumar, K. (2018). An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications. *Renewable and Sustainable Energy Reviews*, *82*(3), 3379-3399. https://doi.org/10.1016/j.rser.2017.10.052

[13] Baker RH. Electric power converter. US Patent 03-867-643; February 1975.

[14] Nabae, A., Takahashi, I., & Akagi, H. (1980). A new neutral-point clamped PWM inverter. *In Proceeding of the industryapplicationsociety conference*, 761-766.

[15] Meynard, T. A. & Foch, H. (1992). Multi-level conversion high voltage choppers and voltage source inverters. *In Proceedings of the IEEE power electronics specialist conference*, *1*, 397-403. https://doi.org/10.1109/PESC.1992.254717

[16] Ehsan, E. & Farhad, M. (2013). Multi-Winding Transformer-Based Diode Clamping Multilevel Inverter, Experimental Results. *Journal of Circuits, Systems, and Computers*, *22*(8), 1350071-1350079. https://doi.org/10.1142/S0218126613500710

[17] Ebrahim, B., Concettina, B., & Carlo, C. (2019). New 8-Level Basic Structure for Cascaded Multilevel Inverters with Reduced Number of Switches and DC Voltage Sources. *Journal of Circuits, Systems and Computers*, *28*(03) https://doi.org/10.1142/S0218126619500385

[18] Ebrahim, B. & Sara, L. (2016). New Extendable 15-Level Basic Unit for Multilevel Inverters. *Journal of Circuits, Systems, and Computers*, *25*(12), 1650151. https://doi.org/10.1142/S0218126616501516

[19] Ebrahim, B. & Seyed, H. (2009). New cascaded multilevel inverter topology with minimum number of switches. *Energy Conversion and Management*, *50*, 2761-2767. https://doi.org/10.1016/j.enconman.2009.06.032

[20] Hew, W. P., Nasrudin, A. R., & Jafferi, J. (2013). New Three-Phase Multilevel Inverter with Shared Power Switches. *Journal of Power Electronics*, *13*(5). https://doi.org/10.6113/JPE.2013.13.5.787

[21] Tapas, R., Pradip, K. S., & Abhijit, D. (2017). A New Single Phase Multilevel Inverter Topology with Two-step Voltage Boosting Capability. *Journal of Power Electronics*, *17*(5).

[22] Venkataramanaiaha, J., Suresha, Y., & Anup, K. P. (2017). A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies. *Renewable and Sustainable Energy Reviews*, *76*, 788-812. https://doi.org/10.1016/j.rser.2017.03.066

[23] Lee, S. S. (2018). Single-Stage Switched-Capacitor Module (S3CM) Topology for Cascaded Multilevel Inverter. *IEEE Transactions on Power Electronics*, *33*(10), 8204-8207. https://doi.org/10.1109/TPEL.2018.2805685

[24] Hsieh, C., Liang, T., Chen, S., & Tsai, S. (2016). Design and Implementation of a Novel Multilevel DC-AC Inverter. *IEEE Transactions on Industry Applications*, *52*(3), 2436-2443. https://doi.org/10.1109/TIA.2016.2527622

[25] Lee, S. S., Sidorov, M., Lim, C. S., Idris, N. R. N., & Heng, Y. E. (2018). Hybrid Cascaded Multilevel Inverter (HCMLI) With Improved Symmetrical 4-Level Submodule. *IEEE Transactions on Power Electronics*, *33*(2), 932-935. https://doi.org/10.1109/TPEL.2017.2726087

[26] Ramkumar, S., Kamaraj, V., Thamizharasan, S., & Jeevananthan, S. (2012). A new series parallel switched multilevel dc-link inverter topology. *International Journal of Electrical Power and Energy Systems*, *36*(1), 93-99. https://doi.org/10.1016/j.ijepes.2011.10.028

[27] Erol, C. H. & Hüseyin, S. (2017). The Increasing Harmonic Effects of SSPWM Multilevel Inverter Controlling Load Currents Investigated on Modulation Indeks. *Tehnički vjesnik*, *24*(3), 397-404. https://doi.org/10.17559/TV-20151020134629

[28] Thamizharasan, S., Baskaran, J., Ramkumar, S., & Jeevananthan, S. (2015). A Carrierless PWM Strategy for Multilevel Inverters. *IET Power Electronics*, *8*(10), 2034-2043. https://doi.org/10.1049/iet-pel.2014.0742

[29] Sangeetha, S. & Jeevananthan, S. (2014). Neighbourhood Crossover Embroiled Binary GA Based SHEPWM for Seven Level MLI. *AMSE Journals-2014-Series: Advances D*, *19*(1). 15-32.

[30] Krishnakumar, V., Kamaraj, V,. Jeevananthan, S. (2015). Random Pulse Width Modulation Technique for Performance Improvement of Multilevel Inverter Brushless DC Motor Drive. *Australian Journal of Basic and Applied Sciences*, *9*(16), 162-171.

[31] Sangeetha, S. & Jeevananthan, S. (2015). Influence of crossover methods used by genetic algorithm-based heuristic to solve the selective harmonic equations (SHE) in multi-level voltage source inverter. *Sadhana- Springer (Journal of Indian Academy of Sciences)*, *40*(8), 2389-2410. https://doi.org/10.1007/s12046-015-0422-2

[32] Kannan, C., Mohanty, N. K., & Selvarasu, R. (2017). A new topology for cascaded H-bridge multilevel inverter with PI and Fuzzy control. *Energy Procedia*, *117*, 917-926.

https://doi.org/10.1016/j.egypro.2017.05.211
[33] Jeevananthan, S., Paramasivam, S., & Thamizharasan, S. (2012). A novel invariable carrier frequency multi-level inverter PWM for balancing switching transitions and better distribution of harmonic power. *Int. J. Power Electronics*, *4*(3), 290-301. https://doi.org/10.1504/IJPELEC.2012.046601
[34] Erol, C. (2018). Analysis and Performance with Vertical Divided Multilevel Voltage on Phase of Induction Engine. *Tehnički vjesnik*, *25*(3), 687-693. https://doi.org/10.17559/TV-20170425110919
[35] Erol, C. (2019). Fault Determination and Analysis of Complex Switching Structure at Multilevel Inverter. *Tehnički vjesnik*, *26*(2), 398-404. https://doi.org/10.17559/TV-20180417194701
[36] Nenad, M., Slobodan, B., Jeroslav, Ž., & Uroš, J. (2017). Simulation of the Impact of Higher Harmonics on the Transient Process of Induction Machine Fed from PWM Inverters. *Tehnički vjesnik*, *24*(1), 265-271. https://doi.org/10.17559/TV-20150502231618

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