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Symmetric Multi-Level Boost Inverter with Single DC Source Using Reduced Number of Switches

Marikkannu MARIMUTHU*, Subramanian VIJAYALAKSHMI

Abstract: In this paper a novel multilevel boost DC to DC converter with H-Bridge inverter circuit for single DC source is proposed. The proposed scheme has two stages: the first one is a multilevel boost converter which gives a multilevel dc output for a single dc source and the second level is a H-Bridge converter which converts multilevel DC to multilevel AC at required frequency. This DC-DC converter not only reduces the DC source but also reduces the switches, diodes and capacitors. This leads to decrease of the amount and the inverter space installation in order to increase the required output voltage by increasing the number of capacitors and diodes in the DC to DC converter. Comparison between the number of power switches for the suggested topology and other topologies in the recent literature is presented. Simulation results are conveyed through MatLAB/Simulink domain and the working of the suggested converter is realized.

Keywords: level circuit; multi-level boost converter (MBC); multi-level inverter (MLI); pulse width modulation (PWM); total harmonic distortion (THD)

1 INTRODUCTION

In order to achieve high boost ratios and excellent efficiency, there are several implemented boost topologies with transformer-less converter. In the conventional boost converter, the capacitor current is discontinuous resulting in larger capacitor size and EMI issues [1-5]. The MBC is the mixture of traditional boost DC-DC converter and the switched capacitor which works to provide different output voltages and a self-sustained voltage using one inductor, one switch, $2M - 1$ (M - number of level) capacitors and $2M - 1$ diodes for M*MBC. It is a PWM based boost converter, where there are different required voltage levels with unidirectional current flow, and self-adjusting various level converters [6-11]. The main advantages of this converter are: it allows high switching frequency, a high gain beyond extreme duty cycle, continuous input current, and excludes transformer. Without modifying the main circuit, more levels of the converter should be achieved by adding diodes and capacitors. In order to achieve reduced switching losses, improved high voltage operation capability, less Electro Magnetic Interference (EMI), and high voltage gain, multilevel inverters are preferred.

To fulfill the demand of power rating and improved power quality with the reduced harmonic distortion, multilevel inverter is better than conventional inverter. Because the gate pulse used in the switches of MLI is high switching frequency PWM is recommended. Due to the easiness of the control and modularity the MLI is highly preferable to conventional inverter.

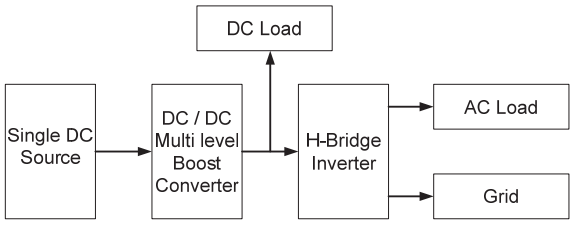


Figure 1a Proposed MLI block diagram

The AC power supply with high power quality and less THD is the primary requirement for the significance of High power. To meet this requirement multilevel inverters are normally used for their sinusoidal like output. In general, the renewable energy sources are DC. It is very hard to get a pure sinusoidal AC output with the use of filters. It may increase overall cost of the system. Hence multilevel inverters are used in such applications. Multilevel inverters are classified into two major categories with single source and multiple sources. H-Bridge topology is used in multiple source inverters and the single source inverters use large capacitor banks. Fig. 1b shows the proposed MLI topology with Multi level Boost converter topology.

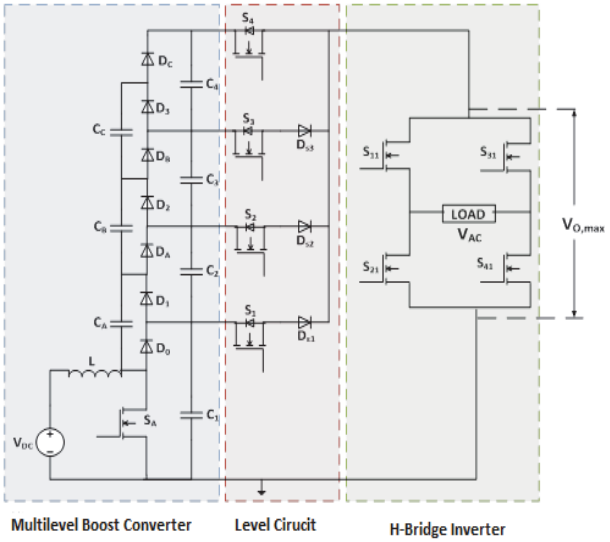


Figure 1b Proposed MLI topology with Multi boost DC to DC converter

The minimum power renewable energy sources have no significance in high power applications, the dc boost converters are used to interface low power sources [20]. The proposed topology can be built for both low and high power application. This circuit consists of a single source multi-level boost converter whose output is the source of H-Bridge inverter. M-level inverter output can be obtained through this topology. The M-level stepped AC output voltage waveform can be obtained using one DC source, minimum number of switches, diodes and capacitors.

Applications of the extended MLI circuit are listed below: computer, telecom power supplies in remote areas supplied from solar panels, electric vehicles [22], uninterrupted power supplies [4] and renewable energy microgrid [21, 23].

2 PROPOSED TOPOLOGY

Fig. 1b depicts the symmetric 9-level inverter. It consists of three units for DC-AC conversion: 1. the multilevel DC to DC Boost converter, 2. the AC output level changing circuit and 3. the conventional H-Bridge inverter. The Multilevel DC-DC Boost converter is the extension of traditional boost converter.

3 MULTILEVEL BOOST CONVERTER

The Boost converter with multilevels consists of a conventional boost converter combined with the voltage multiplier stages as shown in Fig. 2. This MBC contains a switch, inductor, $2M-1$ Capacitors and $2M-1$ diodes to attain the M times of the output voltage of the traditional boost converter. In the proposed topology four levels output is designed. For 4 levels DC output 7 diodes and 7 capacitors are used. In Fig. 1, first part shows the four level boost converters. One important feature of the multilevel dc-dc boost converter is that the level numbers can be raised by adding only diodes and capacitors and need not modify the prime circuit [12, 13].

In First part of Fig. 1, V_{dc}, L, $S1$ constitutes a conventional boost converter. The remaining components in the circuit provide a multiplier output that is VC times M, where $2M + 1$ is the converter number of levels considering the significance of the zero level. The voltage output and the current through the Inductor of the traditional boost converter is

$$\frac{V_C}{V_{dc}} = \frac{1}{1-D} \tag{1}$$

$$I_L = \frac{V_O}{(1-D)R} \tag{2}$$

where V_C, V_{dc}, D, I_L, and R are the output voltage, input source voltage, duty ratio, inductor current, and load resistance respectively.

The new voltage gain can be expressed by Voltage gain

$$N = M \times \frac{1}{1-D} = M \times K \tag{3}$$

where M is the Level of Boost Converter

D is the Duty cycle = $\dfrac{T_{ON}}{T_{ON}+T_{OFF}}$

T_{ON} - Switch ON time
T_{OFF} - Switch OFF time

The inductance L_{crit} of the converter is resolved by the duty cycle D, the switching frequency and the Load resistance R

$$L_{crit} = \frac{D \times (1-D) \times R}{2 \times f} \tag{4}$$

The value of the capacitor is designed based on

$$C = \frac{D}{R \times f \times V_r} \tag{5}$$

where V_r is the output voltage ripple factor

$$V_r = \frac{\Delta V_{out}}{V_{out}} \tag{6}$$

The voltage stress across switch and diode will be calculated as

$$V_{str} = \frac{V_{dc}}{1-D} \tag{7}$$

The potential of the k^{th} level stage across the capacitor

$$kV_c = \frac{V_{dc}}{1-D} - nV_D \tag{8}$$

where M is the total number of diodes encountered till the n^{th} stage. Multilevel Boost converter has two modes of operation, described below.

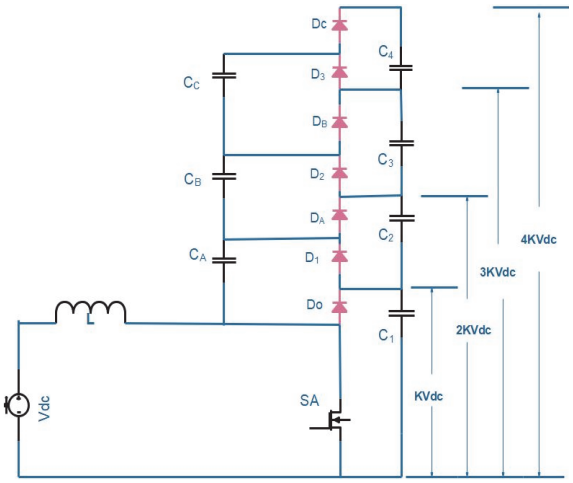


Figure 2 Multi level Boost Converter

During the switch S_A in ON state, the source voltage V_{dc} is charged by the inductor. The capacitor C_A voltage is less than the voltage of C_1, then the C_1 voltage is clasped across C_A through the diode D_1. In a synchronic way if $C_A + C_B + C_C$ voltage is less than $C_1 + C_2 + C_3$ then C_3, C_2, C_1 clasp the voltage across C_A, C_B, C_C.

When Switch S_A is OFF condition, D_0 is closed and all diodes are made to conduct because of inductor current. Finally, C_4, C_3, C_2, C_1 is clasped by C_C, C_B, C_A, input voltage and inductor voltage.

4 LEVEL CIRCUIT

The function of the level circuit in the prescribed topology is to produce the stepped level input to the H-Bridge inverter. The switch S_1 is ON then the voltage at the capacitor C_1 (kV_{dc}) is the input of H-Bridge inverter through S_1 and D_1. When S_2 is ON, then the sum of the voltage at C_1

and C_2 ($2kV_{dc}$) is the inverter input. Similarly when S_3, S_4 is ON then the inverter input is $3kV_{dc}$ and $4kV_{dc}$ respectively. The operation of the Level circuit is depicted in Tab. 1.

Table 1 Level circuit operation

S_1	S_2	S_3	S_4	Output from level circuit
1	0	0	0	$+kV_{dc}$
0	1	0	0	$+2kV_{dc}$
0	0	1	0	$+3kV_{dc}$
0	0	0	1	$+4kV_{dc}$

5 MLI WITH SINGLE H-BRIDGE

Fig. 3 is the H-Bridge inverter derived from the model graphical representation of such a circuit.

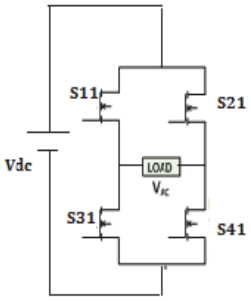


Figure 3 H-Bridge inverter

A H-Bridge is constructed by four power switches namely MOSFET, IGBT, or BJT. Whenever the switches S_{11} and S_{41} are turned ON a positive voltage will be applied to the load and the switches S_{21} and S_{31} are closing; then the reverse voltage is applied to the load. Tab. 2 and Fig. 4 represent the level selection, inverter operation and its corresponding output.

In relation to the input voltage level of inverter, the output voltage level of the inverter is found. The number of output voltage levels of the inverter is taken as M, and n is the multi boost converter output voltage level number.

$$\text{The number of switches} = 5 + n \tag{9}$$

$$\text{Number of diodes} = \frac{3M-7}{2} \tag{10}$$

$$\text{Number of capacitors} = M - 2 \tag{11}$$

$$\text{Inverter level } M = 2n + 1 \tag{12}$$

The output voltage across the multi-level boost converter is

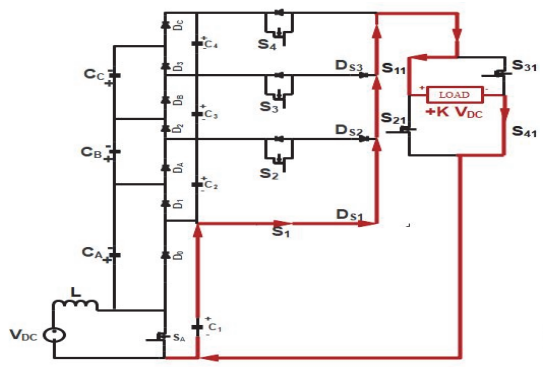
$$V_{0DC} = \sum_{i=1}^{\frac{M-1}{2}} V_i \tag{13}$$

where V_i is the individual capacitor voltage

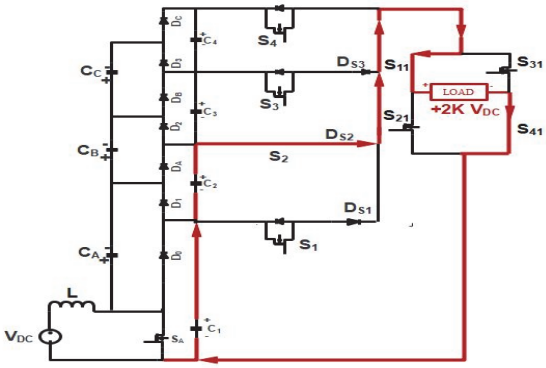
$$= \frac{V_{in}}{1-D} \times M \tag{14}$$

D is the switching ratio of Boost converter

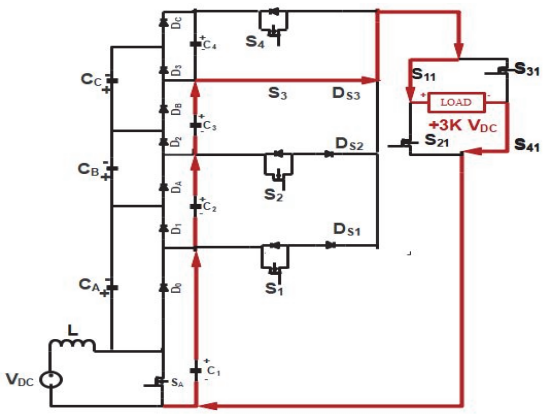
$$V_{0,\max} = \begin{cases} +\sum_{i=1}^{\frac{N-1}{2}} V_i, S_{11} = S_{41} = \text{ON} \\ -\sum_{i=1}^{\frac{N-1}{2}} V_i, S_{21} = S_{31} = \text{ON} \end{cases} \tag{15}$$



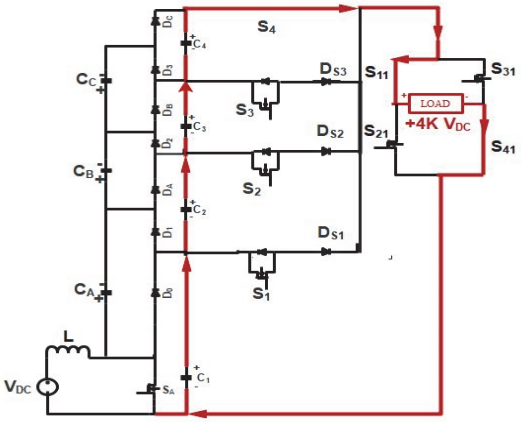
(a) Multi level inverter output is kV_{dc}



(b) Multi level inverter output is $2kV_{dc}$

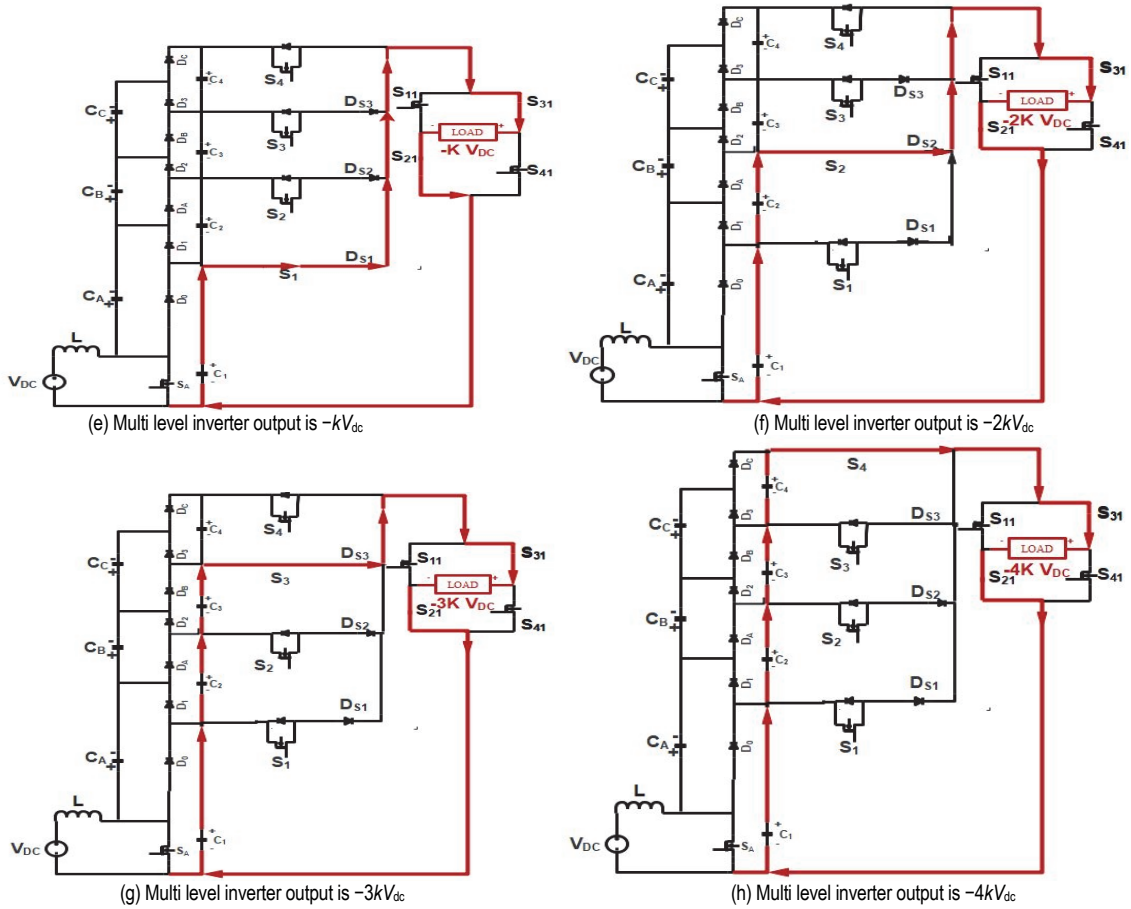


(c) Multi level inverter output is $3kV_{dc}$



(d) Multi level inverter output is $4kV_{dc}$

Figure 4 Multi level inverter operation



(e) Multi level inverter output is $-kV_{dc}$

(f) Multi level inverter output is $-2kV_{dc}$

(g) Multi level inverter output is $-3kV_{dc}$

(h) Multi level inverter output is $-4kV_{dc}$

Figure 4 Multi level inverter operation (continuation)

Fig. 4a shows the voltage at C_1 (kV_{dc}) applied to the inverter load via the switch S_1, D_{S1}, S_{11} and S_{41}, Similarly the sum of voltage at C_1 and C_2 is applied to the load via the switch S_2, D_{S2}, S_{11} and S_{41} is depicted in Fig. 4b. Similarly $3kV_{dc}$, $4kV_{dc}$, kV_{dc}, $-2kV_{dc}$, $-3kV_{dc}$, $-4kV_{dc}$ is illustrated in Figa. 4c, 4d, 4e, 4f, 4g and 4h respectively. The operation of multilevel inverter is also explained through Tab. 2.

Table 2 Output voltage of the H-Bridge inverter

	Levels	Switching sequence				Voltage Levels
		*S*1	*S*2	*S*3	*S*4	
Positive Half cycle *S*11, *S*41 ON	0	OFF	OFF	OFF	OFF	0
	1	ON	OFF	OFF	OFF	$+kV_{dc}$
	2	OFF	ON	OFF	OFF	$+2kV_{dc}$
	3	OFF	OFF	ON	OFF	$+3kV_{dc}$
	4	OFF	OFF	OFF	ON	$+4kV_{dc}$
	3	OFF	OFF	ON	OFF	$+3kV_{dc}$
	2	OFF	ON	OFF	OFF	$+2kV_{dc}$
	1	ON	OFF	OFF	OFF	$+kV_{dc}$
	0	OFF	OFF	OFF	OFF	0
Negative Half cycle *S*21, *S*31 ON	1	ON	OFF	OFF	OFF	$-kV_{dc}$
	2	OFF	ON	OFF	OFF	$-2kV_{dc}$
	3	OFF	OFF	ON	OFF	$-3kV_{dc}$
	4	OFF	OFF	OFF	ON	$-4kV_{dc}$
	3	OFF	OFF	ON	OFF	$-3kV_{dc}$
	2	OFF	ON	OFF	OFF	$-2kV_{dC}$
	1	ON	OFF	OFF	OFF	$-kV_{dc}$
	0	OFF	OFF	OFF	OFF	0

6 SIMULATION RESULTS

Fig. 5 depicts the simulated topology for H-Bridge inverter with MBC using MatLAB/Simulink. The gate pulse whose switching frequency is 10 kHz and 50% duty cycle of PWM pulse is given to the multilevel boost converter switch. The selection of level circuit switches is made through MatLAB program. In the H-bridge inverter, for the first 10 mS gate pulse with the frequency of 100 Hz is given to the positive output pair (S_{11} and S_{41}) the next 10 mS gate pulse is given to negative output pair (S_{21} and S_{31}). The design parameters of the multilevel boost converter fed H-Bridge inverter of the simulation circuit are shown in Tab. 2.

The DC voltage input of the MBC is 21 V and the capacitor voltage (output) *C*1 is 46 V, sum of *C*1 and *C*2 output is 86 V. Simultaneously by the addition of *C*1, *C*2 and *C*3, and *C*1, *C*2, *C*3 and *C*4 outputs are 126 V and 166 V respectively, illustrated in Fig. 5. Tab. 3 depicts the design parameters of Multilevel Boost converter fed H-Bridge inverter. By using the Eqs. (4) and (5), the inductor and capacitor values are calculated.

Table 3 Design parameters of multilevel boost converter fed H-Bridge inverter

Parameters	Values
Input voltage for DC-DC Converter	21 V
Output voltage for both DC-DC converter & Inverter	168 V
Duty cycle	50 %
Capacitor C_1, C_2, C_3, C_4, C_A, C_B, C_C	89 µF
Inductor	8 mH
Switching frequency of MBC	10 kHz
Switching frequency of MLI	50 Hz
Load Resistance	25 Ω

The H-Bridge 9-level inverter output voltage (0, 40,80,120, 160, −40, −80, −120, −160) with the total time period of 20 mS is depicted in Fig. 6. Depending upon the load value the output current will be varied. The output current inverter waveform is also illustrated in Fig. 6.

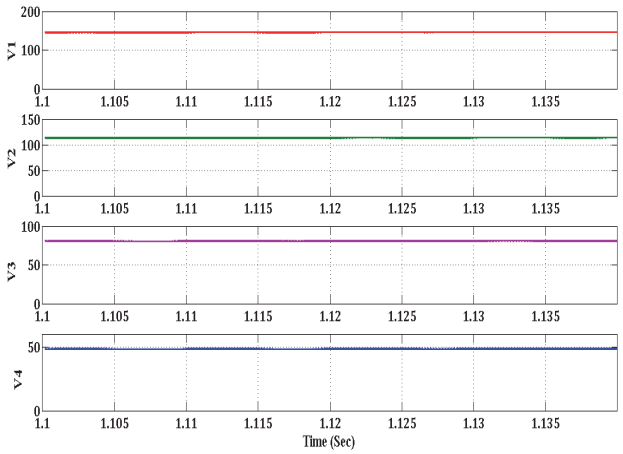


Figure 5 Capacitor output voltages at Multi level boost converter

7 RESULTS AND DISCUSSION

Key traits of the proposed topology with its correlatives are analyzed with Multilevel Inverter as NPCMLI, FCMLI, CHBI, Symmetric MLC (SMLC) [16], SCQNLI [18], A Cascaded MLI based on Switched Capacitor [19], Self-balanced step-up MLI [14], and A Quasi Resonant Switched Capacitor MLI (QRSCMLI) with self-voltage stabilizing [15] is depicted in Tab. 4. A comparative analysis of some of the key traits of the recommended topology with its correlative is presented in Tab. 4. The evaluation is made in terms of number of switches (N_{swi}), number of gate drives (N_{dri}), sources (N_{sou}), and the diodes (N_{dio}) for nine level multi level inverter.

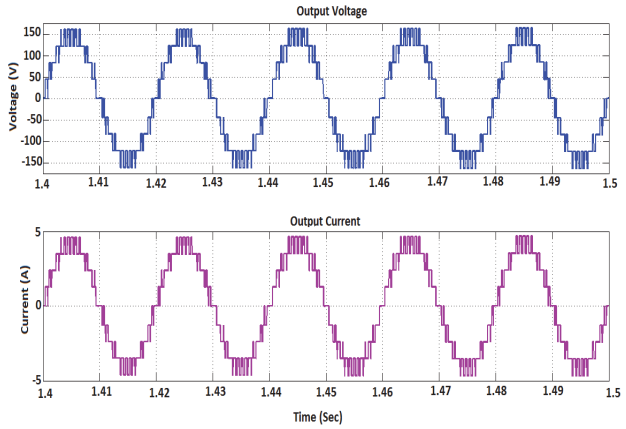


Figure 6 H-Bridge inverter output voltage and Current

In terms of reliability, the second critical component is that of the capacitors, and it is essential to hold on its count lesser.

Table 4 Comparison of the recommended MLI with the preexisting and present recommended topologies Component count

Reference Name or No.	N_{swi}	N_{dri}	N_{dio}	N_{cap}	N_{sou}
NPC MLI	16	16	56	8	1
FC MLI	16	16	--	36	1
CHB	16	16	--	--	4
[16]	10	10	--	4	2
[18]	12	12	0	2	1
[19]	12	12	2	2	2
[14]	19	19	3	3	1
[15]	10	10	4	4	1
Proposed	9	9	10	7	1

It is visible from Tab. 4 that one of the MLIs, the recommend circuit needs a lesser count of switches, sources and driver circuit. Further generalized circuits have a higher number of switches, and also have too many of either capacitors, or diodes or sources, which increases not only the cost but losses also, which substantially decreases the efficiency of the circuit. The remaining circuits [14-19] have more switches than the proposed one.

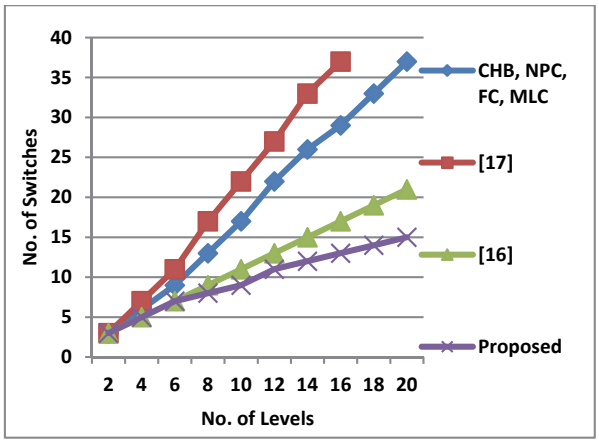


Figure 7 Number of levels V_S amount of switches for MLI

The number of levels V_S number of switches is given in Fig. 7. From the graph one can understand that the CHB, NPC, FC and [17] need higher number of switches. It is clear that recommended topology needs lesser amount of switches than the other topologies.

8 HARDWARE RESULTS

The prototype model for Multilevel DC-DC converter fed H-Bridge inverter is depicted in Fig. 7. The components used in the prototype model are shown in Tab. 5.

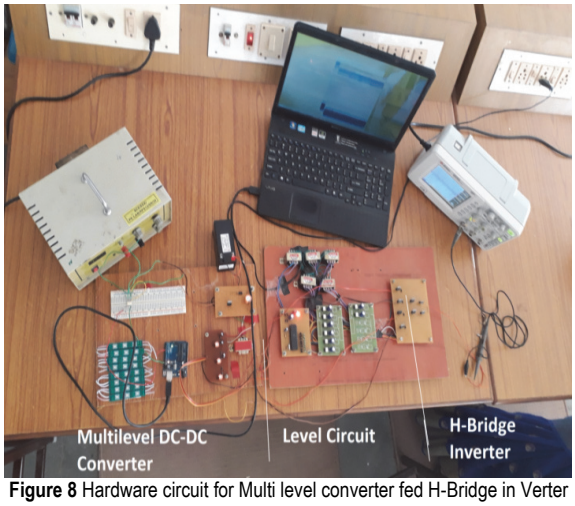


Figure 8 Hardware circuit for Multi level converter fed H-Bridge in Verter

The input voltage given to the MBC DC/DC boost converter is 2.8 V, and the pulse with 50% duty ratio of the boost converter is furnished in Fig. 9. Four different output voltage levels can be attained in the boost converter. At level 1 ($C1$) and level 2 ($C1 + C2$), the obtained output voltage is 5.6 V, 11.2 V respectively, illustrated in Fig. 10. The level 3 voltage is ($C1 + C2 + C3$) and the voltage at level 4 ($C1 + C2 + C3 + C4$) is 16.8 V and 22.4 V

respectively depicted in Fig. 11. The gate pulse with the time period of 10 mS given to the couple of the switch in the H-Bridge Inverter is furnished in Fig. 12. AC output obtained from the MLI is shown in Fig. 13.

Table 5 Experimental values for the proposed circuit

Description	Experimental values
MOSFET	IRF 840
Diode	2N 4007
Duty cycle	50 %
Capacitor C_1, C_2, C_3, C_4, C_A, C_B, C_C	70 µF
Inductor	7 mH
Switching frequency of DC-DC converter	10 kHz
Switching frequency of Inverter	50 Hz
Load Resistance	100 Ohm
Input Voltage (V_{dc})	2.8 V
Multi level DC Output Voltage (V_o)	5.6 V, 11.2 V, 16.8 V, 22.4 V
Input current (I_{in})	1.9 A
Load current (I_o)	0.9 A
Pulse generated for Multi level DC converter by Arduino controller (SMDR3)	5V, 10 kHz
Pulse generated for H-Bridge Inveter by Mircocontroller (ATMEL 89S51)	5V, 50 Hz

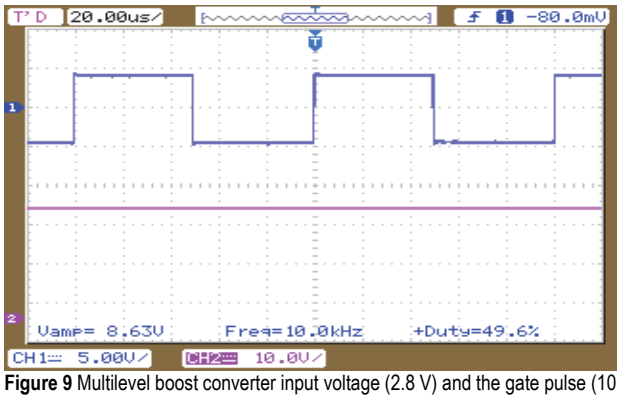


Figure 9 Multilevel boost converter input voltage (2.8 V) and the gate pulse (10 kHz) for main switch

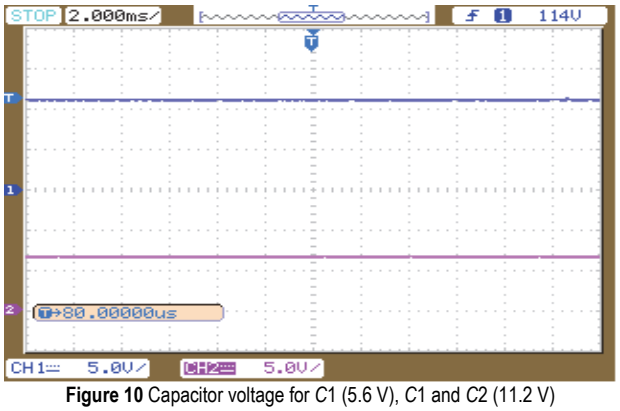


Figure 10 Capacitor voltage for *C*1 (5.6 V), *C*1 and *C*2 (11.2 V)

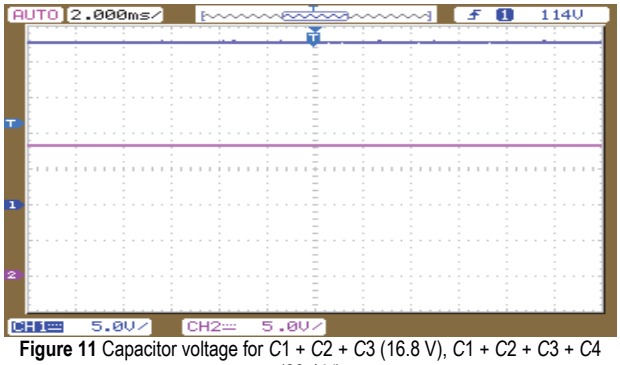


Figure 11 Capacitor voltage for *C*1 + *C*2 + *C*3 (16.8 V), *C*1 + *C*2 + *C*3 + *C*4 (22.4 V)

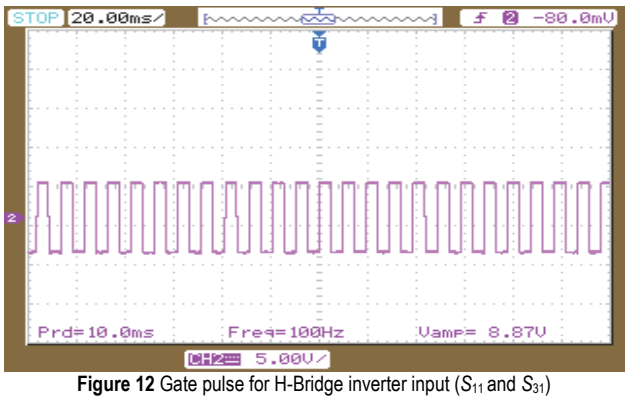


Figure 12 Gate pulse for H-Bridge inverter input (S_{11} and S_{31})

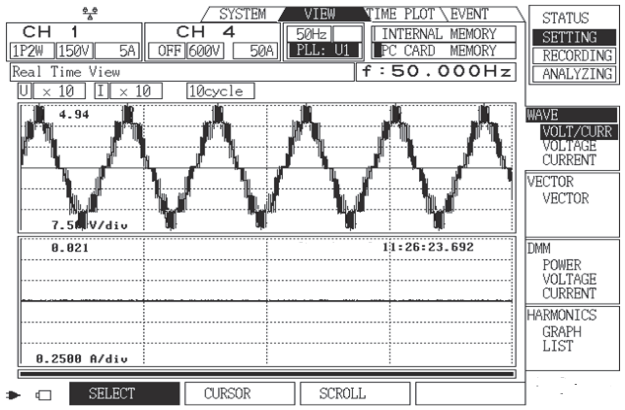


Figure 13 Multi level Inverter Output Voltage

9 CONCLUSION

The proposed modern multilevel inverter has required isolated voltage source (DC) and minimum quantity of switches. An input voltage from the DC source has been boosted up at a different level. It needs only a conventional H-Bridge Inverter for obtaining any number of required levels of the inverter. The proposed topology extends up to the required quantity of levels and could be raised by raising the number of diodes and capacitors only. It decreases the amount of diodes, switches, cost, dimension of the system and the amplitude of the total blocked reverse voltage in verification with the conventional and similar circuits. At the end, the capability and working of *M* level MLI circuit has been proved with various simulations and practical outcomes.

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Contact information:

Marikkannu MARIMUTHU
(Corresponding author)
Saranathan College of Engineering,
Trichy, Tamilnadu, India - 620012
E-mail: marimuthueeephd@gmail.com

Subramanian VIJAYALAKSHMI
Saranathan College of Engineering,
Trichy, Tamilnadu, India - 620012
E-mail: bksviji@gmail.com