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Performance comparison between optimization algorithms for asymmetrical cascaded multilevel inverter control

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ABSTRACT

This paper discusses the hardware and control system design of the asymmetric cascade multilevel inverter. The asymmetric cascaded multilevel inverter structure is adopted to minimize bridges, gate drive circuits and DC power source number. Therefore, the proposed structure is able to generate higher voltage at higher speed with low switching losses and high efficiency. Selective Harmonic Elimination (SHE) based on Newton-Raphson (N-R) algorithm is developed to calculate a switching angle for a range of modulation index to control asymmetric cascade multilevel inverter. Simulation results prove that Newton-Raphson technique is more effective than genetic algorithm (G-A) and equal calculated switching angles method (ECSA). A comparison between the algorithm performance for 9-level asymmetric cascade H-bridge inverter control was evaluated and experimentally tested on FPGA-based prototypes

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Asymmetrical CHB multilevel inverter; Newton-Raphson algorithm; genetic algorithm switching angles; THD; FPGA

1. Introduction

Multilevel inverters are an appealing option for applications in high power because of their superior efficiency than two-level inverters. In this regard, there are three forms: multilevel inverter clamped diode, multilevel inverter flying capacitor and CHB multilevel inverter [1,2].

Compared to clamped diode, flying capacitor multilevel inverter and cascaded H-bridge (CHB) inverter needs fewer components while achieving the same amount of voltage levels. Furthermore, optimized circuit architecture is feasible as each stage has the same structure, without the need to an extra-clamping diodes or capacitors [3,4].

Considering the same number of power electronics, by varying the ratio between DC source voltages, asymmetric CHB configuration produces a higher number of output levels than the symmetric one. As a result, an asymmetrical cascaded multilevel inverter's storage area and overall cost are smaller than symmetrical inverter-based applications [5–7].

In the literature, several approaches are put out for the harmonic elimination. The methods based on conventional pulse width modulation (PWM) cannot fully eliminate lower order harmonics [8,9]. In addition, Space Vector Modulation (SPVM)-based cascaded multilevel inverter topology control remains limited to a small number of rates due to the wide number of switching vectors [10].

Selective harmonic elimination (SHE) for multilevel inverter control requires nonlinear harmonic equations to be solved in order to eliminate lower order harmonics based on calculated switching angles. In this regard, the resulting theory has been proposed in many works to develop a mathematical model; however, this approach remains complicated, time-consuming and not suitable for variable DC sources. Furthermore, many studies have been conducted to find optimal angles using optimization techniques such as the theory of resulting polynomials (PRT) [11] or solutions based on genetic algorithms (GA) [8]. In the PRT solution, the resulting high-order polynomial terms can no longer be solved when the voltage levels of multilevel inverters are high. The main challenge in a GA-based method is that the result might fall into the trap of local minima. Thus, despite its considerable efficiency for problems with large dimensional optimization, it cannot guarantee the best optimized result [12].

In order to implement real-time control systems in power electronic applications, the system designers have many choices. Microcontrollers, microprocessors and DSPs are software-based devices, which come with efficient software compilers and programs usually written in C or assembly language. Furthermore, the advantages of MCU and DSP, such as simple circuitry, software realization and flexibility, have been exploited in online and offline switching angle calculation for multilevel inverter control in [13]. Although

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these technologies are matured and usually have a dedicated PWM generation block, they have limited sampling rates and limited speed due to their natural sequence-based operation and the programs are executed line by line, not simultaneously.

Furthermore, when DSP or MCU cannot provide sufficient on-chip peripherals, such as comparators and dead-time controllers, to support the outputs of control signals, additional hardware circuits must be designed to work with the controller.

An attractive idea is to use Application Specific Integrated Circuit (ASIC) to implement switching angles for inverter control. FPGA is a subclass of ASIC devices that delivers features such as fast prototyping, simple hardware and software design and higher switching frequency. The development on FPGA has reached a maturity level which has made them the choice to implement in many fields [13]. In addition, switching angles are analyzed and implemented in FPGA to control asymmetrical cascaded 9-level CHB inverters to solve the above problems and to provide easy, fast and steady control.

Asymmetrical cascaded 9-level inverter performances are compared based on the switching angles generated by Newton-Raphson, Genetic Algorithm and Equal Calculated Switching Angles (ECSA) [12]. Indeed, the objective of introducing Equal Calculated Switching Angles in performances comparison is to show the significant improvement made by optimization algorithms on output voltages THD by eliminating lower harmonics order [13]. Contrary to what has been reported in [14], in this paper, Newton-Raphson efficiency and accuracy compared with Genetic Algorithm are justified based on simulation and experimental results

This paper is organized as follows: Section 2 describes Multilevel Cascade Inverter Power Topology. Section 3 explains the problem of harmonic elimination in CHB multilevel inverters based on an N-R optimization. Based on simulation results, a comparative study between N-R algorithm, Genetic algorithm and ECSA performances is provided in section 4. To validate simulation results, experimental results are presented in section 5. Finally, section 6 is devoted for concluding remarks.

2. Cascaded multilevel inverter topology

One of several configurations of multilevel inverter is the cascaded multilevel inverter. It is designed, as shown in Figure 1, by connecting single-phase H-bridge inverters in series T11, T12, T13 and T14 are the first HB commutation cells, and T21, T22, T23 and T24 are the second H-B commutation cells.

In symmetrical cascade multilevel inverter, where HBs' DC-link voltages are identical, output voltage level

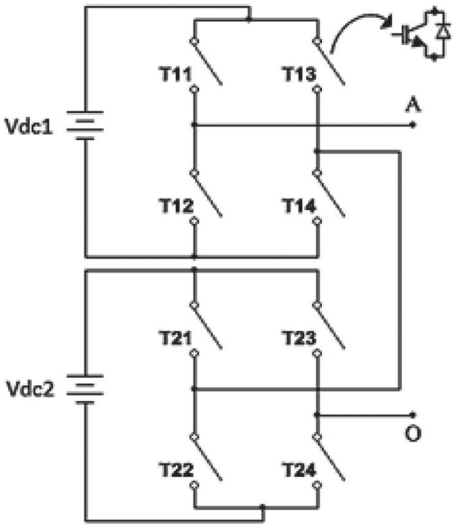

Figure 1. Single-phase topology of: (a) 5-level symmetric CHB inverter for Vdc1 = Vdc2. (b) 7-level asymmetric CHB inverter for Vdc2 = 2Vdc1, (ratio binary). (c) Asymmetrical 9-level CHB inverter for Vdc2 = 3Vdc, (ratio ternary).

numbers are calculated as follows:

$$m = 2h + 1, \quad h: \text{ H - Bridge number} \tag{1}$$

Therefore, the single-phase symmetric inverter output voltage VAO provides 5-level output voltage, if the number of HB unit is equal to 2 ($h = 2$), as shown in Figure 1.

For asymmetric cascade multilevel inverter where the HBs Vdcj DC-link voltages are unequal, the output level numbers are standardized as follows:

$$m = 2(\sum_{j=1}^{h} \lambda_j) + 1, \quad \lambda_j = \frac{\text{Vdc}j}{\text{Vdc1}} \tag{2}$$

For HB unit number $h = 2$ and Vdc2 = 3Vdc1 = 3E, the asymmetrical 9-level HB inverter is obtained as follows: $m = 2(1 + 3) + 1 = 3^2 = 9$.

Asymmetrical cascaded multilevel inverter with binary and ternary ratios are considered as most popular ones. Hence; DC voltages with ratio 1:2:4:8 ... : 2α ($\alpha\epsilon$ âĎŢ*) as binary progression within H-Bridge inverter's maximal output voltage VAO would be equal to (2^h-1) E, and the obtained voltage levels is equal to (2^{h+1}-1). However, in ternary progression, for HB unit DC voltages ratio 1: 3: 9: 27. α: 3α, with $\alpha \varepsilon$ N*, as a result, inverter output voltage is equal to ((3^n-1)/2) E and number of levels is equal to 3^h.

Based on the result given above, the asymmetric structure compared to the symmetrical one, produces higher levels for the same number of bridges. Hence, for the same number of components required, a better output voltage waveform is obtained that makes the asymmetric topology as a good candidate for selective harmonic elimination (SHE) control.

The comparison, provided in Table 1, justifies the choice of 9-level asymmetrical CHB topology with ratio

Table 1. DC-voltage sources and switches comparison for CHB topologies.

Topology	No. of voltage sources	No. of switches	No. of output level
Symmetrical CHB	2	8	5
Asymmetrical CHB (ratio binary)	2	8	7
Asymmetrical CHB (ratio ternary)	2	8	9

ternary among the other topologies for algorithm performances.

3. Optimization-based selective harmonic elimination

3.1. Newton-Raphson analysis

In this section, staircase voltage waveform, as shown in Figure 2, is selected for multilevel inverter selective harmonic elimination (SHE) control [6]. The challenge to be considered is to find suitable switching angles designed by $\theta_1, \theta_2, \theta_3 \ldots \theta_p$, such as p-1 **non-triplen** odd harmonics can be eliminated while achieving fundamental component control [5].

Figure 2 shows 9-level output voltage waveform V_{AO}. VAO is known as an odd-quarter symmetrical waveform with 4 positive steps of equal magnitude.

Fourier series-based periodic function $V_{AO}\ (\omega t)$ development is provided as follows [15]:

$$V_{AO}(\omega t) = B_0 + \sum_{n=1}^{+\infty} B_n \cos(n\omega t) + A_n \sin(n\omega t) \quad (3)$$

The Fourier series for odd functions contain only sine terms: $B_0 = 0$ and $B_n = 0$ for all n. The sine function is odd and the cosine function is not.

$$V_{AO}(\omega t) = \sum_{n=1}^{+\infty} A_n \sin(n\omega t) \quad (4)$$

Considering A_n as the magnitude of the n^{th} harmonic order, the following results:

$$\begin{cases} A_n = \left(\frac{4}{\pi}\right) \int_0^2 V_{AO}(n\omega t) d\omega t & \text{for odd } n \\ = 0, & \text{for even } n \end{cases} \quad (5)$$

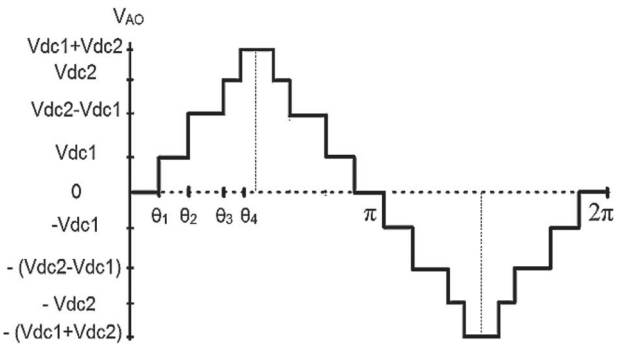

Figure 2. Staircase CHB 9-level inverter output voltage.

$$A_n = \left(\frac{4}{\pi}\right) \int_{\theta_1}^{\frac{\pi}{2}} Vdc1 \sin(n\theta) d\theta, \quad \text{Where } \theta = \omega t \quad (6)$$

$$A_n = 4Vdc/\pi \left[\int_{\theta_1}^{\theta_2} \sin(n\theta) d\theta + \int_{\theta_2}^{\theta_3} \sin(n\theta) d\theta + \int_{\theta_3}^{\theta_4} \sin(n\theta) d\theta \int_{\theta_4}^{\pi/2} \sin(n\theta) d\theta \right] \quad (7)$$

$$A_n = \frac{4Vdc1}{n\pi} [\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4)], \quad n = 1, 3, 5, 7 \quad (8)$$

$$A_n = \frac{4Vdc}{n\pi} \sum_{i=1}^{p} \cos(n\theta_i) \quad (9)$$

Switching angles based on staircase output voltage waveform are calculated as follows:

$$p = \frac{m-1}{2} \quad (10)$$

m and p are, respectively, the number of output voltage level and switching angles number.

For $m = 9$, harmonics to be eliminated is equal to (p-1) = 3.

When switching angles are equal to zero, fundamental voltage is maximal and obtained as follows:

$$A_{1\,\max} = \frac{4p}{\pi} V_{dc1} = \frac{16}{\pi} E \quad (11)$$

Lower order harmonics produce output voltage and current with higher THD. It is desirable to control at a certain value the output voltage of fundamental component while eliminating lower order harmonics as much as possible.

Angles $\theta_1, \theta_2, \theta_3$ and θ_4 are calculated to eliminate the first three odd non-triplen harmonics 5, 7 and 11 [9]. Triplen harmonics will be systematically eliminated from the three-phase system. Nonlinear equation system (12) solution set is obtained based on an iterative method adopting N-R optimization method [16].

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) = r * \pi \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \\ \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0 \end{cases} \quad (12)$$

Considering modulation index r expression, provided by

$$r = \frac{A_1}{pV_{dc1}} = \frac{A_1}{pE} \quad (13)$$

System (12) is developed to obtain the following equation:

$$F(\theta) = T \quad (14)$$

With:

$$F(\theta)=\begin{bmatrix}\cos(\theta_1) & \cos(\theta_2) & \cos(\theta_3) & \cos(\theta_4)\\ \cos(5\theta_1) & \cos(5\theta_2) & \cos(5\theta_3) & \cos(5\theta_4)\\ \cos(7\theta_1) & \cos(7\theta_2) & \cos(7\theta_3) & \cos(7\theta_4)\\ \cos(11\theta_1) & \cos(11\theta_2) & \cos(11\theta_3) & \cos(11\theta_4)\end{bmatrix} \tag{15}$$

T as the amplitude harmonic vector is given by

$$T=\begin{bmatrix}r\pi\\0\\0\\0\end{bmatrix} \tag{16}$$

The Newton-Raphson (NR) method is a commonly used iterative method for solving equations which are difficult to solve analytically [16]. Below, the NR method is used in Matlab to solve the set of transcendental equations in (12), and the following matrices are implemented:

$$\theta^j=\begin{bmatrix}\theta_1^j\\ \theta_2^j\\ \theta_3^j\\ \theta_4^j\end{bmatrix} \tag{17}$$

F^j is the nonlinear system matrix as given below:

$$F^j=F(\theta^j)=\begin{bmatrix}\cos(\theta_1^j) & \cos(\theta_2^j) & \cos(\theta_3^j) & \cos(\theta_4^j)\\ \cos(5\theta_1^j) & \cos(5\theta_2^j) & \cos(5\theta_3^j) & \cos(5\theta_4^j)\\ \cos(7\theta_1^j) & \cos(7\theta_2^j) & \cos(7\theta_3^j) & \cos(7\theta_4^j)\\ \cos(11\theta_1^j) & \cos(11\theta_1^j) & \cos(11\theta_3^j & \cos(11\theta_3^j)\end{bmatrix} \tag{18}$$

And:

$$\left[\frac{\partial F}{\partial\theta}\right]^j=-\begin{bmatrix}\sin(\theta_1^j) & \sin(\theta_2^j) & \sin(\theta_3^j) & \sin(\theta_4^j)\\ 5\sin(5\theta_1^j) & 5\sin(5\theta_2^j) & 5\sin(5\theta_3^j) & 5\sin(5\theta_4^j)\\ 7\sin(7\theta_1^j) & 7\sin(7\theta_2^j) & 7\sin(7\theta_3^j) & 7\sin(7\theta_4^j)\\ 11\sin(11\theta_1^j) & 11\sin(11\theta_2^j) & 11\sin(11\theta_3^j) & 11\sin(11\theta_4^j)\end{bmatrix} \tag{19}$$

Matrixes (13) to (19) are used for switching angles calculation based on Newton–Raphson [17]. As a result, algorithm steps and procedure are provided as follows:

- Guess a set of initial values for θ^j with $j=0$

$$\text{Assume, } \theta^0=\begin{bmatrix}\theta_1^0\\ \theta_2^0\\ \theta_3^0\\ \theta_4^0\end{bmatrix} \tag{20}$$

- Calculate the value of:

$$F(\theta^0)=F^0 \tag{21}$$

- Linearize equation (14) about θ^0

$$F^0+\left[\frac{\partial F}{\partial\theta}\right]^0 d\theta^0=T \tag{22}$$

$$d\theta^0=\begin{bmatrix}d\theta_1^0\\ d\theta_2^0\\ d\theta_3^0\\ d\theta_4^0\end{bmatrix} \tag{23}$$

- Solve $d\theta^0$ from equation (20):

$$d\theta^0=INV\left[\frac{\partial F}{\partial\theta}\right]^0(T-F^0) \tag{24}$$

Taking into account $INV\left[\frac{\partial F}{\partial\theta}\right]^0$ as the matrix inverse of $\left[\frac{\partial F}{\partial\theta}\right]^0$

- Considering the updated initial values,

$$\theta^{j+1}=\theta^j+d\theta^j \tag{25}$$

(21) to (24) solving process are repeated; until $\mathrm{d}\theta^j$ is satisfied to the desired degree of accuracy, and the condition given below must be satisfied:

$$\theta_1<\theta_2<\theta_3<\theta_4<\frac{\pi}{2} \tag{26}$$

The above equations are used for estimating the optimum switch angle value. Figure 3(a) shows the flow chart for algorithm solving. Hence, the provided flow chart brings more details concerning the calculation process of switching angles. Figure 3 shows that the N-R flow chart refers to the optimal switching angles to eliminate lower order harmonics while optimizing THD value.

3.2. Genetic algorithm analysis

The steps to formulate a problem and applying GA to calculate switching angles for harmonic elimination are as follows:

A. Select binary or floating point strings.
B. Find the number of specific variables to the problem; Founded number will be genes number in

a chromosome. In this application the number of variables is the number switching angles for cascaded multilevel inverter. A 9-level inverter requires four switching angles; thus, each chromosome for this application will have four switching angles, i.e. $(\theta_1, \theta_2, \theta_3, \theta_4)$.

C. Set a population size and initialize the population. Higher population might increase the rate of convergence, but it also increases the execution time. The selection of an optimum-sized population requires some experience in GA. The population in this paper has 20 chromosomes, each containing four switching angles. The population is initialized with random angles between 0 and 90 degree taking into consideration the quarter-wave symmetry of the output voltage waveform.

D. The fitness function plays a very important role in guiding GA to obtain the best solutions within a large search space. The objective of this paper is to minimize lower order harmonics (5, 7 and 11) and reduce the THD. Therefore, the fitness function has to be associated to THD. The fitness function is formulated as follows. $FV(\theta_1, \theta_2, \theta_3, \theta_4) = \frac{V5+V7+V11}{V1}$, where $V1$ is the fundamental component magnitude; $V5$, $V7$ and $V11$ are the magnitudes of harmonics 5,7 and 11, respectively.

To find the desired value GA need to run for a certain number of iterations (1000 in this case). After the first iteration, fitness values are used to determine new offspring. These go through crossover and mutation operations and a new population is created which goes through the same cycle starting from evaluation. After these iterations, the GA finds one solution, such as the switching angle set, producing the maximum FV is the best solution of the first iteration. The flow chart is shown in Figure 3(b).

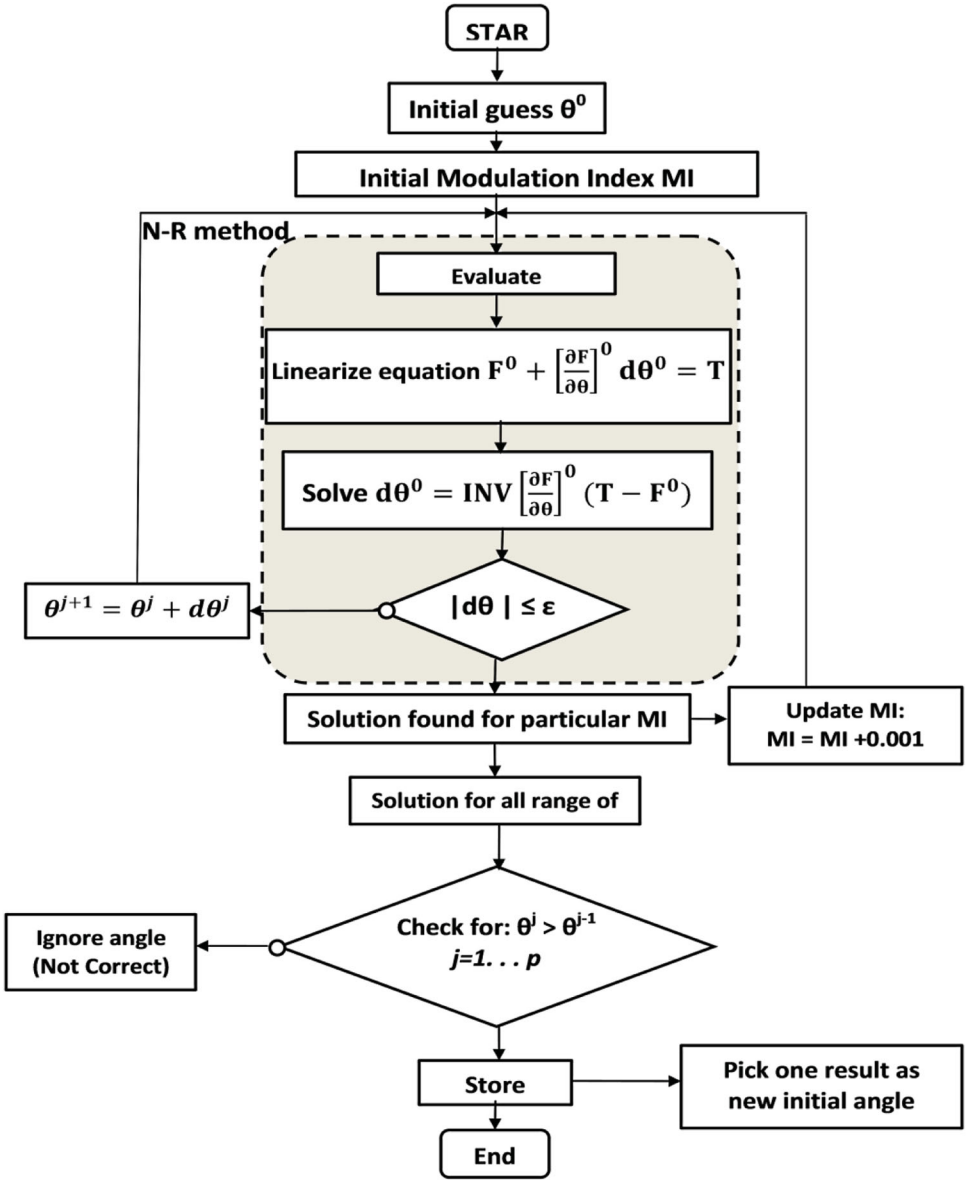

Figure 3. (a) Newton-Raphson flow chart of computer algorithm for solving the equation. (b) Genetic algorithm flowchart.

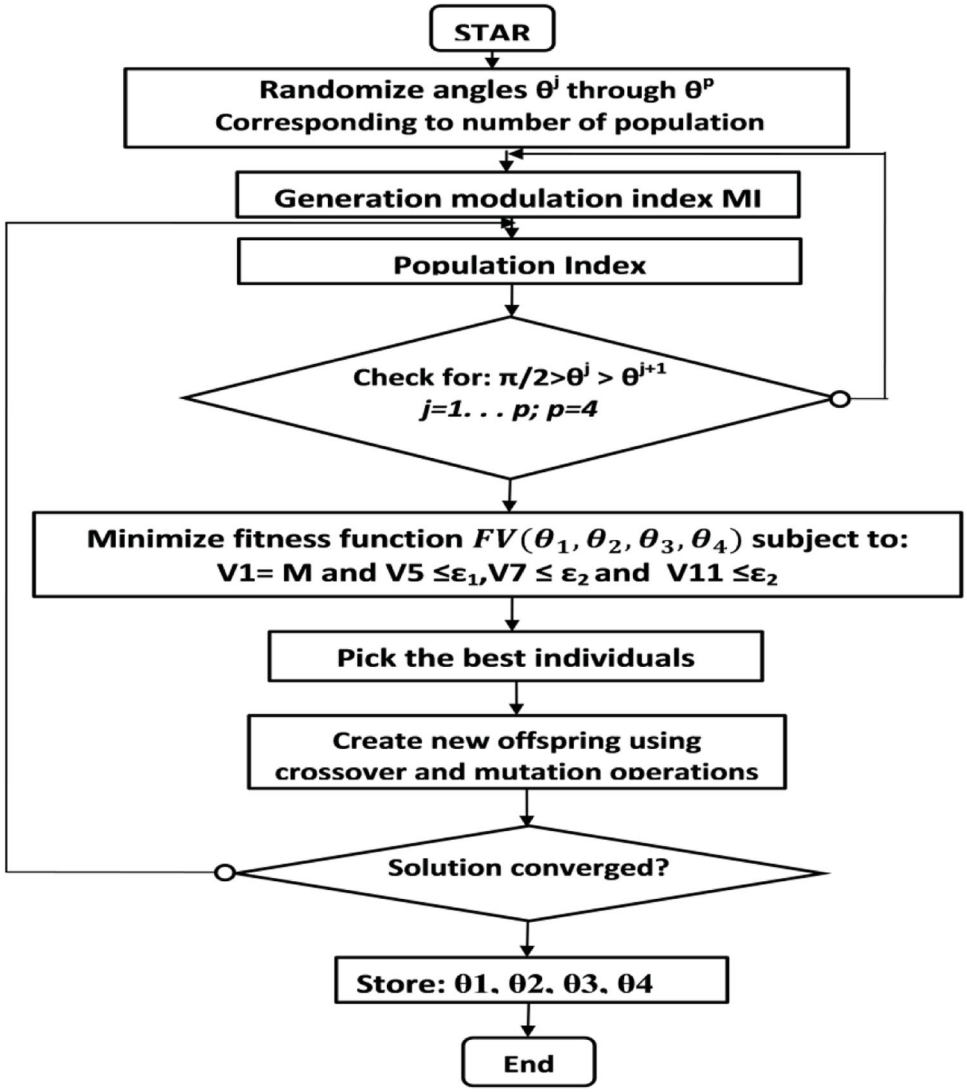

Figure 3. Continued.

3.3. ECSA analysis

ECSA is an algorithm for commutation cells' switching instant calculation to obtain an output voltage with the desired 9-level output voltage, which is studied in this paper. Indeed the calculated angles are with regular steps so that the difference between two successive angles is equal while obtaining the desired level, without taking into account lower order harmonics elimination that represents the most harmful harmonics on output voltage waveform. Considering this algorithm, THD is optimized by obtaining the desired number of levels as the number of levels that increases the THD of the output voltage is reduced while approaching to a sine waveform. Furthermore, ECSA algorithm allows optimizing THD without targeting lower order harmonic elimination, hence the difference between Newton-Raphson and GA. Indeed, 9-level inverter output voltage angles are quarter waveform symmetry. ECSA-based switching angles are as follows: $\theta_1 = \theta_2\text{-}\theta_1 = \theta_3\text{-}\theta_2 = \theta_4\text{-}\theta_3 = 2\ (\pi\ /2\text{-}\theta_4)$. In general, the p switching angles calculated based on ECSA are as follows: $\theta_1 = \theta_2\text{-}\theta_1 = \theta_3\text{-}\theta_2 = \ldots\ \theta_p\text{-}\theta_p\text{-}1 = 2\ (\pi/2\text{-}\theta_p)$.

4. Performance analysis and comparison between N-R, G-A and ECSA based on simulation results

In this section, 9-level asymmetrical CHB inverter control based on N-R, GA and ECSA is tested based on Matlab/Simulink. Since the hardware implementation is expensive, simulation phase is considered as a primary stage before hardware realization.

Optimized Harmonic Elimination Stepped Waveform (OHESW) technique was employed to improve output waveform quality. In this section, performances of NR, GA and ECSA are compared based on computed switching angle for 9-level asymmetrical CHB inverter control.

In equal calculated switching angle technique, harmonics 5, 7 and 11 are not taken into account to be eliminated. Furthermore, this technique is introduced

in comparison with N-R and G-A to show the necessity to use N-R and G-A in Optimized Harmonic Elimination Stepped Waveform (OHESW) techniques for THD minimization while improving inverter output voltage waveform quality. Figure 4(a,b) are obtained based on Matlab programming. These figures represent the graph drawn θ_1, θ_2, θ_3 and θ_4 set solution at various modulation index **r** based on N-R and G-A, respectively.

N-R technique returns all possible combinations of the switching angles for different r values based on MATLAB program. As a result, we can obtain a unique switching angle set solution for each modulation index r, $0.55 \leq r \leq 0.65$, $0.82 \leq r \leq 0.9$ and $0.92 \leq r \leq 1$. N-R does not provide any solution, as shown in Figure 4(a).

Figure 4(b) shows that the developed G-A optimization technique has successfully solved the SHE equations set for the entire range of **r** from 0 to 1 whereas it is not possible to find based on N-R technique. Set solutions θ_1, θ_2, θ_3 and θ_4 in degrees unit obtained by G-A are provided in Figure 4(b).

Asymmetrical cascaded 9-level commutation cells' control signals are obtained and provided in Figure 5(a–c). Theses control signal are based on the calculated switching angles θ_1, θ_2, θ_3 and θ_4.K1, K2, K3, K4, K5, K6, K7 and K8 that represent the control signals of the 9-level inverter commutation cells T_{11},T_{12},T_{13} T_{14} T_{21},T_{22},T_{23} and T_{24}, respectively. Control signal based on N-R algorithm and G-A is obtained by using Figure 4(a,b), respectively. Modulation index is chosen to be equal to 1 ($r = 1$). As a result, the four switching angles obtained by N-R algorithm are $\theta_1 = 10.01°$, $\theta_2 = 22.14°$, $\theta_3 = 40.75°$, $\theta_4 = 61.75°$ and those obtained based on G-A are $\theta_1 = 26.05°$, $\theta_2 = 34.21°$, $\theta_3 = 44.83°$ and $\theta_4 = 52.63°$.

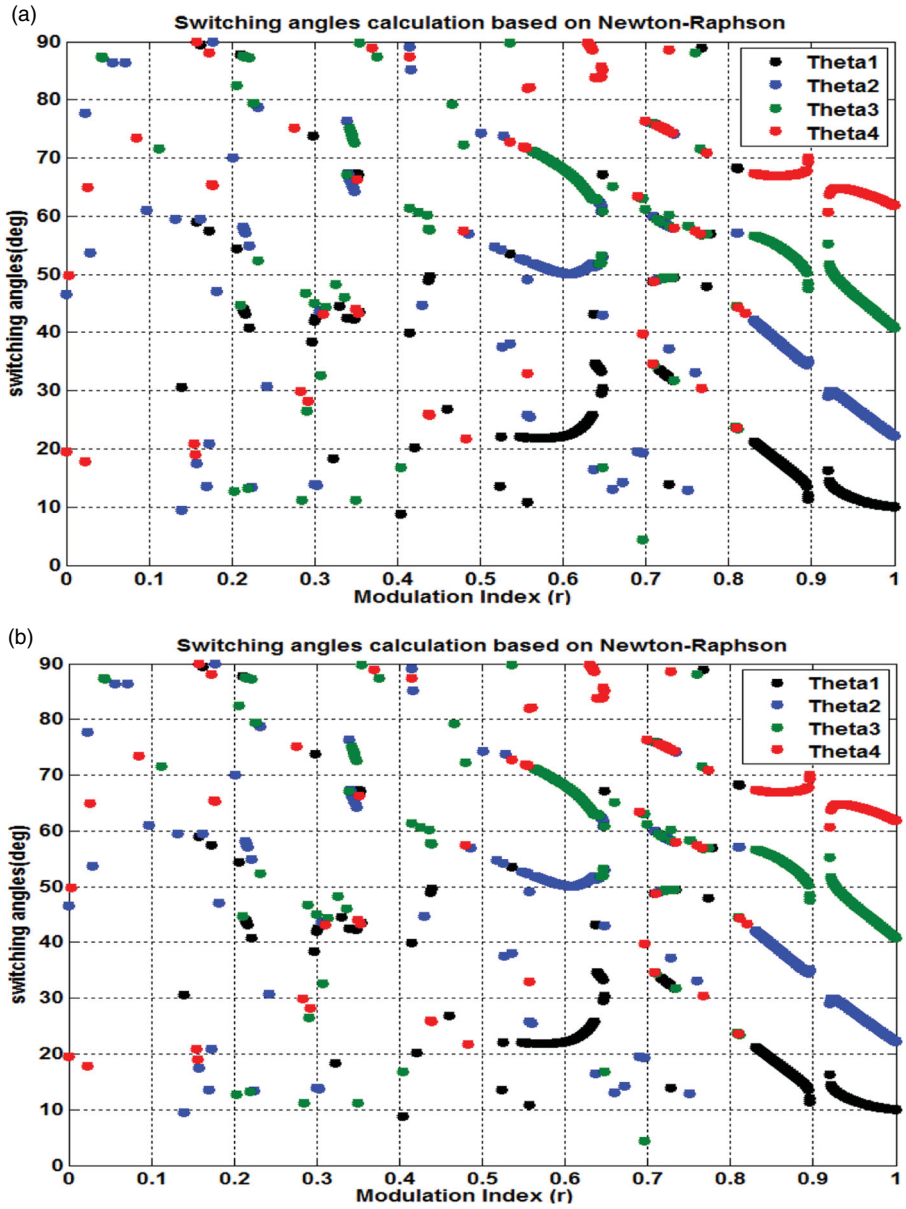

Figure 4. (a). Switching angles versus modulation index based on Newton-Raphson technique. (b). Switching angles versus modulation index based on Genetic Algorithm.

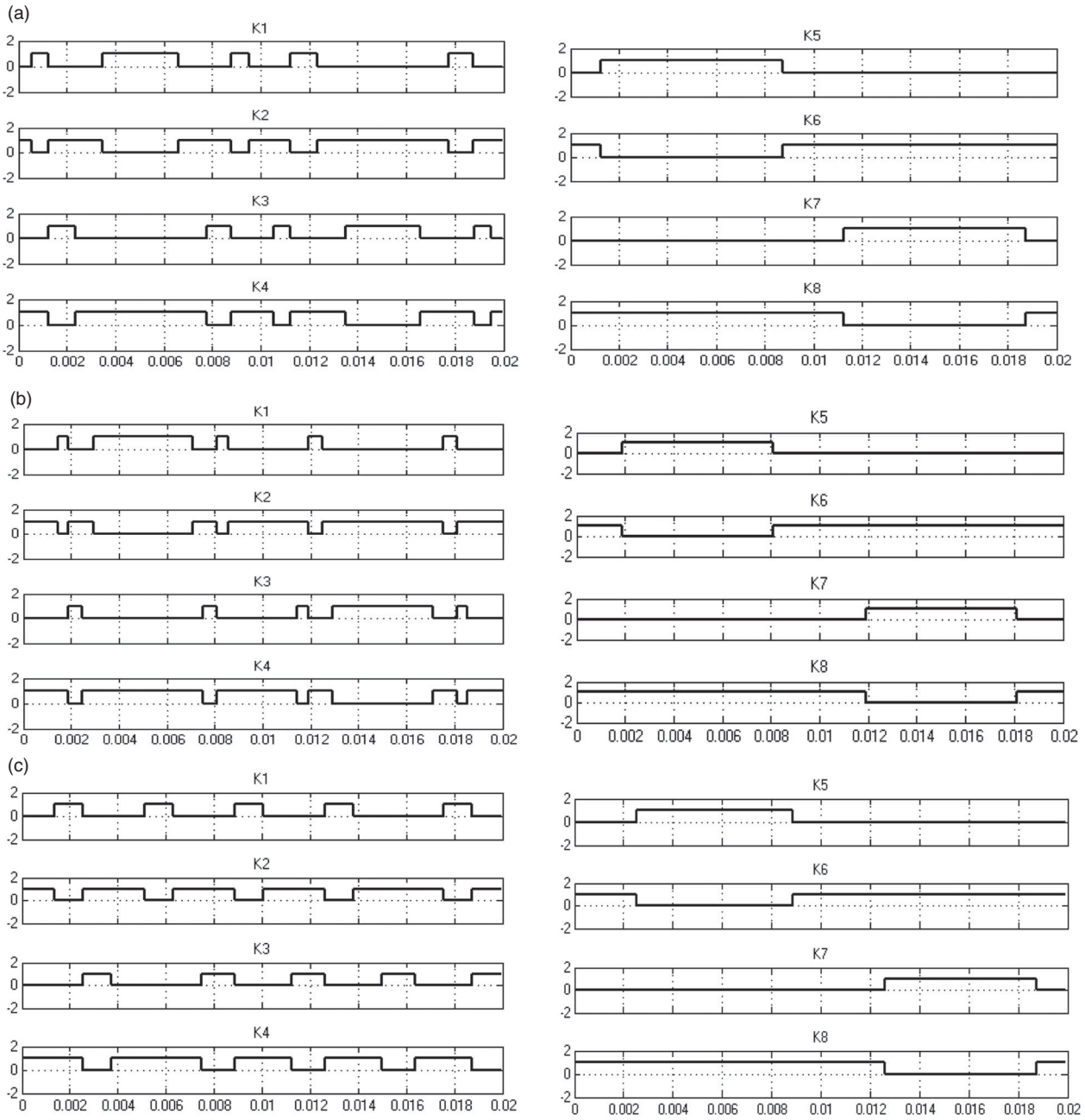

Figure 5. (a) Asymmetrical 9-level inverter control signals based on N-R. (b) Asymmetrical 9- level inverter control signals based on G-A. (c) Asymmetrical 9-level inverter control signals based on ECSA.

Switching angles based on ECSA are obtained such as $\theta_1 = \theta_2\text{-}\theta_1 = \theta_3\text{-}\theta_2 = \theta_4\text{-}\theta_3 = 2(\pi/2 - \theta_4)$, which gives: $\theta_1 = 20°$, $\theta_2 = 40°$, $\theta_3 = 60°$ and $\theta_4 = 80°$. To verify the results obtained above, we presented, in Figure 5(a–c), the simulation results of the 9-level inverter commutation cell signal control based on N-R, G-A and ECSA, respectively.

Inverter commutation control signals ON state and OFF state, respectively, are chosen to obtain the desired number of levels, equal to nine, as shown in Figure 6. On the other hand, commutation cell state duration depends on the switching angles solution obtained. These durations are provided as the interval form in terms of switching angles θ_1, θ_2, θ_3 and θ_4. Switching angle intervals are provided in Table 2. Figure 6 and Table 2 provide for each selected state its equivalent output voltage level and its corresponding interval duration according to switching angles.

To check the control signals obtained above based on N-R algorithm, GA and ECSA and to compare algorithm accuracy based on calculated switching angles, signal controls are applied to control a single-phase asymmetrical cascaded 9-level inverter. This inverter is used to drive R-L load (R = 10 Ω, L = 0.5 mH) such as the first HB inverter unit (HB1) and the second HB inverter unit (HB2) DC source voltages are Vdc1 = E = 20 V and Vdc2 = 3E = 60 V, respectively. By using Matlab/Simulink, asymmetrical cascaded 9-level inverter simulation output voltage and

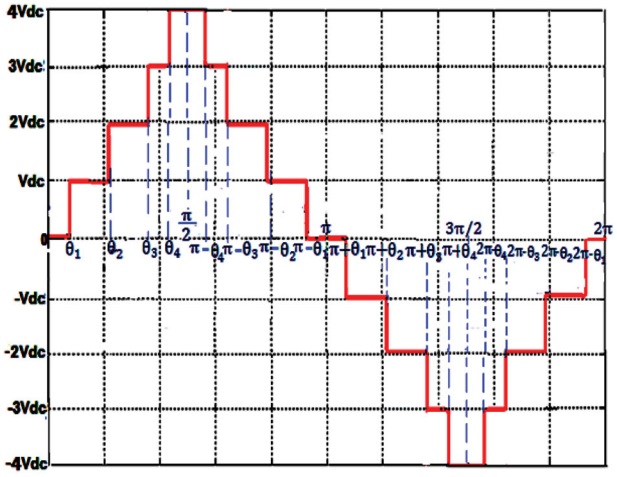

Figure 6. Inverter output voltage levels according to switching angles.

its FFT analysis, based on N-R, G-A and ECSA, are depicted in Figures 7–9(a,b), respectively.

From the spectrum analysis, we can see clearly that the THD obtained by N-R is equal to 10.20%; however, for those obtained, based on G-A and Equal Calculated Switching Angles, are equal to 14.22% and 18.16, respectively. In Figure 7(b), where N-R algorithm is adopted, it is clearly identified that the 5th, 7th and the 11th harmonics are completely eliminated. This result explains the significant improvement in harmonic profile achieved by the N-R based approach. Compared to the results obtained in Figure 8(a,b), when switching angles solution are based on G-A algorithm, harmonics 5, 7 and 11 are not completely eliminated, reflecting a higher THD and an output voltage waveform quality is slightly better than that obtained based on the N-R technique. Figure 9(a,b) represent the 9-level inverter output voltage and its FFT analysis, obtained based on the ECSA technique. Figure 9(b) reveals harmonics 5, 7 and 11 in its entirety, because the THD is higher than that obtained by N-R and G-A. Hence a poor quality of the output voltage waveform compared to those obtained by N-R and G-A. N-R-based simulation results present better performance than those obtained by G-A and ECSA. Accuracy of the calculated switching angles by each algorithm made the difference between the performances. Switching angle solutions provided by Newton-Raphson are more accurate than those provided by GA and ECSA, because lower order harmonics 5, 7 and 11 are completely removed in the case of N-R-based selective harmonic elimination control.

Table 2. Inverter 9-level output voltage according to switching states.

	CHB1 commutation cells				CHB2 commutation cells					
State	T11	T12	T13	T14	T21	T22	T23	T24	Output voltage VAO Level	Subinterval
1	Off	On	Off	On	Off	On	Off	On	0	$[0\ \theta_1]$
2	On	Off	Off	On	Off	On	Off	On	$Vdc1 = +Vdc$	$[\theta_1\ \theta_2]$
3	Off	On	On	Off	On	Off	Off	On	$Vdc2 - Vdc1 = +2Vdc$	$[\theta_2\ \theta_3]$
4	Off	On	Off	On	On	Off	Off	On	$Vdc2 = 3Vdc$	$[\theta_3\ \theta_4]$
5	On	Off	Off	On	On	Off	Off	On	$Vdc1 + Vdc2 = 4Vdc1 = 4Vdc$	$[\theta_4\ \pi\text{-}\theta_4]$
6	Off	On	Off	On	On	Off	Off	On	$Vdc2 = +3Vdc$	$[\pi\text{-}\theta_4\ \pi\text{-}\theta_3]$
7	Off	On	On	Off	On	Off	Off	On	$Vdc2 - Vdc1 = +2Vdc$	$[\pi\text{-}\theta_3\ \pi\text{-}\theta_2]$
8	On	Off	Off	On	Off	On	Off	On	$Vdc1 = +Vdc$	$[\pi\text{-}\theta_2\ \pi\text{-}\theta_1]$
9	Off	On	Off	On	Off	On	Off	On	0	$[\pi\text{-}\theta_1\ \pi+\theta_1]$
10	Off	On	On	Off	Off	On	On	Off	$-Vdc1 = -Vdc$	$[\pi+\theta_1\ \pi+\theta_2]$
11	On	Off	Off	On	Off	On	On	Off	$Vdc1 - Vdc2 = -2Vdc$	$[\pi+\theta_2\ \pi+\theta_3]$
12	Off	On	Off	On	Off	On	On	Off	$-Vdc2 = -3Vdc$	$[\pi+\theta_3\ \pi+\theta_4]$
13	Off	On	On	Off	Off	On	On	Off	$-Vdc1-Vdc2 = -4Vdc1 = -4Vdc$	$[\pi+\theta_4\ 2\pi\text{-}\theta_4]$
14	Off	On	Off	On	Off	On	On	Off	$-Vdc2 = -3Vdc$	$[2\pi\text{-}\theta_4\ 2\pi\text{-}\theta_3]$
15	On	Off	Off	On	Off	On	On	Off	$Vdc1 - Vdc2 = -2Vdc$	$[2\pi\text{-}\theta_3\ 2\pi\text{-}\theta_2]$
16	Off	On	On	Off	Off	On	Off	On	$-Vdc1 = -Vdc$	$[2\pi\text{-}\theta_2\ 2\pi\text{-}\theta_1]$
17	Off	On	Off	On	Off	On	Off	On	0	$[2\pi\text{-}\theta_1\ 2\pi]$

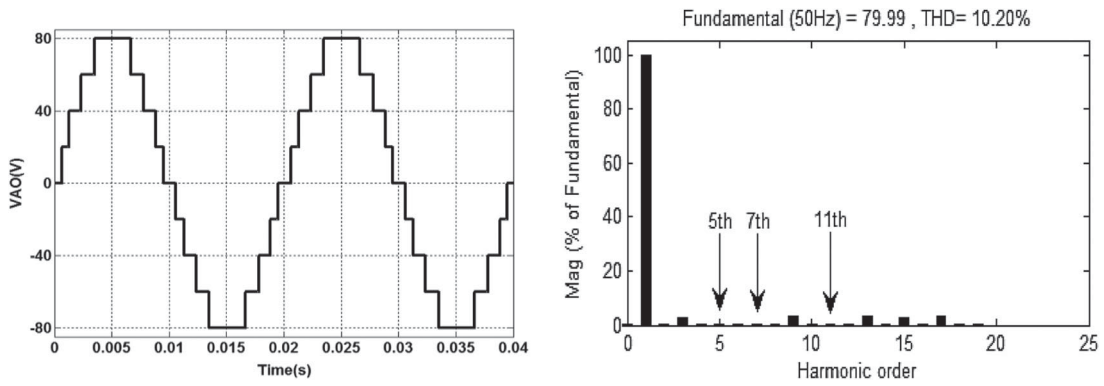

Figure 7. (a) Single-phase 9-level inverter output voltage wave form (VAO) based on N-R. (b) FFT analysis of the 9-level output voltage waveform (VAO) based on N-R Algorithm.

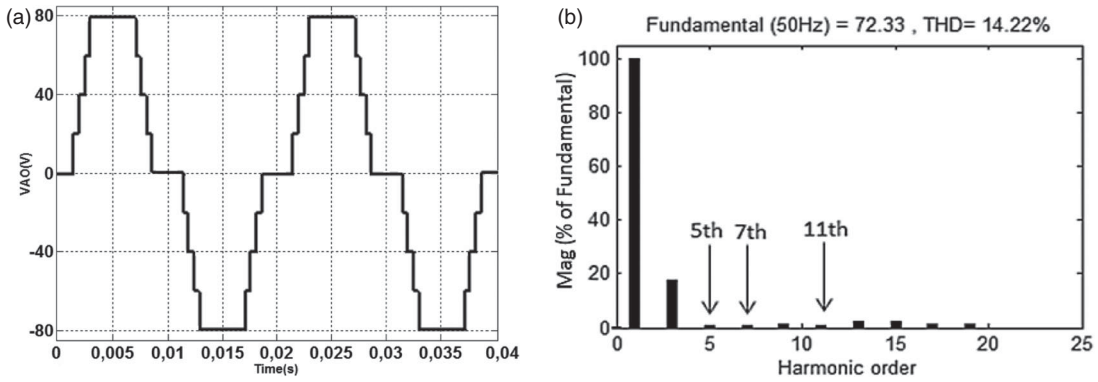

Figure 8. (a) Single-phase 9-level inverter output waveform based on G-A. (b) FFT analysis of the l 9-level output voltage waveform (VAO) based on G-A.

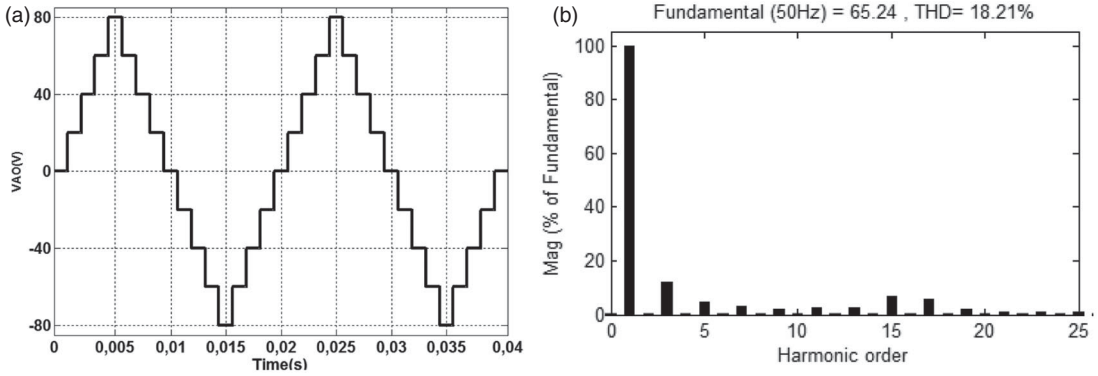

Figure 9. (a) Single-phase 9-level inverter output voltage waveform based on ECSA. (b) FFT analysis of the l 9-level output voltage waveform (VAO) based on ESCA.

5. Experimental results

Power circuit is a single-phase asymmetrical cascaded inverter, designed to provide a 9-level output voltage. The prototype inverter is constituted by connecting in series 2 single-phase H Bridge unit inverters (HB1 and HB2) using the MOSFET (IRF540NPBF) as switching devices and HB1 and HB2 DC source voltages Vdc1 and Vdc2 are unequal such as Vdc2 = 3Vc1. As given in Figure 10, this low power asymmetrical cascaded 9-level inverter has been developed to verify the feasibility of the proposed strategy and confirm the validity of the simulation and theoretical findings. HB1 and HB2 DC source voltage values are chosen such as Vdc1 = E = 20 V and Vdc2 = 3E = 60 V. Asymmetrical cascaded 9-level inverter is used to drive a digital R-L load ($R = 10\Omega$, $L = 0.5$ mH), such as output voltage frequency: $f = 50$ Hz, switching frequency $f_c = r^*f = 1^*50 = 50$ Hz. Inverter output voltage maximal value: $V_{AOmax} = 4E = 80$ V. Inverter output voltage fundamental component RMS value: $V_{AOfundamentalRMS} = 16E/(\pi\sqrt{2}) = 72$ V, load current RMS value = 4.58A and apparent power value S = 330VA.

The digital implementation of control strategy is done around the development of ALTERA-Cyclone II 100 MHz clock frequency FPGA card and VHDL code is written and synthesized using QUARTUS II 13.0 and Model SIM-Intel FPGA 10.5b software.

The FPGA generates eight control signals K1 to K8 of magnitude 0 and 3.3 V, through FPGA pins H3, L7, K6, G3, G1, J7, J6 and K4. FPGA-based control signals are sent to inverter commutation cells gate via integrated protection circuit to prevent the ground sharing between FPGA and power circuit represented by the H-Bridge module. Circuit protection solution provided in Figure 10 is based on a 4N25 opto-isolator circuit. 4N25 is able to isolate the power circuit from control circuit represented by FPGA. FPGA control signals are sent to the inverter power switch via 4N25 circuit, as shown in Figure 10. Furthermore, MOSFET gates require a signal control of magnitude equal to 12 V. A risk of a short circuit is highly probable when controlling two switches of the same arm with complementary control signals. Hence, a circuit is able to provide control signals with 12 V magnitudes, while avoiding short circuit problems between two complementary control signals is strongly recommended. As shown in Figure 10, a circuit driver based on IR2110 is able to amplify the weak signals generated by the PFGA and to introduce a necessary dead time in control systems to avoid the arms inverter short circuits.

Inverter commutation cell control signal generated by FPGA is programmed once switching angles in

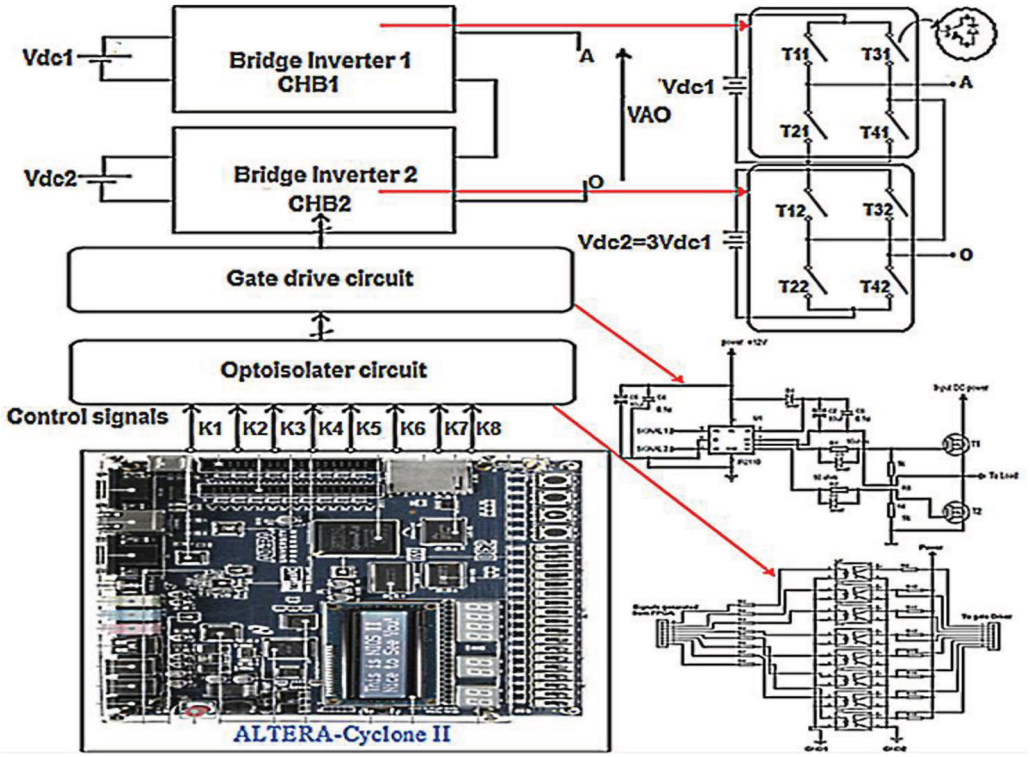

Figure 10. Block diagram of asymmetrical cascaded 9-level inverter using FPGA.

unit degree are obtained and calculated based on Matlab. Thereafter, these angles must be converted into equivalent FPGA clock cycle number to be implemented in FPGA. There are two steps to follow to convert angles from unit degree to the clock cycle number. Knowing that the control signal period is equal to $T = (1/f) = 0.02$s, and for chosen modulation index $r = 1$, switching angles obtained based on Newton-Raphason are $\theta_1 = 10.01°$, $\theta_2 = 22.14°$, $\theta_3 = 40.75°$, $\theta_4 = 61.75°$ and those obtained based on G-A are $\theta_1 = 26.05°$, $\theta_2 = 34.21°$, $\theta_3 = 44.83°$ and $\theta_4 = 52.63°$. Switching angles based on ECSA are obtained such as $\theta_1 = \theta_2\text{-}\theta_1 = \theta_3\text{-}\theta_2 = \theta_4\text{-}\theta_3 = 2(\pi/2 - \theta_4)$, which gives: $\theta_1 = 20°$, $\theta_2 = 40°$, $\theta_3 = 60°$ and $\theta_4 = 80°$. In this case, the first step is to convert interval range, given in Table 3, representing state pulse width from degree unit to time domain (second). Subinterval range, respectively width pulse $\Delta\theta(°)$ in degree unit, is calculated as

$$\Delta\theta_i(^\circ) = \theta_{up(i)}(^\circ) - \theta_{low(i)}(^\circ) \tag{27}$$

where $\theta_{\text{up(i)}}(°)$ and $\theta_{\text{low(i)}}(°)$ are subinterval (i) upper and lower bound, respectively, with $i = 1 \ldots 17$, as given in Table 2. As a result, conversion equation is given by

$$\Delta\theta_i(\text{second}) = \frac{\Delta\theta_i(^\circ) * T}{360^\circ} \tag{28}$$

Table 3. Control signals width unit conversion.

State $i = 1 \ldots 17$	Subinterval	Subinterval range $\Delta\theta(°)$	NR P.W (°)	GA P.W (°)	ECSA P.W (°)	NR P.W (ms)	GA P.W (ms)	ECSA P.W (ms)	NR TM_i (Cyclesnumber)	GA TM_i (Cyclesnumber)	ECSA TM_i (Cycles number)
1	$[0\ \theta_1]$	$\theta 1$	10.01	26.05	20	0.5561	1.4472	1.1111	55611	144722	111111
2	$[\theta_1\ \theta_2]$	$\theta_2\text{-}\theta_1$	12.14	8.16	20	0.6744	0.4533	1.1111	67444	45333	111111
3	$[\theta_2\ \theta_3]$	$\theta_3\text{-}\theta_2$	18.1	10.62	20	1.0055	0.5900	1.1111	100555	59000	111111
4	$[\theta_3\ \theta_4]$	$\theta_4\text{-}\theta_3$	21	7.8	20	1.1666	0.4333	1.1111	116666	43333	111111
5	$[\theta_4\ \pi\text{-}\theta_4]$	$\pi\text{-}2\theta_4$	56.5	74.74	20	3.1388	4.1522	1.1111	313888	415222	111111
6	$[\pi\text{-}\theta_4\ \pi\text{-}\theta_3]$	$\theta_4\text{-}\theta_3$	21	7.8	20	1.1666	0.4333	1.1111	116666	43333	111111
7	$[\pi\text{-}\theta_3\ \pi\text{-}\theta_2]$	$\theta_3\text{-}\theta_2$	18.1	10.62	20	1.0055	0.5900	1.1111	100555	59000	111111
8	$[\pi\text{-}\theta_2\ \pi\text{-}\theta_1]$	$\theta_2\text{-}\theta_1$	12.14	8.16	20	0.6744	0.4533	1.1111	67444	45333	111111
9	$[\pi\text{-}\theta_1\ \pi\text{+}\theta_1]$	$2\,\theta_1$	20.02	52.1	40	1.1122	2.8944	2.2222	111222	289444	222222
10	$[\pi\text{+}\theta_1\ \pi\text{+}\theta_2]$	$\theta_2\text{-}\theta_1$	12.14	8.16	20	0.6744	0.4533	1.1111	67444	45333	111111
11	$[\pi\text{+}\theta_2\ \pi\text{+}\theta_3]$	$\theta_3\text{-}\theta_2$	18.1	10.62	20	1.0055	0.5900	1.1111	100555	59000	111111
12	$[\pi\text{+}\theta_3\ \pi\text{+}\theta_4]$	$\theta_4\text{-}\theta_3$	21	7.8	20	1.1666	0.4333	1.1111	116666	43333	111111
13	$[\pi\text{+}\theta_4\ 2\pi\text{-}\theta_4]$	$\pi\text{-}2\theta_4$	56.5	74.74	20	3.1388	4.1522	1.1111	313888	415222	111111
14	$[2\pi\text{-}\theta_4\ 2\pi\text{-}\theta_3]$	$\theta_4\text{-}\theta_3$	21	7.8	20	1.1666	0.4333	1.1111	116666	0.4333	111111
15	$[2\pi\text{-}\theta_3\ 2\pi\text{-}\theta_2]$	$\theta_3\text{-}\theta_2$	18.1	10.62	20	1.0055	0.5900	1.1111	100555	59000	111111
16	$[2\pi\text{-}\theta 2\ 2\pi\text{-}\theta 1]$	$\theta 2\text{-}\theta 1$	12.14	8.16	20	0.6744	0.4533	1.1111	67444	45333	111111
17	$[2\pi\text{-}\theta_1\ 2\pi]$	θ_1	10.01	26.05	20	0.5561	1.4472	1.1111	55611	144722	111111

P.W: Pulse Width.

Table 4. Correspondence between FSM stage and CHB inverter control signals.

FMS	CHB1 commutation cells				CHB2 commutation cells			
P_0	0	1	0	1	0	1	0	1
P_1	1	0	0	1	0	1	0	1
P_2	0	1	1	0	1	0	0	1
P_3	0	1	0	1	1	0	0	1
P_4	1	0	0	1	1	0	0	1
P_5	0	1	0	1	1	0	0	1
P_6	0	1	1	0	1	0	0	1
P_7	1	0	0	1	0	1	0	1
P_8	0	1	0	1	0	1	0	1
P_9	0	1	1	0	0	1	1	0
P_{10}	1	0	0	1	0	1	1	0
P_{11}	0	1	0	1	0	1	1	0
P_{12}	0	1	1	0	0	1	1	0
P_{13}	0	1	0	1	0	1	1	0
P_{14}	1	0	0	1	0	1	1	0
P_{15}	0	1	1	0	0	1	0	1
P_{16}	0	1	0	1	0	1	0	1
P_{17}	0	1	0	1	0	1	0	1

Once control signal widths are converted to time domain, the second step is to convert them to FPGA clock cycle number TM to be programmed thereafter into FPGA to generate inverter control signals. Knowing that FPGA frequency clock is $f_{clk} = 100\,\text{MHz}$ corresponding to a Period Clock $T_{clk} = 1/f_{clk} = 10^{-5}\,\text{ms}$.

The following equation describes conversion from degree to T_{clk} cycle number designed per TM provided by FPGA counter.

$$\text{TM}_i = \text{FPGA clock cycle number} = \frac{\Delta\theta_i(\text{second})}{T_{clk}} \tag{29}$$

Considering subinterval range according to switching angles, Table 3 provides control signal width conversion obtained based on NR, GA and ECSA from

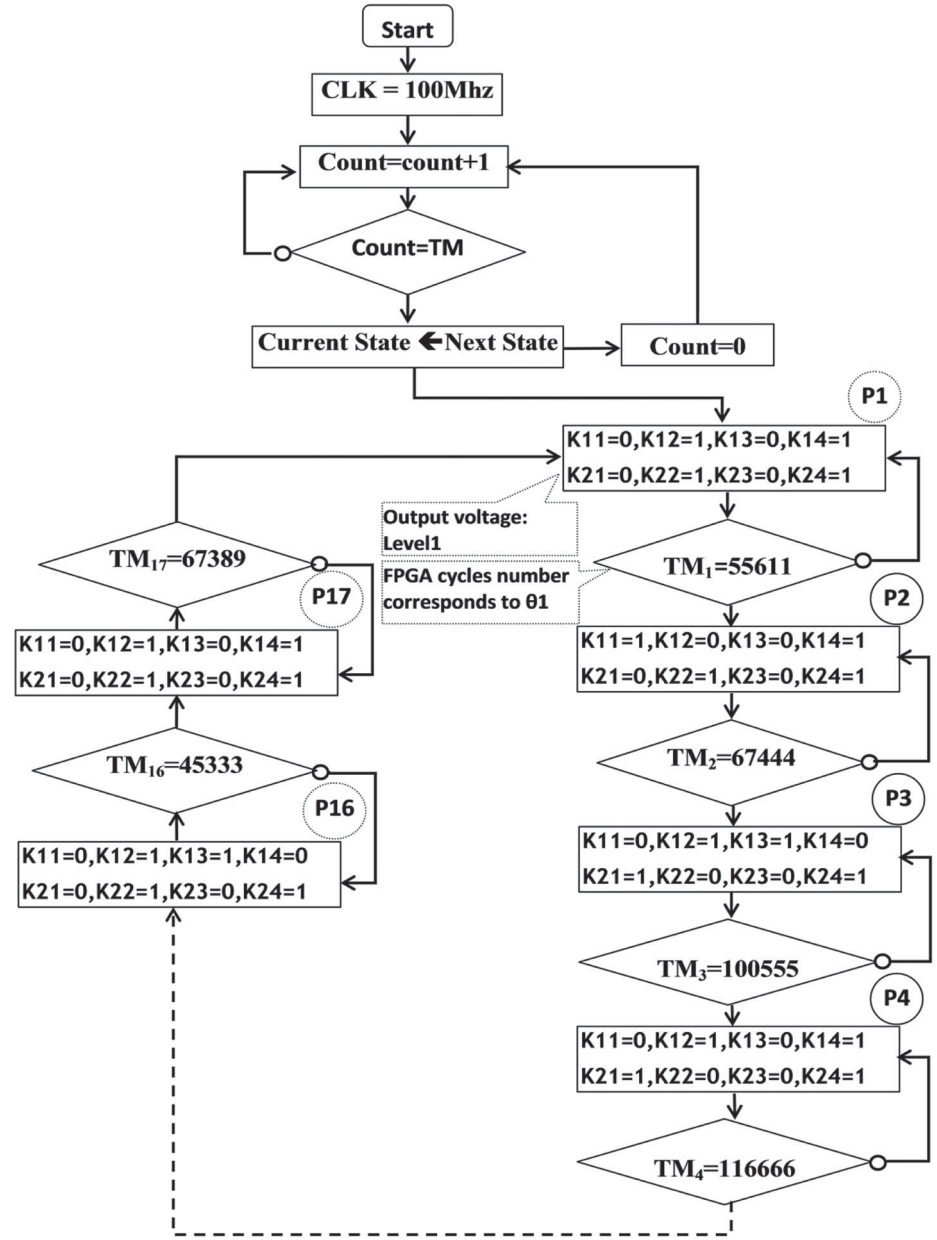

Figure 11. Flowchart of Newton-Raphson control signal generation based on FPGA.

Table 5. Comparison of inverter output voltage THD between simulation and experiment.

Technique	Output waveform THD		
	Simulation	Experiment	THD error
Newton-Raphson (N-R)	10.20%	10.9%	0.7%
Genetic Algorithm (G-A)	14.22%	14.8%	0.58%
Equal Calculating Switching Angles (ECSA)	18.21%	20.1%	1.89%

degree to FPGA cycle number TM, to be programmed thereafter and implemented in FPGA

Therefore,each inverter control signal can take during its width the logic states "0" or "1", depending on the level of voltage to be obtained based on Table 1 results. Once the impulses in unit degree are converted to FPGA clock cycle number, the next step in the design is to choose a method to implement control signals into FPGA. It was decided that the best way to generate control signals is to program a finite state machine (FSM) using FPGA.

The FSM-based design is made up of 17 states represented in Table 2. FSM is given with 17 states considered from P1 to P17 to generate control signals. P1 to P17 represents subinterval 1 to subinterval 17, respectively, given in Tables 2 and 3, such as one state for every subinterval i.e. one state for each output level for one period of the inverter output waveform.

Duration of state is given in Table 3 as a number of FPGA clock cycles TM_i. As a result, FSM changes from one state to the next according to FPGA signal control states K1, K2, K3, K4 and K5, K6, K7, K8 of CHB1 and CHB2 commutation cells T11, T12, T13, T14 and T21, T22, T23, T24, respectively. Generally, FSM sate stage with the control signal of logical value "1" means that the corresponding commutation cells will be in "ON" state, otherwise the states carrying the value logic "0" mean that the corresponding commutation cells will be in "OFF" state. Once the program is loaded into the FPGA, FPGA acts as a controller and gating pulses generator by sending the control signals to the inverter power switches.

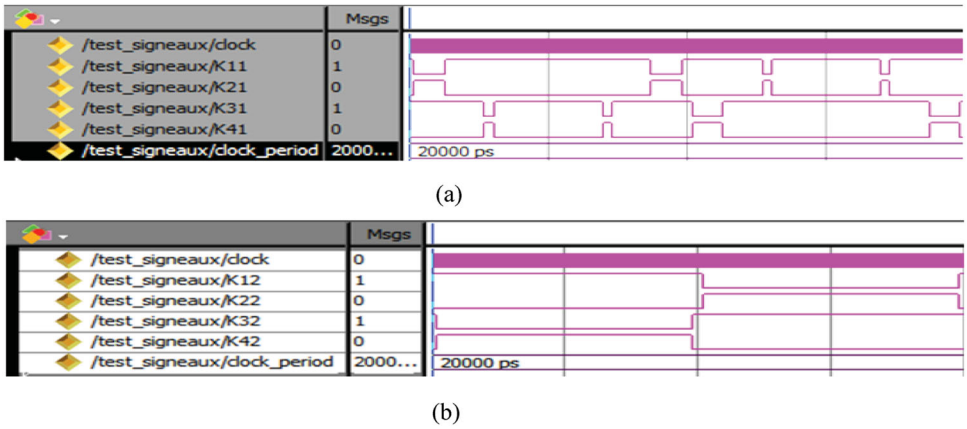

Figure 12. VHDL test bench simulation of the control signals for asymmetrical 9-level invert, $r = 1$: (a) HB1, (b) HB 2.

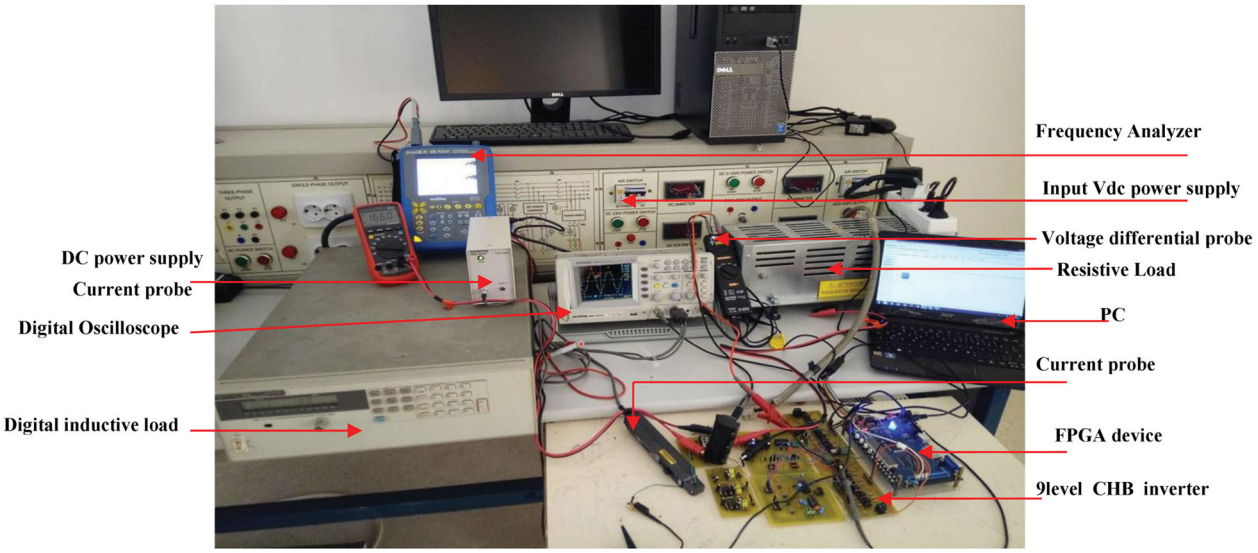

Figure 13. Photograph of the experimental prototype of the single-phase asymmetrical cascaded 9-level inverter.

Table 4 summarizes inverter commutation cells states during one cycle, given as FMS $P_{i=1..17}$ stage state that can be taken in the case of NR, GA and ESA-based solving. In this regard, for every stage Pi, NR, GA and ECSA are the same control signal states, only TM_i of each stage changes from one algorithm to another.

TM_i, given in the flowchart of Figure 11, represents the state Pi ($i = 1 \ldots 17$) duration, given as FPGA

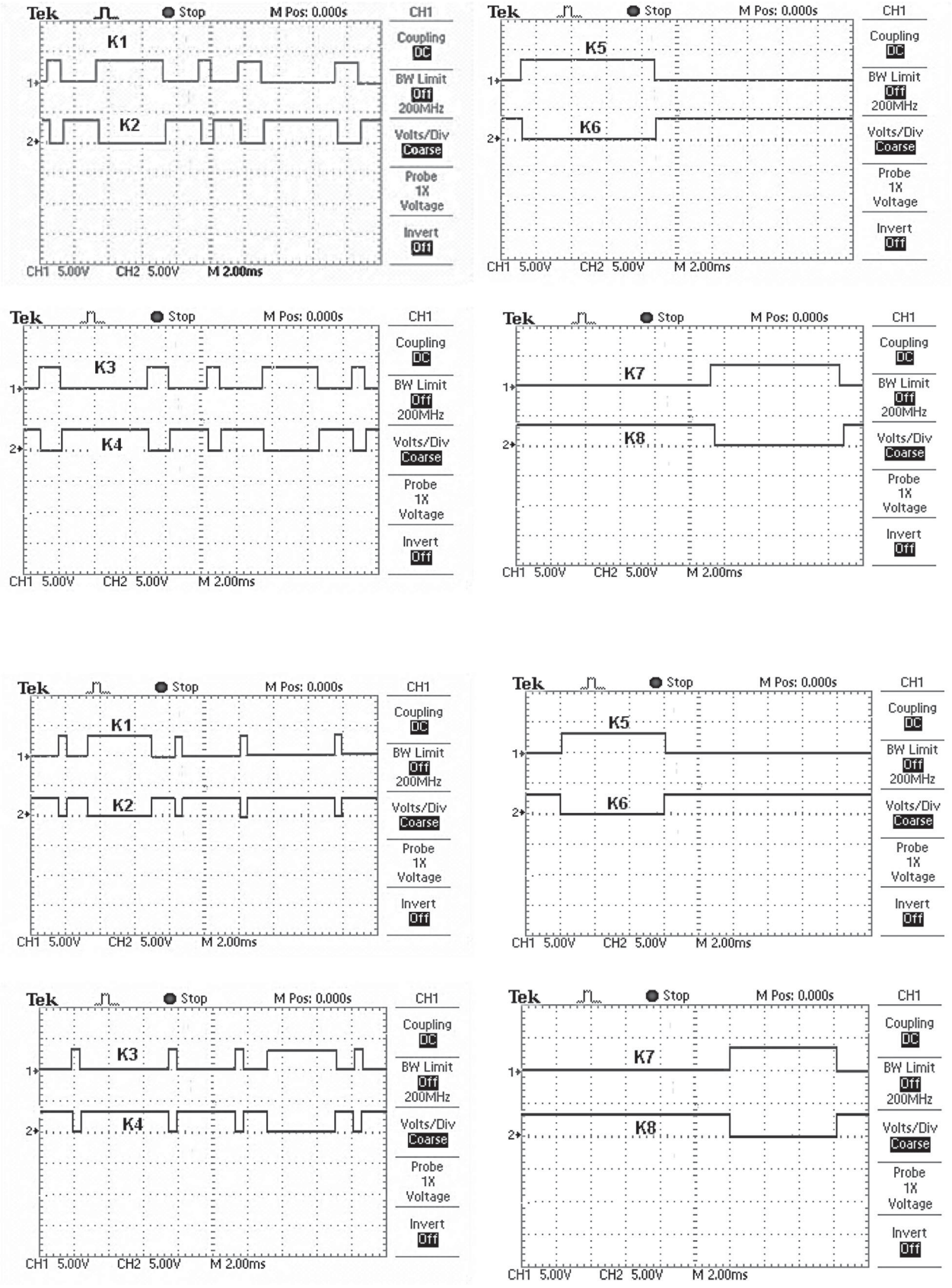

Figure 14. (a) Asymmetrical 9-level inverter control signals based on N-R generated by FPGA. (b) Asymmetrical 9-level inverter control signals based on G-A generated by FPGA. (c) Asymmetrical 9-level inverter control signals based on ECSA generated by FPGA.

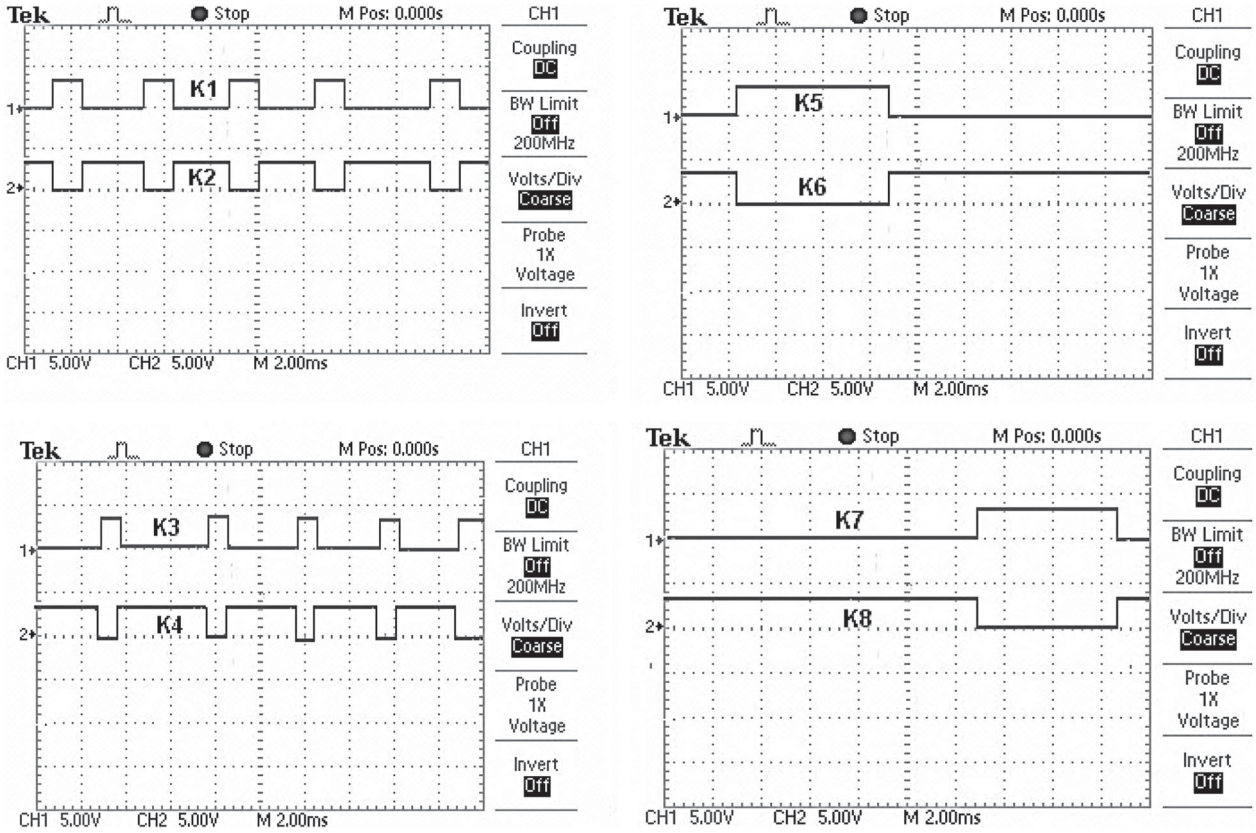

Figure 14. Continued.

cycle number and provided by a developed VHDL subprogram divider frequency counter. Every state Pi represents inverter commutation cell control signals states, corresponding to the sub-interval i of Table 2, to be sent thereafter to inverter power switches. The passage from one level to the next, respectively, from one inverter commutation cell states to the following state is under the condition that the number of FPGA cycles TM dedicated for the considered state is achieved, otherwise the level is maintained. Figure 11 represents the flow chart for generating inverter switching control signals obtained by Newton-Raphson algorithm.

Pi: represents inverter commutation cell states given in the line i of Table 5.

TMi: the number of FPGA clock cycles given in Table 3.

The output gating signal can be observed in digital storage oscilloscope (DSO), as given in Figure 12, where gating signals are generated based on N-R algorithm.

Figure 12 represents NR-based signal control simulation results while using ISE design tools. Signal control simulation results, provided in Figure 12, are given for one period T = 20 ms (f = 50 Hz) to eliminate harmonics 5, 7 and 11.

As for the simulation test, the digital implementation of the control strategy is done on a SPARTAN-6 FPGA, for modulation index $r = 1$ and switching angles obtained by: N-R: $\theta_1 = 10.01$, $\theta_2 = 22.14$, $\theta_3 = 40.75$, $\theta_4 = 61.75$, G-A algorithm: $\theta_1 = 26.05$, $\theta_2 = 34.21$, $\theta_3 = 44.83$ and $\theta_4 = 52.63$.and ECSA: $\theta_1 = 20°$, $\theta_2 = 40°$, $\theta_3 = 60°$ and $\theta_4 = 80°$.

Figure 13 shows the realized experimental set-up to test the gating signals obtained by N-R, G-A and ECSA and implemented in FPGA.

Figure 14(a–c) represent switching pulses obtained by NR, GA and ECSA, respectively, and generated by FPGA. Switching pulses are sent first to an opto-isolator circuit before being applied to driver circuit-based pulse amplifiers. Therafter, amplified pulses are sent to the proposed 9-level CHB inverter commtation cells.

The experimental result of the asymmetrical cascaded 9-level inverter output voltage and its FFT analysis, based on N-R algorithm, are given by Figure 15(a,b), respectively. This result confirms simulation results and NR accuracy to eliminate completely lower order harmonics.

Experimental CHB inverter output voltage and its FFT analysis, based on GA, are presented by Figure 16(a,b), respectively. Experimental CHB inverter output voltage and its FFT analysis, based on ECSA technique, are presented by Figure 17(a,b), respectively.

Among the results, THD = 10.9%, obtained based on NR, represents smaller rate than those obtained by GA and ECSA. Furthermore, the output voltage FFT analysis result obtained by GA, given by Figure 16(b), shows that harmonics 5, 7 and 11 are not completely eliminated. This result confirms the comparison

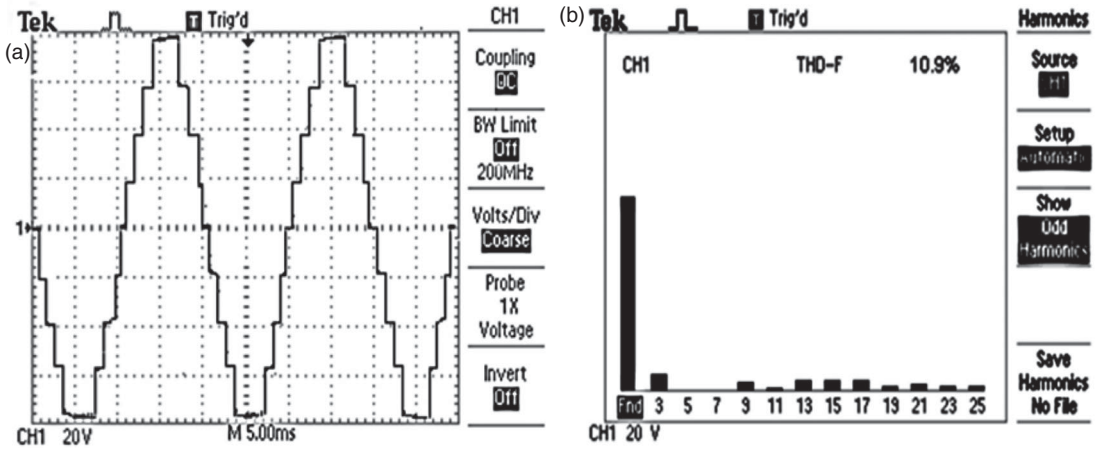

Figure 15. (a) Experimental result of the phase asymmetrical 9-level inverter output voltage based on N-R algorithm. (b) FFT analysis of the experimental 9-level inverter output voltage based on N-R.

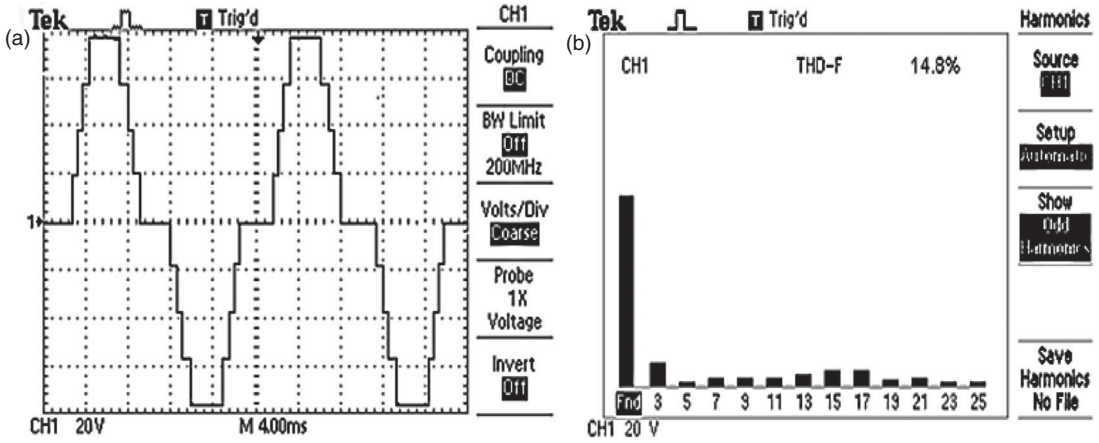

Figure 16. (a) Experimental result of the phase asymmetrical 9-level inverter output voltage based on GA. (b) FFT analysis of the experimental 9-level inverter output voltage based on GA.

obtained in simulation results and proves once again the efficiency and accuracy of N-R compared with G-A to eliminate completely harmonics 5, 7 and 11. In this regard, ECSA provides a higher harmonic rate than those obtained by both N-R and G-A. This rate is explained by the absence of optimization technique to eliminate lower harmonic orders. Hence, harmonics of 5, 7 and 11 are not eliminated, leading to an output voltage waveform with a poor quality Figure 17(a,b) confirm the important role that plays optimization algorithm, especially NR to reduce harmonic distortion (THD) by eliminating completely harmonics. Hence, the experimental results agree well with the simulation ones, as depicted in Table 2, with slight deviations.

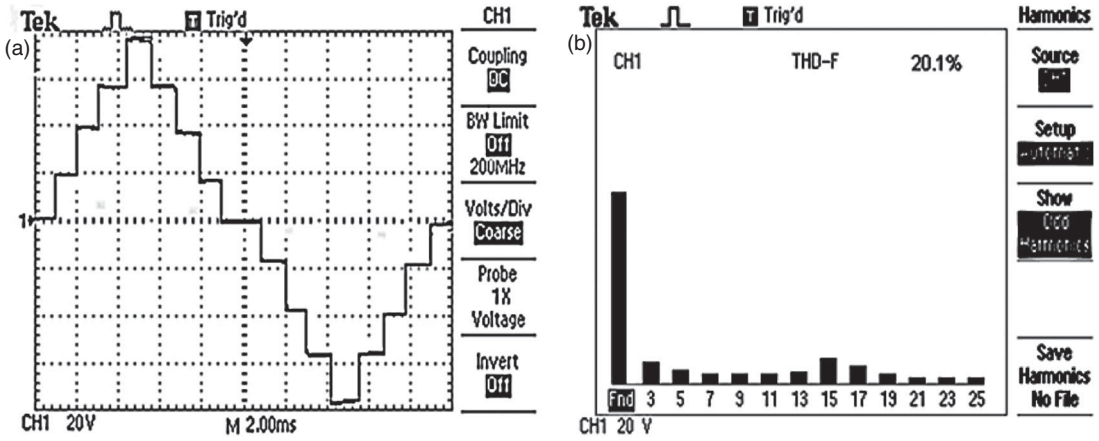

Figure 17. (a) Experimental result of the phase asymmetrical 9-level inverter output voltage based on ECSA algorithm. (b) FFT analysis of the experimental 9-level inverter output voltage based on ECSA.

Even more objectives are achieved by using only two HB with a ratio ternary to obtain an asymmetrical 9-level inverter with a minimum number of electronic power components. Indeed, the obtained inverter guarantees a reduced THD output voltage with a minimum cost. Furthermore, the comparison between algorithm performances allow us to choose the best one to minimize as much as possible THD output voltage by eliminating completely lower harmonics (5th, 7th and 11th) in higher power applications.

6. Conclusion

This paper mainly focused on a comparative study on performances between N-R, G-A and ECSA in order to choose the most accurate one to obtain the smallest output voltage THD rate, while eliminating completely lower order harmonics. A single-phase 9-level CHB asymmetrical inverter has been chosen to evaluate algorithm performances. A comparative study has led to conclude on the accuracy of switching angles obtained by N-R optimization while allowing to eliminate completely lower order harmonics and to obtain an output voltage THD significantly lower than that obtained by GA and ECSA. FPGA-ALTERA-Cyclone II 100 MHz device is used to generate experimental control signals for the chosen CHB multilevel inverter topology. Experimental and simulation results are nearly equal, and both confirm the effectiveness of N-R algorithm.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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