Performance Improvement of SIMD Processor for High-Speed end Devices in IoT Operation Based on Reversible Logic with Hybrid Adder Configuration

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Abstract: The reversible logic function is gaining significant consideration as a style for the logic design by implementing modern Nano and quantum computing with minimal impact on physical entropy. Recent advances in reversible logic allow for computer design applications using advanced quantum computer algorithms. In the literature, significant contributions have been made towards reversible logic gate structures and arithmetic units. However, there are many attempts to dictate the design of Single Instruction-Multiple Data (SIMD) processors. In this research work, a novel programmable reversible logic gate design is verified and a reversible processor design suggests its implementation of SIMD processor. Then, implementing the ripple-carry, carry-select and Kogge-Stone carry look-ahead adders using reversible logic and the performance is compared. The proposed reversible logic-based architecture has a minimum fan out with binary tree structure and minimum logic depth. The simulation result of the proposed design is obtained from Xilinx 14.5 software. From the simulated result, the computational path net delay for 16×16 reversible logic with Kogge Stone Adder is 17.247 ns. Compared with 16-bit Kogge Stone Adder, the reversible logic-based 16-bit Kogge Stone Adder gives low power and low time delay. By looking at the speed, energy and area parameters, including fast applications in which two smaller delay and low power adders are required, the effectiveness, including the proper area use of the hybrid adder recommended by it is evaluated.

Keywords: IoT; Kogge-Stone carry look-ahead; quantum; reversible logic; single instruction-multiple data

1 INTRODUCTION

The Internet of Things (IoT) exemplifies a wide range of sensors, computations, and networking that multiply our physical world. As a result, it is shaping up to be one of the most influential technologies in the modern world. IoT is affecting regions spreading over from agriculture [1-3], medical services [4], manufacturing [5] and by empowering unavoidable information assortment to help further investigation. One of IoT's key segments is the sensor hub, normally a little, low-power device with various sensors, remote communication, and an unassuming measure of computation. As these nodes are often set at locations without significant networking or power structures, such as on farms and forests, many sensor nodes are designed to be highly resource-efficient to operate arbitrarily time-efficient automatically. For example, they may work for quite a long time on a little battery [6, 7] and convey through slow and low-power communication networks [8, 9].

While we see development in both data assortment abilities of IoT devices and examination limit on the gathered data, wireless communications' exhibition and power effectiveness have not scaled as much because of actual imperatives. Subsequently, the data assortment limit of low-power IoT gadgets is regularly confined by the upheld data rate and power utilization of its wireless communication module [10-11]. Network advances for IoT devices give a wide spectrum of decisions, traversing from fast and eager for power to moderate and power proficient. One noticeable way to address the communications issue is edge mining, where the IoT nodes themselves play out some calculations to reduce the measure of data to be sent. Some true applications have shown various adders can reduce the data transmission prerequisite by more than 95% [12-15]. In any case, moving calculation to the edge additionally implies the IoT nodes should have critical calculation capacities, which builds the expense and power prerequisites of every node.

In this research work, we present a case reversible logic-based Kogge-Stone carry look-ahead adder for Field-Programmable Gate Arrays (FPGA), improving execution and power effectiveness calculation significantly [16]. Besides, by offloading the calculation initially done at a central server to power-productive FPGAs, this methodology additionally improves the absolute organization's calculation of power proficiency by a significant magnitude [17, 18]. While using redesign hardware such as FPGAs to achieve high performance on the accelerator is not a new idea [19, 20], we provide an instance of a complex adder implementation and in-depth evaluation on performance and power efficiency incorporating wireless communication overhead.

1.1 IoT Applications

The function of IoT devices in different application regions is shown in Fig.1.
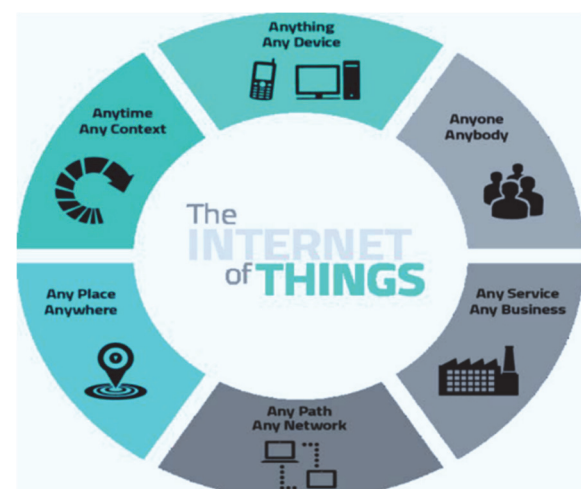

Figure 1 The function of IoT device

The significant destinations for IOT are simply the formation of smart environments/spaces and mindful things (for instance smart vehicle, cities, urban

communities, buildings, energy, health, living, etc.) for the environment, food, energy, portability, advanced society and health applications [22]. The advancements in smart entities will introduce the improvement of the novel advances expected to address the arising difficulties of public health, maturing populace, environment assurance and environmental change, the protection of energy and scant materials, upgrades to safety and security and the continuation and development of economic prosperity.

2 REVERSIBLE LOGIC GATE

Customary logic gates were generally (n : 1) in nature. Where n addresses the number of input signals applied, and 1 shows the single output produced from the gate. Simultaneously, reversible logic gates are (n, n) logic gates. Here both, the number of input signals and the quantity of the output signal are equivalent to n. In ordinary logic gates, output signals are less in number than the number of input signals. In any case, in reversible gates, input and output signals are equivalent in number. The mix of the output signal, in any case, can give the specific status of the input mix. This is the fundamental motivation to name these (n, n) gates reversible logic gates [23-25].
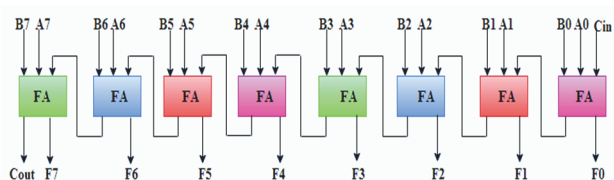

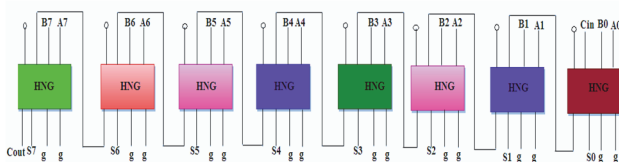**Figure 2** Conventional 8-bit ripple carry adder

Figure 3 Reversible 8-bit ripple carry adder

Fig. 2 shows the conventional 8-bit ripple carry adder, and Fig. 3 shows a reversible logic-based 8-bit ripple carry adder. The quantum cost (48), constant input (8), garbage output (16) and number gate (8) are the most important things for reversible logic-based 8-bit ripple carry adder design.

2.1 Design Constraints of Reversible Logic Gates

Delay and TRLIC are the two constraints in constructing reversible logic circuits that ought to be carefully kept up. The logical mix of reversible logic circuits with a redesigned structure will be finished by having the following attributes.
i.   The least number of logic gates should be used in the design.
ii. Constant input should be negligible.
iii. The proportion of garbage outputs should be kept negligible.
iv. Quantum costs should be kept as low as could be expected.

3 PROPOSED METHOLOGY

Reversible Logic-Based Adder Design
This section presents the design of the adder topology using the reversible logic gate. In this work, the following adder structures are used
i.   Ripple Carry Added.
ii. Carry Select Added.
iii. Kogge-Stone carry look-ahead adder.

3.1 Reversible Logic-Based Ripple-Carry Adder Design

The ripple carry adder is built by falling full adders (FA) blocks in a series arrangement. A single full adder is answerable for adding two binary digits at any phase of the ripple carry adder. The carryout of one phase is taken care of straightforwardly to the carry-in of the procedure stage. Even though this is a straightforward adder and can add unlimited bit length numbers, it is wasteful when enormous bit numbers are utilized. Quite possibly, the most extreme downside of this adder is that the delay increments straightly with the bit length.

3.2 Reversible Logic-Based Carry-Select Adder

Carry Select Adders are among the quickest adders in numerous information preparing processors to perform quick arithmetic functions. The carry-select adder segments the adder into a few gatherings, every one of which performs two increments in parallel. Two four-bit ripple-carry adders are utilized to produce carry per select stage. One ripple-carry adder assesses the carry chain expecting the carry-in is zero; the subsequent ripple-carry adder accepts carry-in to be one. When the carry signals are figured, the right entirety and carryout signs will be chosen by a bunch of multiplexers. Reversible carry select added is carried out straightforwardly from the customary technique. For executing a 1-bit adder, this plan requires four PERES gates and two FREDKIN gates. 4-bit carry select adder constructed utilizing reversible logic can be found in Fig. 4. RFA is a Reversible full adder which can be found in Fig. 5. At each stage, two RFA's are utilized.
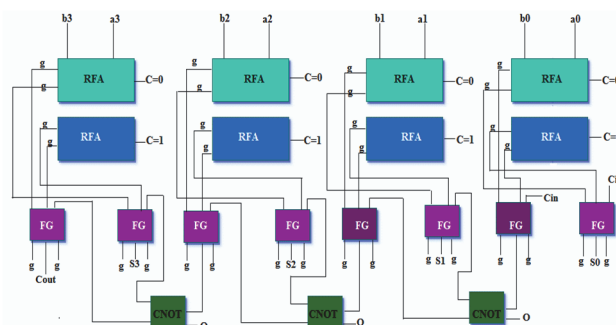

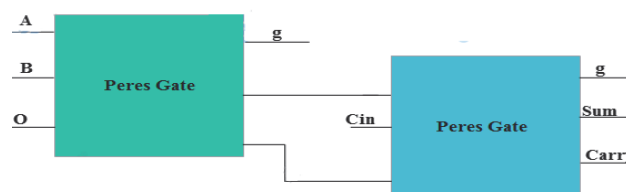**Figure 4** 4-bit reversible carry select adder

Figure 5 Reversible full adder

At whatever point, carry-in is "0", and another for carry-in is "1". FG (FREDKIN) gates in the circuits are utilized as multiplexers, CNOT gates at the base, and buffers. The quantity of garbage yields for each stage is eight. This plan has a Quantum cost of 26 for each stage, as it requires four Peres gates which costs four for each and two Fredkin gates which costs five for each.

3.3 Reversible Logic-Based Carry Look-Ahead Adder

Furthermore, it is quite possibly the essential activities for advanced digital frameworks, and Ripple Carry Adder (RCA) is the establishment of computerized adders, although it has certain conspicuous defects. Then again, carry Look-ahead Adder (CLA) is a sort of enhancement to traditional RCA, which beats RCA imperfections, for example, low computing effectiveness and long delay. Subsequently, CLA becomes one kind of wide-utilized adder. This paper presents another plan of 16-bit CLA that can upgrade computing productivity and diminish energy dissipation dependent on reversible logic theory. Fig. 6 outlines the total construction of the proposed reversible CLA.
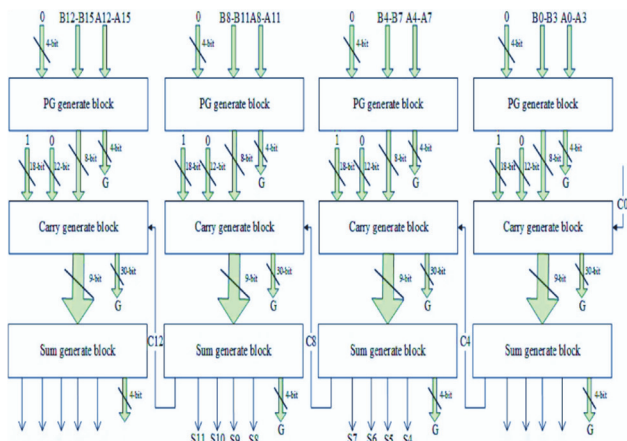
Figure 6 16-bit reversible carry look-ahead adder

The design of the proposed reversible CLA is indistinguishable from the classic electrical circuit. Notwithstanding, we needed to remake every one of the parts with quantum gates, so the circuit has the quality of reversible logic. As referenced previously, the proposed 16-bit CLA is built by four digits gatherings, which implies the four 4-bit CLA are indistinguishable, and we need to course each stage's carry-out to the carry-in of the following stage. Hence, we chiefly worry about rebuilding all aspects of 4-bit CLA, which is PG produces a block, Carry creates a block, and Sum creates block by quantum gates.

The internal quantum circuit is shown in Fig. 7, which PG generates. Quantum circuits have 4 CNOT gates and 4 TOFFOLI gates. The function f this block is $P! = A! \$. B!$ and $G! = A! \, ' \, B!$. The quanta cost of this block is 24.

The Quantum circuit of Carry that generates the block is shown in Fig. 8, which is designed using 10 CNOT gates and 20 TOFFOLI gates. The quantum cost of this block is $10 \cdot 1 + 20 \cdot 5 = 110$. The function of this block is to generate the carry out $C! - \text{CH4}$ of the current stage by $P! - P + z$ and $G - Gf. + Z$.

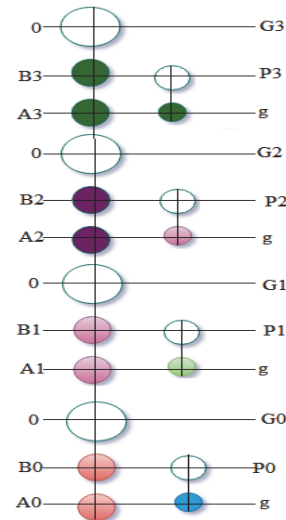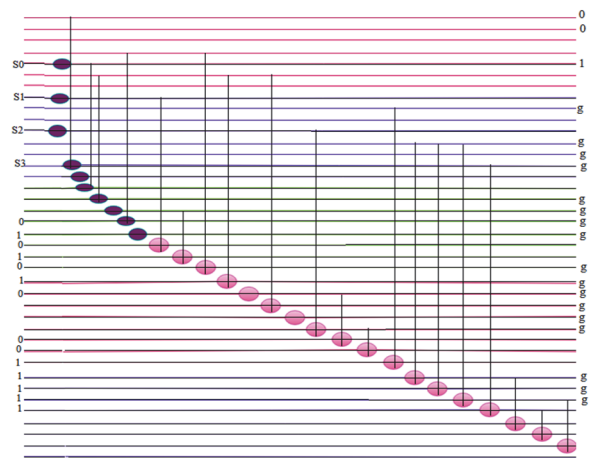**Figure 7** The quantum circuit of PG generates a block

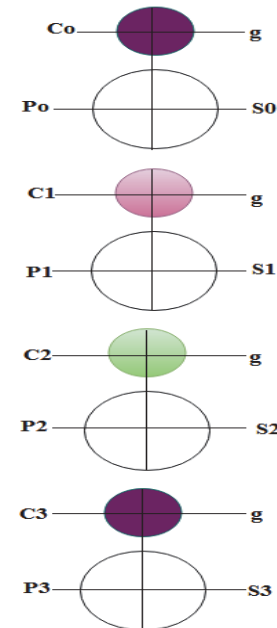**Figure 8** Quantum circuit of carry generates the block

Figure 9 Quantum circuit of the sum generates a block

The Quantum circuit of the Sum generates a block shown in Fig. 9, designed using 4 CNOT gates. The quantum cost is $4 \cdot 1 = 4$ and $S! = C! \$. P!$ is the function of this block. In all figures, "g" is referred to as a garbage line.

3.4 Reversible Logic-Based Kogge-Stone Carry Look-Ahead Adder

Reversible Kogge-Stone adder (RKSA) is a parallel prefix structure that carries a look-ahead adder. In RKSA, all ordinary full adders are supplanted with a reversible HNG gate. Reversible Kogge-Stone prefix adder is a quick adder configuration known as a parallel prefix adder that performs quick logical expansion. Reversible Kogge Stone adder is utilized for wide adders since it shows less delay among different designs. In every upward stage, it produces Propagate and Generate bits. Create bits are delivered in the last stage, and these bits are XOR-ed with the underlying propagate after the contribution to create the sum bits. The proposed rapid 16-bit KSA utilizing prefix adder RLG is displayed in Fig. 10. The fundamental reason for the plan is to abolish tremendous delays, generally speaking to carry calculations. So the profundity logic advanced to the configuration is ideal. Planning a 16-bit prefix reversible adder utilizing logic gates has been acknowledged through CMOS logic's assistance in FPGAS and DSP.
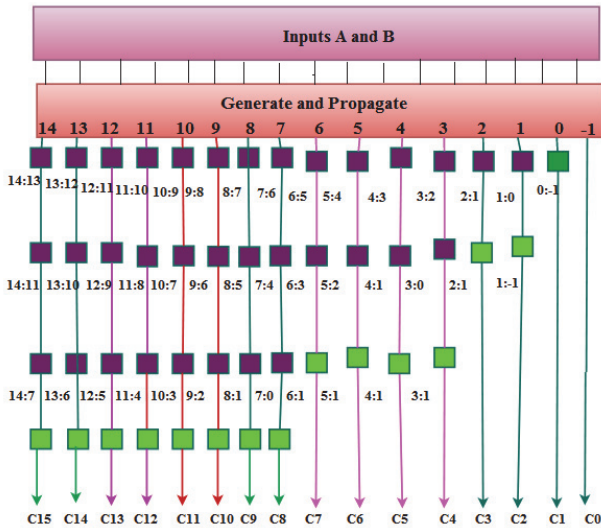

Figure 10 16-bit reversible Kogge-Stone adder

Basic logic develops are just inverter works, so that odd falling cells and even cells give the consequences of annulling alters between those two cells. Two contributions of each stage will be given to the XOR gate and AND gate to such an extent that it is anything but a half adder circuit. Be that as it may, by utilizing the XOR and AND gate, the time delay and power consumption increase. For this, by eliminating both the gates (XOR and AND) are Kogge Stone Adder. Supplanting with reversible logic gates like PERES GATE, applying this gate decreases time delay and force consumption. The geography of the plan is simple to diminish impedance coordinating.

3.5 Reconfigurable IoT Processor

The importance of SIMD stems from being a source of many applications, whether in opening new horizons in the use of technology or in re-evaluating the traditional use of the processors. In this section, we will highlight the number

of applications that have been used as properties of SIMD in their implementation. The Advantages of SIMD for these applications stem from the need for the scientific effort to obtain a speed of implementation, less energy consumption, and cheaper price to shed light on three SIMD uses. Then we will see how these uses have facilitated processors and make them work efficiently.

Conventional SIMD processors are very effective for early visual processing because of their parallelism. However, in performing more advanced processing, they exhibit some problems, such as poor performance in global operations and a tradeoff between processing flexibility and the number of pixels. This work shows a new architecture and sample algorithms of a vision chip that can reconfigure its hardware dynamically by chaining processing elements.

A new architecture has been designed to solve the problems described above and make a more flexible vision chip that can perform more advanced processing. It contains more different features than conventional vision chips and SIMD processors. In particular: 1) it can calculate scalar feature values such as summations at high speed; 2) it can perform fast communication between distant PEs, and 3) the grain size of the PE and network structure is dynamically reconfigurable. These features are achieved by only a small change to a regular SIMD image processor, but the total performance is highly improved.
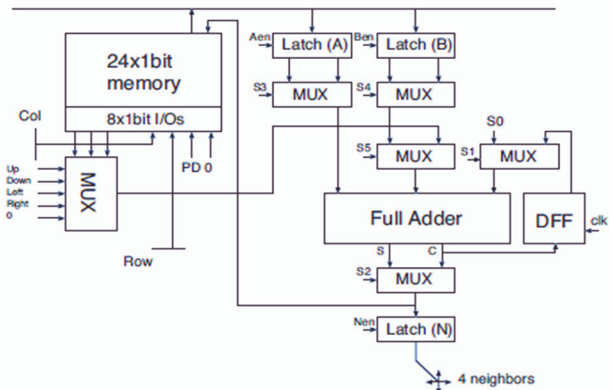
Figure 11 Structure of SIMD-PE

The structure of the PE is shown in Fig. 11. It is similar to that of a regular SIMD image processor with a 1-bit ALU and local memory, which performs a single-bit operation at a time. Still, it differs in that the neighbor output port for inter-PE communication consists of a latch, not a flip-flop. PEs are arranged in a two-dimensional array, and a photo detector (PD) is attached to each PE. Each PE is connected to the neighboring up, down, left, and right PEs and performs inter-PE communication. The grid is open-ended, and the data from outside the array is always 0. A common global bus is provided for every row and column, and data is supplied to the buses from outside via shift registers. Scalar values are output as the processing result via column adders connected to the right-end PEs in an LSB-first bit-serial manner.

The SIMD reversible Hybrid Adder, the multiplier and the shifter are three basic processing units in the ALU. These three segments can be replicated in various widths (4, 8, and 16-bits) for computing data and can answer all the design instructions.

4 RESULT AND DISCUSSION

This section discusses the simulation results and performance analysis of the proposed reconfigurable IoT system using a reversible logic function with some other existing methods. The simulation of the proposed system is designed using Xilinx 14.7 software using Spartan 6 xc6slx-3csg32. Tab. 1 discusses the device utilization of existing adders.

Table 1 Device utilization of different existing adders (16 and 32-bit inputs)

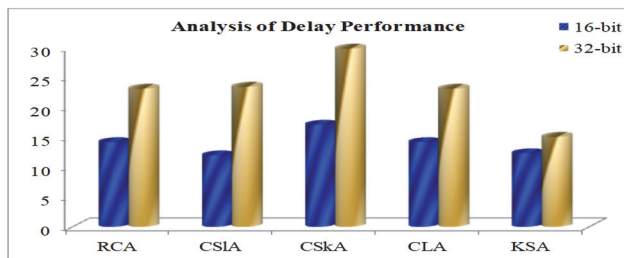| Devices	16-bit inputs					32-bit inputs				
	RCA	CSlA	CSkA	CLA	KSA	RCA	CSlA	CSkA	CLA	KSA
No. of LUTs	24	28	30	24	55	48	48	61	48	144
No. of FFs	24	28	30	24	55	48	48	61	48	144
No. of Ios	49	49	49	49	49	97	97	97	97	97
Delay / ns	14.184	11.968	17.108	14.184	12.309	23.176	23.502	29.904	23.176	15.089

Figure 12 Delay analysis of different existing adders (16 and 32-bit inputs)

Fig. 12 discusses the performance analysis of delay using different adders with 16 and 32 bits. This comparison clearly shows Kogge-Stone adder obtains the minimum delay when compared with other adders. So by using a hybrid combination of an adder with Kogge-Stone one gets a better response. The following Tab. 2 discusses the Device Utilization of different hybrid based on kogge stone adder.

Table 2 Device utilization of different existing hybrid (16 and 32-bit inputs)

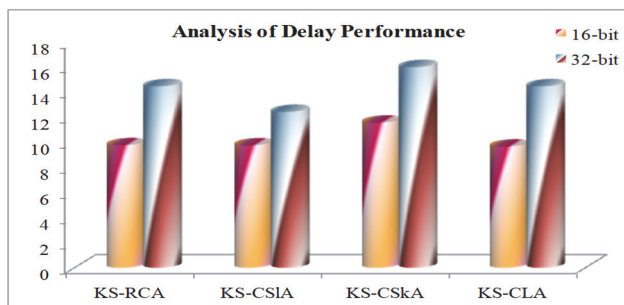| Devices	16-bit inputs				32-bit inputs			
	KS-RCA	KS-CSlA	KS-CSkA	KS-CLA	KS-RCA	KS-CSlA	KS-CSkA	KS-CLA
No. of LUTs	29	31	32	29	78	89	81	78
No. of FFs	29	31	32	29	78	89	81	78
No. of Ios	49	49	49	49	97	97	97	97
Delay / ns	9.793	9.784	11.6	9.688	14.51	12.464	16.046	14.51

Figure 13 Delay analysis of different hybrid adders (16 and 32-bit inputs)

Fig. 13 discusses the performance analysis of delay using different hybrid adders with 16 and 32-bits. This comparison clearly shows that the hybrid combination of kogge stone adder carrying look-ahead adder obtains the minimum delay compared with other hybrid adder combinations.

The following Tab. 3 discusses the Device Utilization of different Reversible hybrid Adders. Compared with normal adders, the hybrid adders consume more devices, but the power consumption and delay are low.

Table 3 Device utilization of different reversible hybrid adders (16 and 32-bit inputs)

Devices	16 - bit inputs				32 - bit inputs			
	Rev-KS-RCA	Rev-KS-CSlA	Rev-KS-CSkA	Rev-KS-CLA	Rev-KS-RCA	Rev-KS-CSlA	Rev-KS-CSkA	Rev-KS-CLA
No. of LUTs	32	33	36	33	81	94	87	84
No. of FFs	31	34	35	34	82	94	85	82
No. of Ios	53	32	53	54	102	102	102	103
Delay / ns	6.85	7.12	7.65	6.896	10.63	9.569	9.61	8.67
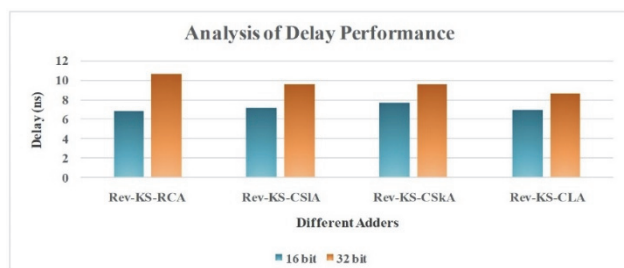
Figure 14 Performance analysis of delay for reversible hybrid adders (16 and 32-bit inputs)

Fig. 14 discusses the performance analysis of delay using different hybrid adders based on reversible logic functions. For example, a Kogge Stone carrying look-ahead adder with reversible logic function obtains the minimum delay in both 16 and 32-bits compared with all adders.

Tab. 4 presents the strong analysis for different adders with proposed reversible logic-based hybrid adders for 16-bit inputs.

This comparison clearly shows the proposed reversible logic-based hybrid adder consumes low power while compared with other adders. For example, the overall power consumption, delay, ADP and PDP of reversible logic based KSA-CLA is 15520.912 nW, 1023 ps, 524.621 and 0.0189 pJ.

Table 4 Performance analysis of different hybrid adders (16-bit inputs)

16-bit inputs	Gates	Area / μm²	Power / nW			Delay / ps	ADP	PDP / pJ
			Static	Dynamic	Total			
Typical Adders								
RCA	16	307	1354	12518.578	13872.683	3996	1226.772	0.0554
CSlA	46	602	3233	24787.813	28020.376	1510	909.02	0.0423
CSkA	28	369	1469	14199.569	15668.505	4417	1629.873	0.0692
CLA	60	389	2238	14688.602	16926.732	3226	1254.914	0.0546
KSA	92	682	4725	24406.227	29130.952	895	610.39	0.0261
Hybrid Adders								
KSA-RCA	45	434	2775	15962.185	18737.54	1774	769.916	0.0332
KSA-CSlA	53	528	3298	19949.696	23247.507	1340	707.52	0.0312
KSA-CSkA	47	457	2707	16381.24	19088.689	2152	983.464	0.0411
KSA-CLA	67	507	3537	17096.911	20633.915	1571	796.497	0.0324
Hybrid Adders with reversible Logic Function								
Rev-KSA-RCA	65	410	2160	13687.162	15847.162	1356	652.362	0.0125
Rev-KSA-CSlA	71	470	2465	15263.786	17728.786	986	436.215	0.0143
Rev- KSA-CSkA	68	395	2045	11463.21	13508.24	1520	761.245	0.0256
Rev-KSA-CLA	88	475	2956	12564.912	15520.912	1023	524.621	0.0189

Table 5 Performance analysis of different hybrid adders (32-bit inputs)

32-bit inputs	Gates	Area / μm²	Power / nW			Delay / ps	ADP	PDP / pJ
			Static	Dynamic	Total			
Typical Adders								
RCA	32	622	2706	26780.396	29486.12	7994	4972.268	0.0725
CSlA	102	1311	7089	55420.45	62509.242	3076	4032.636	0.3929
CSkA	60	765	2974	30834.399	33808.062	9227	7058.655	0.0917
CLA	124	789	4466	30941.361	35406.946	6515	5140.335	0.1382
KSA	238	1674	11380	60069.444	71449.119	1068	1787.832	0.6836
Hybrid Adders								
KSA-RCA	111	1002	6255	39450.761	45705.83	3773	3780.546	0.2468
KSA-CSlA	139	1293	8030	51540.033	59569.863	1510	1952.43	0.4139
KSA-CSkA	121	1059	6266	40773.197	47039.4	4417	4677.603	0.2555
KSA-CLA	157	1118	7455	41589.954	49044.591	3216	3595.488	0.31
Hybrid Adders with reversible Logic Function								
Rev-KSA-RCA	165	1256	5269	34965.897	40234.897	3456	3256.89	0.156
Rev-KSA-CSlA	186	1498	7563	47261.210	54824.12	1325	1742.03	0.263
Rev- KSA-CSkA	172	1369	6879	37692.256	44571.25	4026	4125.36	0.198
Rev-KSA-CLA	196	1496	7012	39456.29	46468.29	2956	3069.31	0.230

Table 6. Performance analysis (16-bit inputs)

Processor	Gates	Area / μm²	Power / nW			Delay / ps
			Static	Dynamic	Total	
Conventional	4918	29258	155799.147	10964626.5	11120425.64	4752
Hybrid adder	4897	29459	152660.644	10885895.8	11038556.49	4562
Reversible Hybrid Adder	4798	30562	149631.632	9765342.36	10215961.40	4163

Tab. 5 presents the strong analysis for different adders with proposed reversible logic-based hybrid adders for 32-bit inputs. This comparison clearly shows the proposed reversible logic-based hybrid adder consumes low power while compared with other adders. For example, the overall power consumption, delay, ADP and PDP of reversible logic based KSA-CLA is 46468.29 nW, 2956 ps, 3069.31 and 0.230 pJ. Finally, the overall performance analysis of different adders with 16-bit adders is shown in Tab. 6.

5 CONCLUSION

This research aimed to define and implement a framework for SIMD architectures that should be reconfigurable using reversible logic-based hybrid adders. Using this framework and the SoC technology, a complete parallel computer has been implemented and to test it in different aspects, an application was also written. This was to reduce the development time and power consumption when implementing a SIMD system and make it easy to evaluate the effectiveness of different applications, intending to construct a reconfigurable framework in VHDL to ease this process. The resulting framework should be implemented on an FPGA and its usability testing. The main parts of a SIMD architecture were identified to be the Control Unit (CU), the Processing Elements (PE) and the Interconnection Network (ICN), and a framework was constructed with these parts as the main building blocks. The proposed SIMD processor design, particularly with the reconfigurable ALU, changed the modifiers for framing adder trees. The possibilities have been demonstrated to decrease delays and power with smart creativity. This demonstrates that reconfigurable processor methods are successful with the capabilities for IoT applications to be enforced. In the future, use a reversible logic-based Vedic multiplier to improve the overall performance of the SIMD processor.

6 REFERENCES

[1] Ayaz, M., Uddin-Ammad, M., Sharif, Z., Mansour, & A El-Hadi. A. (2019). Internet-of-Things (IoT)-Based Smart Agriculture: Toward Making the Fields Talk. *IEEE Access*, 7, 129551- 129583.
https://doi.org/10.1109/ACCESS.2019.2932609

[2] Xianhai, G. (2021). Application of agricultural IoT technology based on 5G network and FPGA. *Microprocessors and Microsystems*, *80*, 103597. https://doi.org/10.1016/j.micpro.2020.103597

[3] Navarro, E., Costa, N., & Pereira, A. (2020).A Systematic Review of IoT Solutions for Smart Farming. *Sensors (Basel), 20*(15), 4231. https://doi.org/10.3390/s20154231

[4] Satpathy, S., Mohan, P., & Das, S. (2020). A new healthcare diagnosis system using an IoT-based fuzzy classifier with FPGA. *Journal of Supercomputing*, *76*, 5849-5861. https://doi.org/10.1007/s11227-019-03013-2

[5] Yang, F. (2020). Passive ultra-low energy building design based on FPGA and Internet of Things. *Microprocessors and Microsystems*, 103412. https://doi.org/10.1016/j.micpro.2020.103412

[6] Alexander, A. & Alexey, M. (2016). Next generation FPGA-based platform for network security. *Proceedings of the XXth Conference of Open Innovations Association FRUCT*, 664, 9-14. https://doi.org/10.1109/FRUCT-ISPIT.2016.7561501

[7] Gomes, T., Pinto, S., Tavares, A., & Cabral, J. (2015). Towards an FPGA-based edge device for the Internet of Things. *IEEE 20th Conference on Emerging Technologies & Factory Automation (ETFA)*. https://doi.org/10.1109/ETFA.2015.7301601

[8] Miguel, M., Luis, A., Rene, C., Jose, J., Claudia, F., & Ignacio, A. (2021). A Compact FPGA-Based Accelerator for Curve-Based Cryptography in Wireless Sensor Networks. *Sensors*. https://doi.org/10.1155/2021/8860413

[9] Ordaz, G., Oscar, O., Manuel, L., Francisco, A., Jose, A., & Solis, R. (2020). DALI Bridge FPGA-Based Implementation in a Wireless Sensor Node for IoT Street Lighting Applications. *Electronics*, *9*, 1803. https://doi.org/10.1155/2021/8860413

[10] Lorandel, J., Jean, P. H., & Herald, M. (2016). Fast Power and Performance Evaluation of FPGA-Based Wireless Communication Systems. *IEEE Access*, *4*. 1-1. https://doi.org/10.1109/ACCESS.2016.2559781

[11] Balan, A., Balan, T., & Cirstea, M. (2020). A PUF-based cryptographic security solution for IoT systems on chip. *Journal of Wireless communication Network*, *231*. https://doi.org/10.1186/s13638-020-01839-6

[12] Chowdhry, B., Poncela, J., & Aamir, M. (2019). Technological Advancements in Wireless and Optical Communication Systems. *Wireless Personal Communication*, 106, 1669-1676. https://doi.org/10.1007/s11277-019-06541-5

[13] Jean-François, P., Jean-Jules, B., & Yvon, S. (2013). Modeling, design and implementation of a low-power FPGA based asynchronous wake-up receiver for wireless applications. *Analog Integrated Circuits and Signal Processing*, *77*, 169-182. https://doi.org/10.1007/s10470-013-0139-2

[14] Ding M., Xu, X., Yan, Y., & Xiong, Z. (2012). An FPGA-Based Real-Time Solution for Networked Motion Control Systems. *Lecture Notes in Computer Science*, 7507. https://doi.org/10.1007/978-3-642-33515-0_57

[15] Velásquez-Aguilar, J., Oubram, O., & Cisneros-Villalobos, L. (2019). Real-Time FPGA-Based Systems to Remote Monitoring. https://doi.org/10.5772/intechopen.89629

[16] Ravi, P., Mahima, G., & Prachi, M. (2015). Design and Implementation of Parallel Prefix Adder for Improving the Performance of Carry Lookahead Adder. *International Journal of Engineering Research & Technology*, *4*(12). https://doi.org/10.17577/IJERTV4IS120608

[17] Indhu, S. (2018).Design and Performance Analysis of Inexact Speculative Han Carlson Adder. *International Journal of Trendy Research in Engineering and Technology*, *2*(4).

[18] Mahesha, Y. & Priya Seema, M. (2020). A Comparative Study on Low Power Adders for Wearable Devices. *International Journal of Scientific & Technology Research*, *9*(10).

[19] Kumari, K., Sri Chakrapani, T., & Kamaraju, M. (2013). Design and Characterization of Koggestone, Sparse Koggestone, Spanning tree and Brentkung Adders. *International Journal of Scientific & Engineering Research*, *4*(10).

[20] Naga Babu, C. & Naga P. (2018). Comparative Analysis of High Speed Carry Skip Adders. *International Journal of Engineering & Technology*, 7, 121-125. https://doi.org/10.14419/ijet.v7i2.24.12015

[21] Satpathy, S., Mohan, P., & Sanchali, S. (2020). A new healthcare diagnosis system using an IoT-based fuzzy classifier with FPGA. *The Journal of Supercomputing*, *76*. https://doi.org/10.1007/s11227-019-03013-2

[22] Thabah, S. & Saha, P. (2019). New design approaches of reversible BCD encoder using Peres and Feynman gates. *ICT Express*, *6*. https://doi.org/10.1016/j.icte.2019.07.001

[23] Mohamed, R., Anshul, G., & Gagan, G. (2014). VHDL Implementation of Reversible Full Adder using PERES Gate. *International Journal of Engineering Research & Technology*, *3*(2).

[24] Gaur, H. & Ashutosh, G. (2018). In-depth Comparative Analysis of Reversible Gates for Designing Logic Circuits. *Procedia Computer Science*, *125*, 810-817. https://doi.org/10.1016/j.procs.2017.12.103

[25] Thakral, S. & Bansal, D. (2016). Implementation and Analysis of Reversible logic Based Arithmetic Logic Unit. *Telkomnika*, *14*. https://doi.org/10.12928/telkomnika.v14i4.323

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