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Optimization of distributed generation units in reactive power compensated reconfigured distribution network

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ABSTRACT

Capacitor Allocation (CA) and Network Reconfiguration (NR) are the traditional methods extensively applied by the researchers for power loss reduction and node voltage improvement in radial Distribution Network (DN) for the past four decades. In recent years, simultaneous optimization of CA and NR is considered to maximize the power loss reduction in a proficient manner in comparison to individual optimization of CA and NR. To solve the objective functions, this work proposes an application of Autonomous Group Particle Swarm Optimization (AGPSO) by optimal allocation and sizing of capacitors with and without NR, under four different cases, subject to satisfying operating constraints. In addition, to ascertain the impact of real power injection on further power loss reduction, this work considers placement and sizing of Distributed Generation (DG) units from single to three optimal nodes in capacitive compensated optimal DN. This proposed methodology is demonstrated using standard IEEE 33 and 69 bus test system and the results obtained by each test case have been compared with other optimization techniques. A significant amount of power loss gets minimized after optimal DG allocation in reactive power compensated optimal DN.

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AGPSO; Capacitor allocation (CA); Network Reconfiguration (NR); Distributed Generation (DG); Distribution Network (DN); Additional Power Loss Reduction

1. Introduction

Most of the DNs are constructed as radial circuits which have only one main source of power supply and the power supply will reach the consumers through feeders (laterals and sub-laterals). As a result, the power losses of the DN get increased with reduction in bus voltage [1]. In India, the average power loss is approximately 30% of the total power generated including power theft [2] considering both transmission and distribution (T&D). Nevertheless, in some states it is still more. Consequently, in order to be more competitive, utilities in the distribution sectors are presently given more attention in minimizing the power losses as it reflects the cost of electricity.

A proficient operation of DN can be done by using NR. NR has been recognized with great importance from 1988 onwards. Hence, many researchers are focussing their researches on optimal NR-based optimization problems [3–6]. By using NR, the advantages, such as reduction in power loss, improvement in bus voltage, load congestion management and reliability of the DN, get improved and this is reflected in the performance improvement of the DN. Although the DN is set as a weak mesh network, its operation is radial only for effective coordination with protection schemes and to reduce the fault level.

Since the 1960s, the application of shunt capacitors has been one of the imperative research studies in radial DN. A part of reduction in power loss could, however, be done by optimal allocation of capacitors which feed a part of reactive power demand. It is well known that by the addition of capacitors in radial DN the benefits, such as reduction in power loss, increase in feeder capacity release as well as power quality improvement, bus voltage enhancement, reduction in kVA demand, improvement in power factor at the sub-station bus etc., can be obtained. Since capacitors lower the reactive requirement from the main source, more real-power output is available. In recent times, many researchers have focused their research on capacitor placement problems [7–17] in DN.

The previous research studies, dealt with either NR or CArelated problems, resulted in unnecessary losses and could not yield minimum loss configuration [18]. Optimal capacitor allocation (CA) along the DN with NR is a non-linear, complex, combinatorial and mixed integer optimization problem which includes integer and binary variables that correspond to the optimal locations at which capacitors are required to be placed and the number of capacitor banks installed at each bus. It is also a computationally in-depth problem whose dimension increases extremely with network size. Only a few research papers are available in the

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literature for optimization of CA and sizing together with NR [19–30].

Minimization of power loss and node voltage deviation as objective, optimal CA with NR under different cases, considering HSA as an optimization method has been proposed in [19]. Combined optimization of CA and NR under five different cases to reduce power loss has been investigated in [20,21]. IBPSO has been utilized to solve the simultaneous NR and optimal CA problem. This method employs a different logically operated structure such as AND, OR, and XOR for the optimization algorithm. NR and CA problem under three different cases using OBDE as an optimization tool has been suggested in [22]. In this work, the cost of the capacitor and energy loss has been taken as an objective. LSF is used to identify the potential location for capacitor installation and the reactive power injection value is fine-tuned by OBDE. NR and CA problem, using a Hybrid Shuffled Frog Leaping Algorithm (HSFLA) associated with fuzzy objective function, has been suggested in [23]. Separate optimization of total real power loss, node voltage deviation and feeder balancing are the goals of this work. Similar to [23], another work, considering HBB-BC as an optimizing method, has been presented in [24]. Ordinal optimization (OO)-based optimal location and sizing of capacitors with NR under three different cases considering power loss reduction as the objective has been reported in [25]. Cost of total energy loss, capacitor purchase cost and voltage constraint penalty as the objective, optimal allocation and sizing of capacitors with and without NR under three cases considering three different load levels (75%, 100% and 125%) were dealt in [26]. Modified Flower Pollination Algorithm (MPFA) has been used in this paper to solve the objective function. NR and CA problem, based on a combination of salp swarm algorithm and real-coded genetic algorithm (SSA-GA) under three scenarios, to reduce power loss has been discussed in [27]. Real power loss reduction, Voltage profile improvement and annual cost saving increase as the objective, optimal allocation and sizing considering two techniques of operations, such as individual OCP and dual OCP-DSR, have been proposed in [28]. In this paper four different optimization algorithms are engaged (MBBO/CS/MIC/MBFBO) to solve multi-objective functions. Self-Adaptive Harmony Search Algorithm (SAHSA) as an optimization method feeder reconfiguration simultaneously with capacitor placement under five different scenarios, considering 100% and 120% loading conditions, to minimize the active power loss and to minimize the bus voltage deviation, has been reported in [29]. DSR (NR)/dual DSR-OCP (NR-CA)-based optimization for IEEE 33 and 69 bus test system were presented in [30]. To find the optimal solution for significant loss reduction and bus voltage profile enhancement, Modified Biogeography Based Optimization (MBBO), Binary Teaching Learning Based Optimization (BTLBO) and Discrete Dolphin Echolocation (DDE) algorithm have been adopted.

Distributed generation (DG) plays a significant role in the modern DN which is associated directly with the DN or on the end-user location. Due to the terrific growth in power demand, the utility DG power has to satisfy the increased power demand. To improve the network performance, such as reduction in power loss and the bus voltage profile enhancement, DGs must be placed optimally with appropriate size while maintaining the system stability which is a complex combinatorial and non-linear optimization problem. Many researchers have solved the DG allocation and sizing problem using various optimization methods. Recently, to reduce power loss in the radial DN, optimal allocation of all the three techniques, such as NR, DG and CA, has been adopted [31–35].

The main focus of this work is to achieve reduction in I^2R loss by reactive power compensation at three and four optimal locations considering with and without NR (cases A to D). This is the initial step of power loss minimization. Furthermore, this work considers real power injection at single to three optimal locations after optimal allocation and sizing of capacitors in the reconfigured DN (cases E and F). This is to identify the impact of DGs on the reduction of additional power loss after reactive power compensation with NR subject to satisfying all the equality and inequality constraints; it has been projected as the next stage of power loss reduction. The node voltage profile has been enhancing further and considerable reduction in additional power loss is also achieved. The method has been tested and verified using standard IEEE 33 and 69 bus test systems. In the light of the above-discussed features, the contributions of this work includes (i) Study of the impact of power loss using DGs (three optimal nodes) in capacitive compensated reconfigured DN (capacitors at three and four optimal locations) (ii) Capacitor sizing simultaneous with NR at three/four optimal nodes.

The entire work has been set in five sections. Section 2 discusses the objective function with Distribution Network Power Flow (DNPF). Section 3 deals with the introduction of AGPSO and its capability to solve the proposed problem. Discussions on the simulation and the results achieved with the comparison have been done in Section 4 and finally Section 5 concludes the work carried out in this work followed by the references.

2. Objective function and power flow

The objective function is to get maximum reduction in power loss/additional power loss by optimal placement and capacity determination of capacitors (at three and four nodes) with NR. Allocation of DG units at

three optimal locations in the reactive power compensated optimal DN while satisfying system equality and inequality constraints.

2.1. Distribution system power flow (DNPF)

Power flow (PF) study plays a very important task for appropriate planning of power transfer to meet the load demands in the modern power system network which is a major task too. From the previous literature, it has been understood that the traditional PF methods, such as Gauss–Seidal, Newton–Raphson and Fast Decoupled PF, used for the Transmission network cannot be used for radial DN because of the radial nature of the DN with high R/X ratio and difficulty in handling power balance equations. In this paper, a robust, fast, flexible and efficient method of PF suitable for radial DN is used which is based on recursive function and a linked-list data structure designed PF study [36]. It has an advantage of the radial nature of DN and also the ability to update easily and to accommodate the reconfiguration of DN and embedded generation. The author exploits a tree-like structure of RDN with efficient use of dynamic data structure.

Let us take a two-bus system $(m, m+1)$, the branch (p) connecting the two buses has an impedance value $(z = r + jx)$. The real and reactive power demand at bus "m" is $P_m + jQ_m$ and the real and reactive PF beyond "$m+1$" is $P_{\text{eff}(m+1)} + j\,Q_{\text{eff}(m+1)}$. Let the load at the receiving end be $(P_{(m+1)} + j\ Q_{(m+1)})$ and P_{LOSS} is the active power loss at branch "p". The bus voltage and phase angle will be obtained by using the DNPF method by applying the above parameters at the load bus according to Equations (1) and (2) [36]. Using the known parameters, such as receiving end real and reactive power, sending end bus voltage with angle (δ) and the line impedance, the receiving end bus voltage with angle for the above-said network can be calculated.

$$V^2_{(m+1)} = -\left[r\,P_{(m+1)} + x\,Q_{(m+1)} - \frac{V^2_m}{2}\right] + \sqrt{\left(r\,P_{(m+1)} + x\,Q_{(m+1)} - \frac{V^2_m}{2}\right)^2 - (r^2 + x^2) \times [(P^2_{(m+1)} + Q^2_{(m+1)})]} \tag{1}$$

$$\delta_{(m+1)} = \delta_{(m)} - \sin^{-1}\left[\frac{x\,P_{(m+1)}r - Q_{(m+1)}}{V_{(m)} \times V_{(m+1)}}\right] \tag{2}$$

At the end of each iteration, DNPF will check the difference between the sum of powers flowing out of the line connected to each bus and the net power injected into each bus. Equations (3) and (4) show the convergence criteria

$$P_{DG}(m) - P_D(m) - \left\{\sum_{m+1}[V_{(m)}\ V_{(m+1)}\ Y_{(m)(m+1)}\ \text{Cos}(\delta_{(m)} - \delta_{(m+1)} - \theta_{(m)(m+1)})]\right\} < \varepsilon \tag{3}$$

$$Q_{DG(m)} - Q_{D(m)} - \left\{\sum_{m+1}[V_{(m)}\ V_{(m+1)}\ Y_{(m)(m+1)}\ \text{Sin}(\delta_{(m)} - \delta_{(m+1)} - \theta_{(m)(m+1)}]\right\} \leq \varepsilon \tag{4}$$

The real and reactive power loss in a distribution feeder section "p" is given by

$$P_{\text{LOSS}(m,\,m+1)} = R_{(m,\,m+1)} \times \frac{[P^2_{(m+1)} + Q^2_{(m+1)}]}{|\,V^2_{(m)}|} \tag{5}$$

$$Q_{\text{LOSS}(m,\,m+1)} = X_{(m,\,m+1)} \times \frac{[P^2_{(m+1)} + Q^2_{(m+1)}]}{|\,V^2_{(m)}\,|} \tag{6}$$

Total real and reactive power loss power loss, incurred in the whole network including all feeders, may be calculated by summing up all the branches of the RDN as given below:

$$TP_{\text{LOSS}} = \sum_{p=1}^{\text{TNB}} P_{\text{LOSS}(p)} \tag{7}$$

$$TQ_{\text{LOSS}} = \sum_{p=1}^{\text{TNB}} Q_{\text{LOSS}\,(p)} \tag{8}$$

where TNB indicates the total number of branches. $Y_{(m,m+1)}$ is the element $(m, m+1)$ in bus admittance matrix, $\theta_{(m,m+1)}$ is the angle of $Y_{(m,m+1)}$ and $\delta_{(m)}$ and $\delta_{(m+1)}$ are the voltage angles of bus "m" and "$m+1$", respectively.

2.2. Problem formulation

$$\textit{Minimize} \quad \text{Fit} = [TP_{\text{LOSS(net)}}] \tag{9}$$

Subject to Equality Constraints

$$P_{MS} - \sum P_D + \sum_{i}^{N_{DG}} P_{DG(i)} - P_{TL} = 0 \tag{10}$$

$$Q_{MS} - \sum Q_D + \sum_{i}^{NC} Q_{C(i)} - Q_{TL} = 0 \tag{11}$$

Subject to Inequality Constraints

$$\sum_{i}^{N_{DG}} P_{DG(i)} \leq \left(\sum P_D + P_{TL}\right) \tag{12}$$

$$P^{\min}_{DG(i)} \leq P_{DG(i)} \leq P^{\max}_{DG(i)} \tag{13}$$

$$Q^{\min}_{C(i)} \leq Q_{C(i)} \leq Q^{\max}_{C(i)} \tag{14}$$

$$\sum_{i}^{NC} Q_{C(i)} \le \left(\sum Q_D + Q_{TL}\right) \tag{15}$$

$$V_{(i)}^{\min} \le V_i \le V_i^{\max} \tag{16}$$

where $TP_{\text{LOSS(net)}=}(TP_{\text{LOSS }(AC)}/TP_{\text{LOSS }(BC)})$ (for cases A to D); $TP_{\text{LOSS(net)}=}(TP_{\text{LOSS (ADGI)}}/TP_{\text{LOSS (BDGI)}})$ (for cases E and F);

Radial configuration constraint: It is mandatory that the DN should be maintained in radial to avoid excess current flow. Therefore, several constraints must be considered to retain the radiality structure during NR. For the selection of switches, many rules and procedures have to be implemented. Sectionalizing switches that do not belong to any loop and connected to the sources that contributed to a meshed network have to be closed.

Isolation constraints: By doing NR, all the nodes must be energized and also reactivated to ensure that all loads get power supplies, that is, during reconfiguration process, all buses should stay connected and no customer should be left unconnected.

3. Proposed technique (AGPSO) [38]

PSO is an evolutionary computation technique that has been proposed by Kennedy and Eberhart [37]. It is inspired from the social behaviour of bird flocking which uses a number of particles flying around the search space to find the best solution. The particles trace the best location (best solution) in their paths over the course of iterations. These concepts have been mathematically modelled using a position vector (x) and velocity vector (v) of length of problem (number of variables). In the course of iterations, a particle adjusts its position and velocity as follows:

$$v_i^{t+1} = (w \times v_i^t) + (C_1 \times \text{rand} \times (p\text{best}_i - x_i^t)) + (C_2 \times \text{rand} \times (g\text{best}_i - x_i^t)) \tag{17}$$

$$x_i^{t+1} = x_i^t + v_i^{t+1} \tag{18}$$

In this paper, PSO is modified by a mathematical model of different functions with diverse slopes, curvatures, and interception points being employed to tune the socio and cognitive constants of C_1 and C_2 parameters to generate particles of different behaviours to achieve the desired solution. This modification has led the standard PSO into a modified particle swarm optimization algorithm named AGPSO.

AGPSO is mainly applied to alleviate the two major problems of trapping in local minima and slow convergence rate of PSO in finding the optimal position of switches and placement and sizing of Capacitor banks and DGs. Detailed descriptions about AGPSO are available in [38] with the merits of AGPSO compared with variants of PSO. Updating strategies to tune the C_1 and C_2 parameters have been given in [38].

3.1. Arrangement of parameters to solve CA with NR and DGs

The use of AGPSO in allocation and sizing of capacitors with NR and allocation of DGs in the reconfigured capacitor allocated radial DN to achieve additional reduction in real power loss which has been described in this segment. The steps to be followed are given below:

Step 1: Initialize the particles Xi of PSO randomly within the boundary limits according to Table 1. For NR, the total number of Solution Vectors (SV) is 10 (5 tie-switches) (case A). Since this paper considers optimal allocation and sizing of capacitors at three/four nodes, the SVs are equal to six/eight (case C). Optimal nodes for CA and its corresponding sizing are represented as N_{cap} and K_{cap}, respectively. Thus the SVs are sixteen/eighteen for cases D and E. Considering cases F and G, the variables are six (two variables for each DG). The optimal node and optimal sizing are represented as N_{DG} and K_{DG}, respectively.

$$X_{(iT)} = \begin{bmatrix} \text{Tie-switch status} & (1 \text{ to } 5) \\ \text{Status of opening of sectionalizing switches} & (6 \text{ to } 10) \\ \text{Optimal Capacitor node} N_{\text{Cap}} & (11, 13, 15, 17) \\ \text{Optimal Capacitor sizing } K_{\text{Cap}} & (12, 14, 16, 18) \\ N_{DG,1}, K_{DG,1}, N_{DG,2}, K_{DG,2} N_{DG,3}, K_{DG,3} & \end{bmatrix}^{T}_{(24\times 1)} \tag{19}$$

Thus the total SVs are twenty four considering NR, capacitors at four optimal nodes and DG at three nodes, as given in (19). "T" indicates the population size from a set of random distributions. Only the particles that satisfy all the constraints will be considered as the initial population. Table 1 indicates the minimum and maximum values of capacitors (kVAr) for four optimal nodes and DGs for three optimal nodes. Figure 1 shows the flow chart for the proposed method.

Step 2: Particles *Xi* are randomly split into some predefined autonomous groups with beneficiary functions according to Table 1 [38].

Table 1. Typical value of particles (cases B to G).

Variables		Solution vectors (SV)		Variables		Solution vectors range
$X^{(11)}$	$X^{(13)}$	Node no. 2–33	/2–69	$X^{(12)}$	$X^{(14)}$	0.15–2.1 MVAr (in discrete steps of 0.15 MVAr)
$X^{(15)}$	$X^{(17)}$			$X^{(16)}$	$X^{(18)}$	
$X^{(19)}$	$X^{(21)}$	Node no. 2–33	/2–69	$X^{(20)}$	$X^{(22)}$	0.5 –2 MW
$X^{(23)}$				$X^{(24)}$		

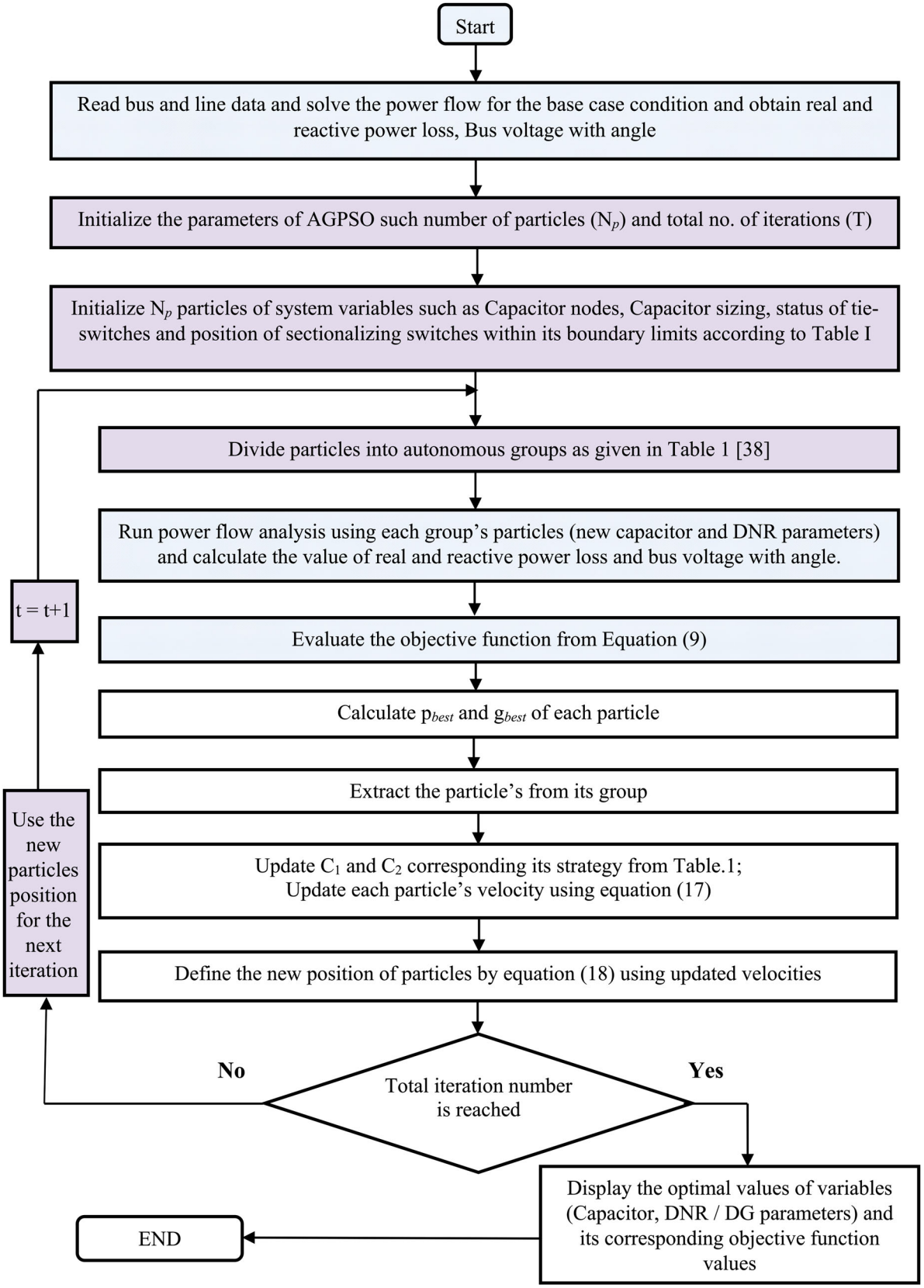

Figure 1. Flow chart of the proposed method (AGPSO).

Step 3: g_{best}, p_{best}, and the fitness given in (1) of each particle (Xi_T) at each iteration have been calculated.

Step 4: For each particle, the coefficients C_1 and C_2 have been updated using its group's strategy.

Step 5: Velocities and positions of particles have been updated using (17) and (18).

Change in variable parameters can be obtained by substituting (19) into (17) and (18) when particles change from existing position to a new position. Recently generated variables were obtained at the end of each iteration, former inferior vectors will get replaced and this process cycle gets completed once

the maximum number of iterations has reached. For both test systems, the parameters, such as agent size and the number of iterations, are selected as 800 and 100, respectively. Out of three objective function values (AGPSO1, AGPSO2 and AGPSO3), only the best one (the least objective value) will be considered.

4. Case study details simulation results

The test system has 33 buses, 32 sectionalizing switches and 5 tie-switches (5 looping branches) as shown in Figure 2. The system voltage is 12.66 KV. The base MVA and base KV for the test case are taken as 100 and 12.66, respectively. The total apparent power demand of this network is $(3715 + j2300)$ kVA. The total apparent power loss under BC is $(211 + j143.135)$ kVA and the minimum voltage recorded is 0.9038 p.u at bus no. 18. Node No.1 (main source node) is considered as a slack node and all the remaining nodes are considered as load nodes. AGPSO coding has been developed in MATLAB software and runs on an Intel i5 third generation processor with 4 GB RAM. The minimum and maximum voltages have been set as 0.95 and 1.05 p.u., respectively. Only the least value that corresponds to each test case is considered as the best value which are tabulated in the corresponding tables.

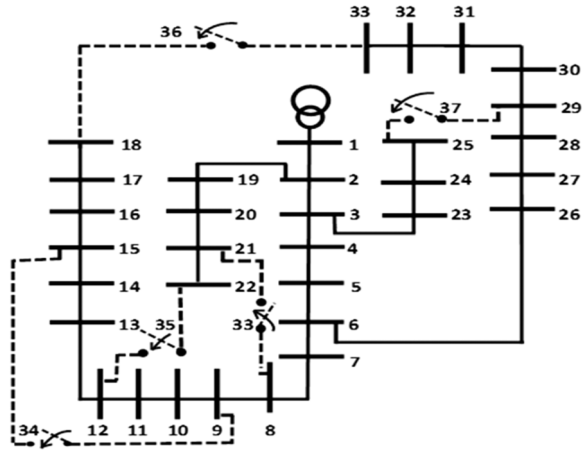

Figure 2. IEEE 33 bus test system – BC.

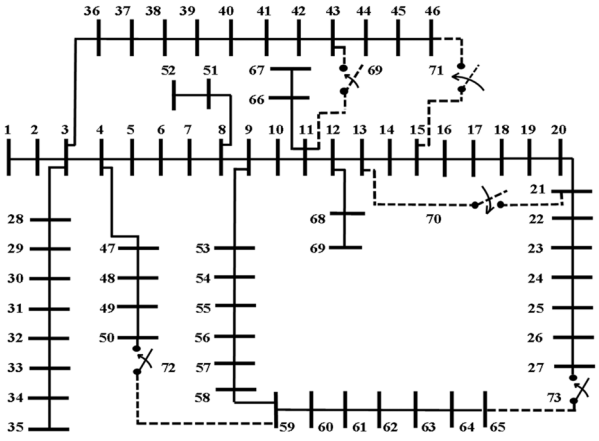

Figure 3. IEEE 69 bus test system – BC.

The next test system is IEEE 69 bus test system which has 69 buses, 68 sectionalizing switches, as shown in Figure 3. Remaining parameter details are similar to those of IEEE 33 bus test system. The total real and reactive power demand of this DN are 3802 kW and 2695 kVAr, respectively. The minimum bus voltage BC is 0.90919 p.u at bus no. 65. The total apparent power loss under BC is $(225 + j102.1155)$ kVA.

Six different cases have been considered for studying the usefulness of the proposed technique in achieving initial power loss reduction (cases A to D) and minimization of additional power losses (cases E and F). The maximum real and the reactive power injection are assumed to be less than or equal to the total real and reactive power demand of the system including BC real and reactive power losses.

Case A: NR is employed in the BC network with the objective to reduce the power loss.

Case B: To evaluate the power loss, capacitors at three and four optimal nodes have been performed in BC DN.

Case C: This condition is similar to the case B, but NR has been carried out to investigate the usefulness of NR in power loss reduction.

Case D: Keeping the optimal location obtained under case B, NR has been performed simultaneously with capacitor sizing to examine the effectiveness of power loss minimization compared to case C.

Case E: To assess the additional power loss minimization, allocation and sizing of DG units from a single optimal node to three optimal nodes have been installed after case C.

Table 2. Results obtained by AGPSO – cases B to D – scenarios 1 and 2 – IEEE 33 bus.

	Scenario 1			Scenario 2		
Parameters	Case B	Case C	Case D	Case B	Case C	Case D
Capacitor details (kVAr)	12 (450), 24 (600), 30 (1050)	12 (450), 24 (600), 30 (1050)	12 (600), 24 (450), 30 (900)	14 (300), 7 (450), 24 (450), 30 (900)	14 (300), 7 (450), 24 (450), 30 (900)	14 (600), 7 (300), 24 (450), 30 (750)
Switch status	33–34–35–36–37	6–14–9–32–37	7–14–9–32–37	33–34–35–36–37	6–13–9–32–37	7–13–9–31–37
P_{Loss} (KW)	**138.44**	**84.1986**	**83.304**	**136.846**	**83.7652**	**83.2835**
Q_{Loss} (KVAr)	94.3894	77.745	78.287	93.4	78.4846	83.242
% P_{Loss} reduction	**34.4**	**60.103**	**60.519**	**35.144**	**60.3**	**60.53663**
$V_{min(p.u)}$/bus no.	0.9309 (18)	0.9607 (33)	0.9626 (33)	0.9342 (18)	0.96412 (32)	0.9672 (32)

Case F: To check the effectiveness of the additional power loss minimization, DGs are placed optimally from a single node to three nodes after case D.

4.1. IEEE 33 bus system results and discussions

After optimal NR (case A), the real and reactive power losses have been reduced by 40.4% and 22%, respectively consequent to the opening of five sectionalizing switches 7, 14, 10, 32 and 28 (maintaining radial arrangement) which is better when compared to [3–6,26]. The bus voltage improvement after case A is around 0.04 p.u compared to BC.

In this work, optimal allocation and sizing of capacitors have been considered to distinguish the effect of power loss reduction and bus voltage enhancement under three and four optimal nodes. From Table 2, it has been seen that a power loss reduction of 34.4% and 35.144% after allocation and sizing of capacitors at three and four optimal nodes. The value of reactive power support is 86.273% of the total reactive power demand plus losses. However, the power loss reduction difference between scenario 1 and 2 under case B is negligible. The bus voltage enhanced after case C is 0.0271 p.u (scenario 1) and 0.0304 p.u (scenario 2) compared to BC. Considering Tables 3 and 4, by comparing the results obtained under scenario 1 and 2, it is obvious that the proposed method yields the power loss reduction in a better way than other existing methods. But still average bus voltage improvement difference after case B with the other methods is around 0.01 p.u.

Keeping the optimal values obtained under case B, the remaining two cases (cases C and D) have been derived considering NR. NR has been performed after case B to know the effect of power loss reduction under case C. Out of the five tie-switches, four switches (33, 34, 35, 36) have been closed against opening of respective sectionalizing switches in that particular loop to maintain the radiality structure. Using NR the reduction of total real power loss achieved is $> 60\%$ and also the additional power loss achieved beyond case B is 25.703% (scenario 1) and the reduction in the power loss difference between scenario 1 and 2 is below 1 kW only.

Yet, the power loss reduction difference between cases B and C under scenario 1 is more than scenario 2. Approximately 0.03 p.u of bus voltage improvement is observed after case C compared to case B. It is to be noted that the values of the bus voltage enhanced from BC to case B and case B to case C are almost the same. The progress in bus voltage comparing BC and D (scenarios 1 and 2) is around 0.0588 and 0.0634 p.u., respectively. The performance of the AGPSO in achieving power loss reduction considering cases C and D is depicted in Table 2 and also the results obtained are compared with the other existing methods which are depicted from Tables 5–8.

Table 3. Comparison of case B – scenario 1 – IEEE 33 bus.

Parameters	Locust search [12]	FPA [10]	MFO/GWO/DFO [13]	GWO [17]	WCA [17]	DVSA [39]	PSOQN [40]	PSOGSA [40]	AGPSO
Capacitor details	450 (12), 350 (25), 900 (30)	450 (13),450 (24), 900 (30)	450 (8), 300(13), 900 (30)	750(5) , 300(13), 750 (29)	750 (5), 300 (12), 750 (29)	450 (12), 450 (24), 1050 (30)	600 (6), 300 (13), 750 (30)	450 (8), 300 (13), 900 (30)	450 (12), 600 (24), 1050 (30)
P_{Loss} (KW)/(P_{Loss} – BC)	139.23/210.97	139.075/210.97	134.0725/202.65	133.94/202.66	134/202.66	138.416/210.987	134.1057/202.6774	134.0725/202.6774	**138.44/211**
Bus voltage (p.u.)	0.9291(18)	–	0.94 (18)	0.9397 (18)	0.9382 (18)	–	0.9369(18)	0.94(18)	0.9309 (18)
% P_{Loss} reduction	34	34.2987	33.84	33.91	33.88	34.39596	33.8239	33.84	**34.4**

Table 4. Comparison of case B – scenario 2 – IEEE 33 bus.

Parameters	IBPSO [20]	HSA [19]	Locust search [12]	FRCGA [7]	wAFSA [14]	AGPSO
Capacitor details	300 kVAr at 3, 14, 22 and 24, 600 kVAr at 30 and 31, 900 kVAr at 1	900 (6), 300 (28), 600 (29), 300 (30)	150 kVAr at 5, 8, 11, 16, 26 and 32, 450 (24), 750 (30)	25 (28), 475 (6), 300 (29), 175 (8), 400 (30), 350 (9)	470 (15), 450 (24), 450 (30), 560 (31)	300 (14), 450 (7), 450 (24), 900 (30)
P_{Loss} (KW)/(P_{Loss} − BC)	134.2/202.68	135.16/202.66	136.1/210.97	141.24/210.98	131.4628/201.8925	**136.846 / 211**
Bus voltage (p.u.)	0.9389	0.9349	0.9325	–	0.9489 (18)	0.9342 (18)
% P_{Loss} reduction	33.787255	33.33	35.488	33.0553	34.88475	**35.144**

Table 5. Comparison of case C – scenario 1 – IEEE 33 bus.

Parameters	MBBO [28]	CS [28]	MIC [28]	MBFBO [28]	AGPSO
Capacitor details	750 (27), 450 (30), 600 (24)	300 (8), 750 (30), 600 (23)	750 (27), 150 (2), 750 (24)	900 (5), 600 (27), 750 (2)	12 (450), 24 (600), 30 (1050)
Switch status	7–11–34–36–28	8–5–37–30–12	9–25–14–33–37	8–37–14–7–36	6–14–9–32–37
P_{Loss} (KW)/(P_{Loss} − BC)	83.469/202.677	95.6628/202.677	97.6377/202.677	97.3076/202.677	**84.1986/211.04**
Node voltage (p.u.)	0.9559	0.9704	0.95	0.95	0.9607 (33)
% P_{Loss} reduction	58.816758	52.8	51.826	51.98885	**60.103**

Table 6. Comparison of case C – scenario 2 – IEEE 33 bus.

Parameters	IBPSO [21]	HBB-BC [24]	Ordinal optimization [25]	SSA-GA [27]	AGPSO
Capacitor details	3 (300), 14 (300), 22 (300), 1 (900), 24 (300), 30 (600), 31 (600)	300 KVAr each at nodes 2, 4, 10, 11, 18, 24,28, 29 & 30	23 (300), 24 (300), 29 (600), 7 (450), 31 (300)	300 kVAr each at Bus No. 6, 9, 12, 23, 25 & 31 and 600(30)	7 (450), 24 (450), 30 (900), 14 (300)
Switch status	7–10–34–36–37	7–11–14–37–32	7–9–14–32–37	7–9–14–32–37	6–13–9–32–37
P_{Loss} (KW)/(P_{Loss} − BC)	95.91/202.68	92.5757/202.677	81.81/204.14	90.05/202.70	**83.7652/211**
Node voltage (p.u.)	0.9658	0.95858745	–	0.961 (33)	0.96412 (32)
% P_{Loss} reduction	52.679	54.32	59.92456	55.35274	**60.3**

Table 7. Comparison of case D – scenario 1 – IEEE 33 bus.

Parameters	OBDEA [22]	HSA [19]	IBPSO [20]	MPFA [26]	AGPSO
Capacitor details	149 (27), 727 (28), 149 (29)	900 (6), 300 (28), 600 (29), 300(30), 300 (9)	600 (7), 300 (12), 300 (25), 600 (30), 300 (33)	200 (28), 200 (29), 550 (30)	12 (600), 24 (450), 30 (900)
Switch status	7–9–14–32–37	33–14–8–32–28	7–9–14–32–37	7–14–9–36–37	7–14–9–32–37
P_{Loss} (KW)/(P_{Loss} − BC)	101.42/202.67	119.72/202.66	93.061/202.66	101.77/212.2	**83.304/211**
Node voltage (p.u.)	0.959	0.9411	0.9585	0.9544	0.9626 (33)
% P_{Loss} reduction	49.958	40.9257	54.08	51.75	**60.519**

Table 8. Comparison of case D – scenario 2 – IEEE 33 bus.

Parameters	HSFLA [23]	IBPSO [23]	IPSO [23]	PSO [23]	AGPSO
Capacitor details	300 KVAr each at nodes 2, 4, 10, 11, 18, 24, 28, 29 and 30	29 (600), 11 (300), 6 (600), 24 (300), 32 (300)	5 (300), 13 (300), 28 (1200), 32 (300)	29 (600), 10 (300), 6 (600), 9 (300), 31 (300)	7 (300), 24 (450), 14 (600), 30 (750)
Switch status	7–11–14–37–32	7–9–14–32–37	11–28–33–34–36	7–10–14–37–36	7–13–9–31–37
P_{Loss} (KW)/(P_{Loss} − BC)	92.5768/202.677	93.061/202.677	98.834/202.677	95.38/202.677	**83.2835/211**
V_{min} (p.u.)	0.95858745 (17)	0.9585 (17)	0.965607 (17)	0.96351 (17)	0.9672 (32)
% P_{Loss} reduction	54.32	54.08	51.23	52.93	**60.53663**

By comparing the results obtained under cases C and D (scenario 1) with Tables 5 and 6, it is clear that the proposed method minimizes the power loss in a better manner than [28,19,20,22,26] and also the minimum and the maximum power loss reduction differences are 1.286242% and 8.277% for case C and for case D, 6.439% and 19.5933%, respectively. Better improvement in bus voltage has been noticed compared to other existing methods. Similarly, by comparing the results obtained under cases C and D (scenario 2) with Tables 7 and 8, it is visible that AGPSO enhances the power loss reduction in a better way than [21,24,25,27,23] and also the minimum and the maximum power loss reduction differences are 6.31663% and 9.40663%, respectively for case C and for case D, a maximum difference of 7.621% has been noticed. However, the minimum power loss difference is negligible. Better improvement in bus voltages is observed compared to other existing methods.

From the above discussion, it is apparent that the performance of AGPSO in power loss minimization is better than other existing methods. Conversely, to

Table 9. Results obtained by AGPSO – cases E and F – scenarios 1 and 2 – IEEE 33 bus.

	Scenario 1		Scenario 2	
Parameters	Case E	Case F	Case E	Case F
	DG at single optimal node			
DG size and (node) (KW)	1517 (8)	1509 (8)	1508 (8)	1488 (21)
P_{Loss} (KW)	**51.505**	**50.887**	**51.79**	**50.899**
Q_{Loss} (KVAr)	46.087	47.077	42.7	48.264
Total P_{Loss} reduction	75.59%	75.883%	75.455%	75.87725%
Additional P_{Loss} reduction	**15.487%**	**15.364%**	**15.155%**	**15.34062%**
V_{min} (p.u.)/bus no.	0.96503 (32)	0.96538 (32)	0.96512 (32)	0.96749 (32)
V_{max} (p.u.)/bus no.	1.0008 (12)	1.0052 (12)	1.0025 (7)	1.001 (7)
	DG at two optimal nodes			
DG size and (node) (KW)	1463 (8)	1414 (8)	1471 (8)	1466 (21)
	965 (30)	991 (30)	996 (30)	965 (30)
P_{Loss} (KW)	**20.949**	**20.512**	**21.429**	**20.814**
Q_{Loss} (KVAr)	26.848	27.171	24.16	29.261
Total P_{Loss} reduction	90.0716%	90.2787%	89.8441%	90.13555%
Additional P_{Loss} reduction	**29.9686%**	**29.7597%**	**29.5441%**	**29.59892%**
V_{min} (p.u.)/bus no.	0.98206 (33)	0.98329 (33)	0.98503 (25)	0.98561 (25)
V_{max} (p.u.)/bus no.	1.0011 (30)	1.0054 (12)	1.0033 (14)	1.0012 (7)
	DG at three optimal nodes			
DG size and (node) (KW)	887 (30)	803 (30)	845 (30)	889 (30)
	785 (25)	832 (24)	1005 (24)	997 (24)
	1457 (8)	1514 (8)	1425 (8)	1367 (8)
P_{Loss} (KW)	**9.7168**	**9.1656**	**9.1485**	**8.5**
Q_{Loss} (KVAr)	19.363	21.161	14.737	13.367
Total P_{Loss} reduction	95.395%	95.656%	95.66422%	95.97156%
Additional P_{Loss} reduction	**35.292%**	**35.137%**	**35.36422%**	**35.43493%**
V_{min} (p.u.)/bus no.	0.98515 (33)	0.98524 (33)	0.99486 (33)	0.99524 (33)
V_{max} (p.u.)/bus no.	1.0039 (30)	1.0054 (12)	1.0034 (7)	1.0013 (30)

prove the performance AGPSO in achieving power loss reduction further, this work considers allocation and sizing of DG units (considering PV renewable power generation) starts from a single to three optimal nodes in capacitive compensated reconfigured DN. Table 9 shows the performance of the real power injection in minimizing the power loss reduction after reactive power injection at three and four optimal nodes (scenarios 1 and 2) in optimal network.

By optimal allocation of DG units at a single to three optimal nodes, the total real power loss reduction achieved by AGPSO is more than 75%, 90% and 95%, respectively and also the reactive power loss reduction achieved is around 64%, 78% and 91%, respectively. A further power loss reduction of around 15%, 30% and 35% beyond cases C and D has been achieved by the real power injection of around 40%, 65% and 88% of the total real power demand of the network. The bus voltage improvement before and after DG incorporation is from 0.035 to 0.04 p.u. (single node) and from 0.018 to 0.02 p.u (two nodes), respectively. On the other hand, the bus voltage improvement after the allocation and sizing of DGs at three locations is 0.02 and 0.0983 p.u, respectively considering scenarios 1 and 2.

By comparing Table 10, it is clear that the minimum and the maximum power loss reduction differences between AGPSO with other methods are . 1.53% to 4%. It is obvious that the proposed method minimizes the power loss in an efficient manner. Figures 4–9 show the bus voltage profile for the cases BC to F considering both scenarios.

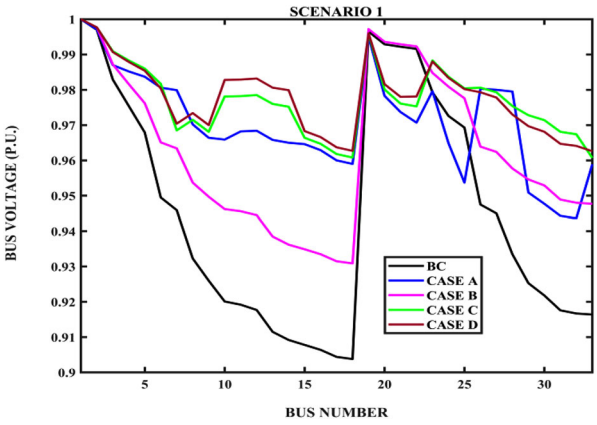

Figure 4. Bus voltage profile – cases BC to D – scenario 1.

Table 10. Comparison of case G – scenario 1 – IEEE 33 bus.

Parameters	IGA [31]	IPSO [31]	ITLBO [31]	LSHADE-EpSin [32]	Analytical [33]	AGPSO
DG nodes and sizes	14 (748)	14 (748)	14 (744)	557 (15),	29 (1300)	803 (30)
	24 (1079)	24 (1003)	24 (1070)	813 (25),	8 (1300)	832 (24)
	30 (1043)	30 (1057)	30 (1048)	630 (32)	32 (325)	1514 (8)
Capacitor nodes and sizes	15 (300)	14 (300)	15 (300)	703 (3),	30 (1000)	12 (600)
	25 (300)	24 (500)	24 (500)	399 (9),	21 (700)	24 (450)
	30 (1100)	30 (1000)	30 (1000)	1198 (30)	6 (300)	30 (900)
Optimal configuration	7–9–17–35–37	7–9–17–25–35	7–9–17–35–37	7–11–12–17–26	7–9–14–28–31	7–14–9–32–37
V_{min} (p.u.)	–	–	–	0.9891 (12)	0.9889 (32)	0.98524 (33)
Power loss (kW)	11.59	11.12	11.21	15.63/210.97	11.71/211.2	**8.5/211**
% Loss reduction	91.91	92.2	92.12	92.5914	**94.46**	**95.97156**

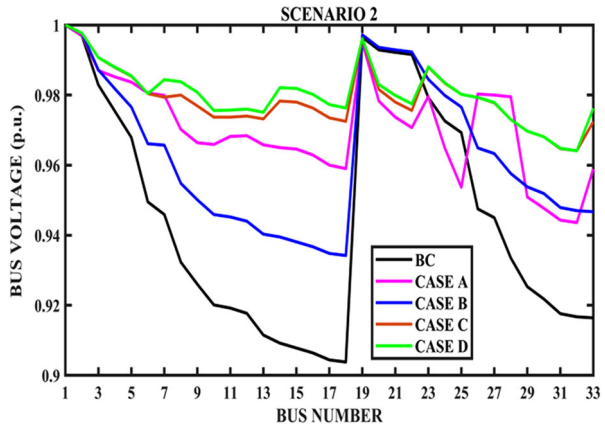

Figure 5. Bus voltage profile – cases BC to D – scenario 2.

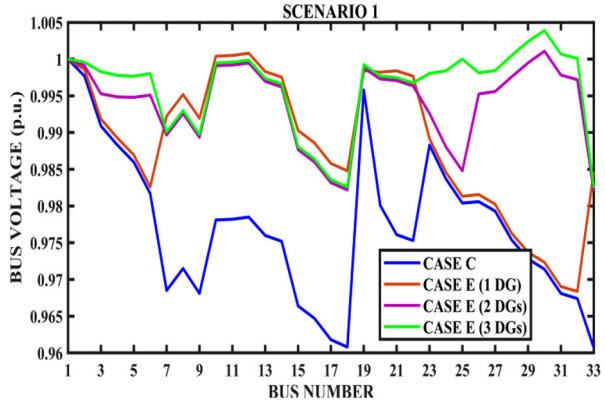

Figure 6. Bus voltage profile – cases C and E – scenario 1.

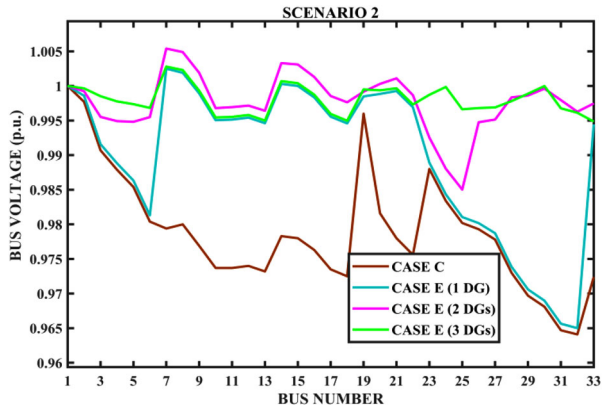

Figure 7. Bus voltage profile – cases C and E – scenario 2.

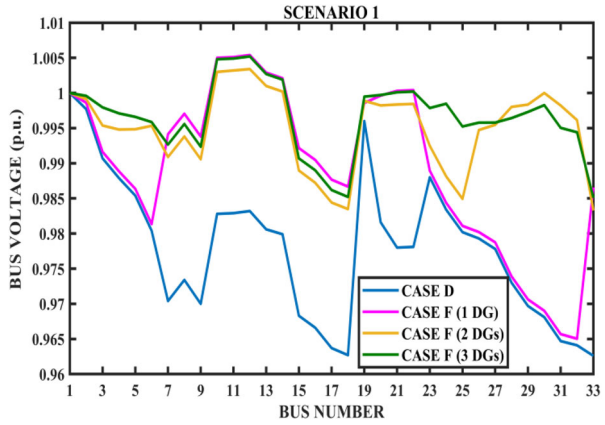

Figure 8. Bus voltage profile – cases D and F – scenario 1.

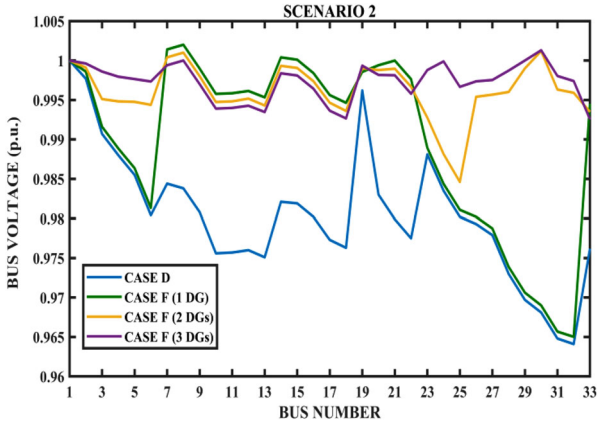

Figure 9. Bus voltage profile – cases D and F – scenario 2.

4.2. IEEE 69 bus system results and discussions

Similar to IEEE 33 bus test system, this test system also underwent six different cases and two scenarios. By successful opening of three sectionalizing switches (71, 72 and 73) against opening three tie switches (14, 58 and 61), a real and reactive power loss reduction of 56.1903% and 9.88%, respectively has been obtained while maintaining radial arrangement. The bus voltage improvement after case A is around 0.04031 p.u compared to BC. It is obvious that the performance of the proposed method is effective in achieving better power loss minimization compared with FPEO [3], BPSO [4], CGA and ICSA [5] and PSO with H-matrix [6].

Table 11 reveals the results obtained using the proposed method. Considering case B, optimal allocation and sizing of capacitors at three/four optimal nodes yields a power loss reduction of 35.5% and 35.83%, respectively by injecting 66.7% and 89.05% of reactive power (scenarios 1 and 2). From case B, it is to be noted that addition of capacitors at fourth node has not yielded the expected effect on power loss reduction, that is, the outcome of scenario 2 on power loss reduction and bus voltage enhancement is very less compared to that of scenario 1. An enhancement in bus voltage after case B is about 0.02161 p.u compared to BC. By comparing the results obtained under scenarios 1 and 2 under case B with the existing methods (Tables 12 and 13), it is obvious that the proposed method yields the power loss reduction in a better manner than [8,9,11,12,15,16,39]. But the average bus voltage improvement difference after case B compared with other methods is almost negligible.

From Table 11, it is visible that a total power loss reduction of around 70% has been achieved under cases C and D (scenarios 1 and 2) which is roughly 35% additional power loss reduction beyond case B and approximately 14% excess power loss reduction compared to case A. Similar to case A, the opening and closing of sectionalizing and tie switches are three only. Bus voltage enhancement after cases C and D is approximately

Table 11. Results obtained by AGPSO – cases B to D – scenarios 1 and 2 – IEEE 69 bus.

		Scenario 1			Scenario 2		
Parameters	BC	Case B	Case C	Case D	Case B	Case C	Case D
Capacitor size (kVAr)/bus no.	–	11 (300) 18 (300) 61 (1200)	11 (300) 18 (300) 61 (1200)	11 (450) 18 (450) 61 (1050)	11 (300) 18 (300) 49 (600) 61 (1200)	11 (300) 18 (300) 49 (600) 61 (1200)	11 (450) 18 (450) 49 (750) 61 (900)
Switch status	69–70–71–72–73	69–70–71–72–73	69–70–14–58–63	69–70–14–58–61	69–70–71–72–73	69–70–14–58–62	69–70–14–58–61
P_{Loss} (KW)	225.00	145.13	68.1766	66.9995	144.3847	67.613	**66.02**
Q_{Loss} (KVAr)	102.1155	67.7124	62.9619	62.1159	65.8195	62.1096	60.4519
% P_{Loss} reduction	–	35.49777	69.7	70.22244	35.82902	69.9497	**70.65777**
V_{min} (p.u.)/bus no.	0.90919 (65)	0.9308 (65)	0.9683 (62)	0.971 (61)	0.931 (61)	0.9719 (61)	0.9725(64)

Table 12. Comparison of case B – scenario 1 – IEEE 69 bus.

Parameters	SCA [15]	FA [16]	BA [16]	ABC [16]	CSO [16]	DVSA [39]	AGPSO
Capacitor details	379.5 (11) 237.3 (21) 1200 (61)	809 (5) 399 (12) 1288 (50)	29 (3) 198 (9) 1500 (50)	225 (8) 210 (44) 1124 (50)	434 (12) 400 (42) 1175 (50)	300 (11) 300 (18) 1200 (61)	300 (11) 300 (18) 1200 (61)
P_{Loss} (KW)/(P_{Loss} − BC)	145.15/225	145.78/224.8	150.845/224.8	148.89/224.8	145.07/224.8	145.397/225.072	**145.13/225**
Bus voltage (p.u.)	–	0.9319	0.9342	0.9298	0.9317	–	0.9318
% P_{Loss} reduction	35.48889	35.20888	32.95777	33.82666	35.46708	35.39978	**35.49778**

Table 13. Comparison of case B – scenario 2 – IEEE 69 bus.

Parameters	EA (PLI) [8]	EA (LSF) [8]	IWOA [11]	Locust search [12]	PSO [9]	AGPSO
Capacitor details	950 (61) 200 (64) 150 (59) 50 (65)300 (21)	150 (57) 50 (58) 100 (59) 150 (60)1000 (61)	450 (9) 300 (17) 1050 (50) 150 (53)	350 (12) 150 (21) 450 (50) 150 (54)1200 (61)	340 (11) 240 (19) 510 (50) 1190 (61)	300 (11) 300 (18) 600 (49) 1200 (61)
P_{Loss} (KW)/(P_{Loss} − BC)	146.1347/224.8949	151.3763/224.8949	145/224.89	144.25/225	144.50/225	**144.3847/225**
Bus voltage (p.u.)	0.9327 (65)	0.9311 (65)	0.93 (65)	0.9315	–	0.931 1 (65)
% P_{Loss} reduction	35.02	32.69	35.52	35.88888	35.78	**35.829**

0.04 p.u. compared to case C. However, the difference in bus voltage improvement between scenarios 1 and 2 (cases C and D) is minuscule.

By comparing AGPSO with other existing methods in achieving power loss reduction considering cases C and D (scenario1), it is to be noted that the results obtained under case C (scenario 1) minimize the power loss in a better manner than CS [28], MIC [28] and MBFBO [28] and also the minimum and the maximum power loss reduction difference is

Table 14. Results obtained by AGPSO – cases E and F – scenarios 1 and 2 – IEEE 69 bus.

	Scenario 1		Scenario 2	
Parameters	Case E	Case F	Case E	Case F
		DG at single optimal node		
DG size and (node) (KW)	1574 (61)	1453 (61)	1464 (61)	1495 (61)
P_{Loss} (KW)	**21.12**	**20.578**	**20.426**	**20.365**
Q_{Loss} (KVAr)	16.025	16.012	15.546	15.881
Total P_{Loss} reduction	90.6133	90.8542	90.9218	90.9488
Additional P_{Loss} reduction	**20.9133**	**20.632**	**20.9721**	**20.291**
V_{min} (p.u.)/bus no.	0.97237 (64)	0.97372 (64)	0.97248 (63)	0.97397 (63)
V_{max} (p.u.)/bus no.	1.001 (61)	1.0012 (63)	1.0015 (61)	1.001 (61)
		DG at two optimal nodes		
DG size and (node) (KW)	1574 (61), 489 (64)	1434 (61), 465 (64)	1451 (61), 456 (64)	1417 (61), 486 (64)
P_{Loss} (KW)	**9.4357**	**9.0712**	**9.2265**	**8.3639**
Q_{Loss} (KVAr)	7.9112	8.2496	7.6435	7.0346
Total P_{Loss} reduction	95.8064	95.9684	95.9	96.283
Additional P_{Loss} reduction	**26.106**	**25.746**	**25.9503**	**25.6253**
V_{min} (p.u.)/bus no.	0.99147 (68,69)	0.99224 (68,69)	0.99164(68,69)	0.99236 (68,69)
V_{max} (p.u.)/bus no.	1.0015 (61)	1.0018 (61)	1.0024 (61)	1.0016 (61)
		DG at three optimal nodes		
DG size and (node) (KW)	1379 (61), 384 (64), 644 (12)	1418 (61), 490 (64), 537(11)	1450 (61), 493 (65), 536 (11)	1343 (61), 489 (64), 535 (11)
P_{Loss} (KW)	**6.974**	**5.5482**	**6.3765**	**5.2089**
Q_{Loss} (KVAr)	7.5787	6.5783	6.0784	6.5998
Total P_{Loss} reduction	96.9	97.5341	97.166	97.685
Additional P_{Loss} reduction	**27.2**	**26.854**	**27.2163**	**27.0272**
V_{min} (p.u.)/bus no.	0.9927 (24)	0.99513 (50)	0.99328 (63,64)	0.99563 (21)
V_{max} (p.u.)/bus no.	1.0021 (68, 69)	1.0022 (66)	1.0026 (61)	1.0018 (61)

Table 15. Comparison of case F – scenario 1 – IEEE 69 bus.

Ref.	Switch position	DG details	Capacitor details	$P_{Loss\,(kW)}$
LSHADE-EpSin [32]	69–70–14–55–61	310 (12), 313 (21), 1627 (61)	582 (12), 881 (49), 1227 (61)	5.81/225
Multi-objective NSGA-II [34]	20–37–43–57–61	58 (500/0.8 pf), 61 (500/0.8 pf), 65 (500/0.8 pf)	7 (500), 12 (500), 50 (500), 61 (500)	29.748/224.962
Fuzzy-BFO [35]	13–17–47–50–69	350 (11), 615 (18), 1164 (61)	150 (21), 300 (61), 450 (64)	28.87/226.92
Fuzzy-GA [35]	14–47–50–69–70	450 (11), 734 (18) 1324(61)	250 (11), 450 (61), 450(64)	32.17/226.92
Fuzzy-PSO [35]	18–43–56–61–69	350 (18), 615 (61) 1164 (64)	450 (11), 300(49), 450(61)	31.23/226.92
AGPSO	69–70–14–58–61	1418 (61), 490 (64), 537 (11)	11 (450), 18 (450), 61 (1050)	**5.5482/225**

5.4511% and 15.4166%, respectively. Conversely, the power loss reduction achieved by MBBO [28] is 5.88% more than the value achieved by AGPSO. All the five tie switches have been closed against opening of sectionalizing switches except MIC [28]. By comparing the results obtained under case D (scenario 1), it is perceptible that AGPSO minimizes the power loss better than SASHOA[29], BTLBO [30], DDE [30] and also the minimum and the maximum power loss reduction difference is 2.56% and 22.0887%, respectively. Alternatively, the power loss reduction achieved using MBBO [30] is 3.72% in excess of AGPSO. All the five tie switches have been closed against opening of sectionalizing switches in a particular loop except [29].

Similar to IEEE 33 bus system, real power injection at a single to three optimal nodes after cases C and D has been performed in 69 bus test system to prove the performance of AGPSO in achieving further power loss reduction. Table 14 indicates the effect of the real power injection in minimizing the power loss reduction after cases C and D.

An additional power loss reduction of around 21%, 26% and 27%, respectively has been gained by injecting 38 to 41.4%, 50 to54% and 62 to65% of the total real power demand of the network. Thus the total power loss reduction increases to around 91%, 96% and 97.5% after real power injection at a single, two and three optimal nodes, respectively. Note that though considerable value of power loss reduction has been obtained by injecting real power up to three optimal nodes, it is economically preferable to select only DG at a single node after cases C and D because selecting the second and third node for real power injection will not yield sufficient power loss reduction compared to real power injection. Table 15 reveals the comparison of case E

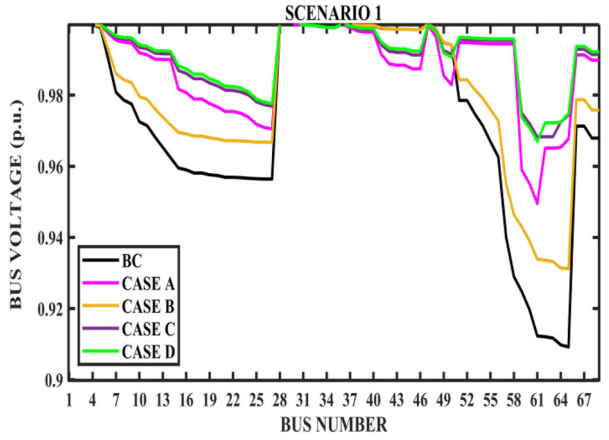

Figure 10. Bus voltage profile – cases BC to D – scenario 1.

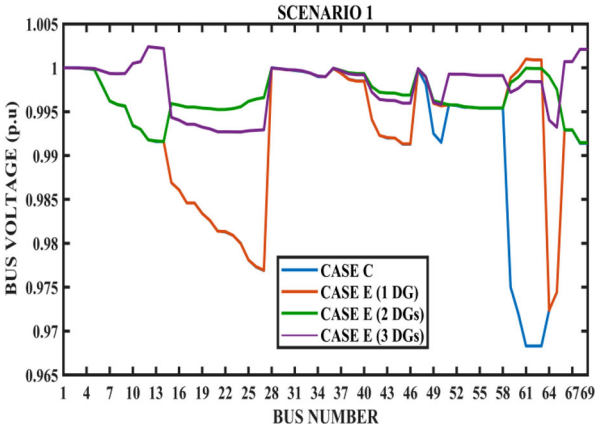

Figure 12. Bus voltage profile – cases C and E – scenario 1.

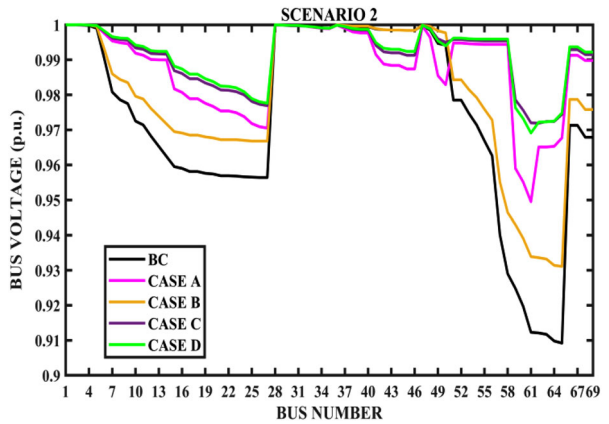

Figure 11. Bus voltage profile – cases BC to D – scenario 2.

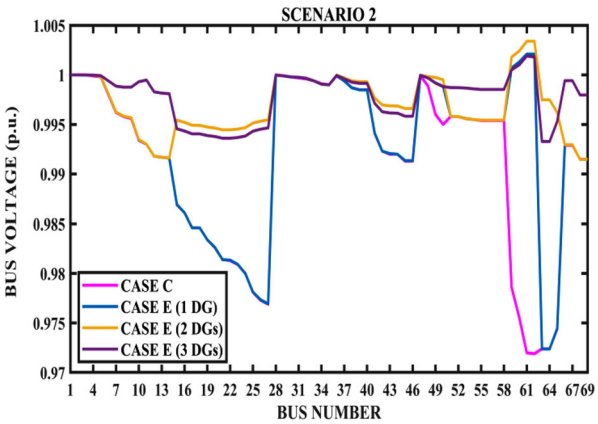

Figure 13. Bus voltage profile – cases C and E – scenario 2.

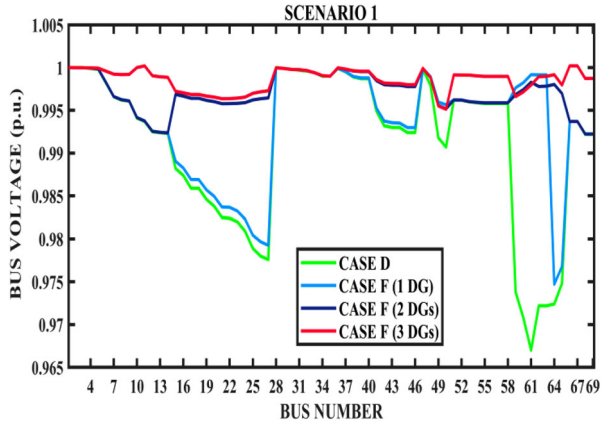

Figure 14. Bus voltage profile – cases D and F – scenario 1.

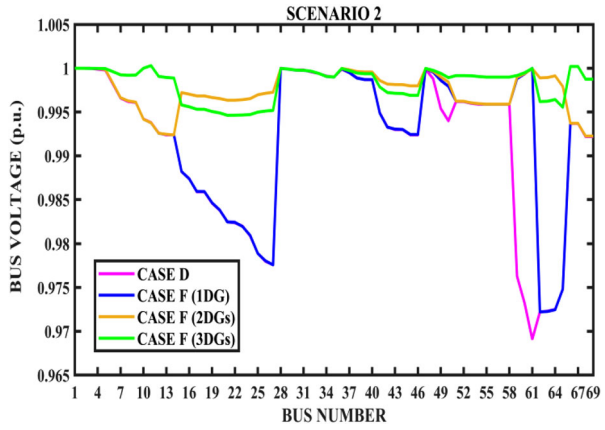

Figure 15. Bus voltage profile – cases D and F – scenario 2.

(scenario 1) with the existing methods. It is visible that the proposed method minimizes the power loss better than [32, 34, 35]. The maximum power loss reduction difference between [35 (Fuzzy-GA)] with AGPSO is 10.7577% and the power loss reduction difference between [32] with AGPSO is minuscule.

Figures 10 and 11 show the bus voltage profile from BC to D (scenarios 1 and 2) and Figures 12–15 show the bus voltage profile for the cases C to F considering both scenarios.

5. Conclusions

In this work, an evolutionary computation (AGPSO) has been suggested to solve the power loss minimization problem using a combination of CA (at three/four optimal nodes) with and without NR under four different configurations and also allocation and sizing of DGs at single, two and three optimal nodes in reconfigured capacitive compensated radial DN. IEEE 33 and 69 bus test systems are used to evaluate the power loss reduction as well as additional power loss reduction (using DGs). Based on the above study, the following are the important observations:

(1) In this work no sensitivity factor has been adopted to find the optimal location for capacitor/DG placement. AGPSO has to search for optimal location and sizing of Capacitor and DGs
(2) The power loss reduction of DN can be effectively and efficiently minimized by proper NR with allocation and sizing of capacitors at three/four optimal nodes compared with other existing methods.
(3) Allocation and the sizing of DGs from single optimal node to three optimal nodes beyond reactive power injection with NR (cases C and D) have been performed to achieve additional power loss reduction.
(4) Around 60% of real power loss reduction is achieved by using capacitors with NR and a maximum additional power loss reduction of around 35% is achieved by injecting around 88% of the total real power demand at three optimal nodes (33-Bus)
(5) The maximum bus voltage enhancement recorded for the cases E and F is 1.0054 p.u.
(6) Since the difference in power loss reduction between scenarios 1 and 2 under cases B to D is very small, it is desirable to limit the reactive power compensation up to three nodes only.

Thus the proposed algorithm (AGPSO) provides an effective solution since it gives a promising and accepted performance over other algorithms in terms of real and reactive power loss reduction and bus voltage profiles.

Disclosure statement

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Nomenclature

BC	Base case
AC	After compensation
ADGI	After DG installation
BDGI	Before DG installation
TNB	Total no. of branches (TB-1)
TB	Total no. of buses
MS	Main source
P_{MS}	Total active power supplied by the main source (kW)
Q_{MS}	Total reactive power supplied by the main source (kVAr)
P_D, Q_D	Total active and reactive power demand in kW/kVAr, respectively
N_{DG}	Total no. of DG units
NC	Total number of nodes demanding reactive power compensation (1–4)
$Q_{C(i)}$	Capacitance of the capacitor at ith node (each rated 150 kVAr)
$Q_{C(i)}^{\min}$	Minimum reactive power injection by capacitor at ith node (150 kVAr)

$Q_{C(i)}^{max}$	Maximum reactive power injection by capacitor at *i*th node (2100 kVAr)
$P_{DG(i)}$	Total active power supplied by DG at *i*th node (kW)
$P_{DG(i)}^{min}$	Minimum real power generated by DG unit at *i*th node (kW)
$P_{DG(i)}^{max}$	Maximum real power generated by DG unit at *i*th node (kW)
P_{TL}	Total active power loss (kW)
Q_{TL}	Total reactive power loss in (kVAr)
V_i^{min}	Minimum voltage at *i*th node (0.95 p.u.)
V_i^{max}	Maximum voltage at *i*th node (1.05 p.u.)

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