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A Modified Three Leg Watkins Johnson Bridge Type DC to DC Converter Simulation and Experimental Verification

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Abstract: In this work, a novel, high boost, DC-to-DC converter topology is proposed and validated. The proposed topology is an extension of the existing two leg bridge type Watkins Johnson DC to DC converter. In the proposed system, an additional leg is included along with an additional inductor and an additional capacitor. The inclusion of the third leg to the existing, two-leg version of Watkins Johnson DC–to-DC bridge type converter helps to boost further the voltage gain. This paper presents the proposed topology and a detailed analysis of the topology using the circuit model in the MATLAB SIMULINK simulation environment. An experimental prototype was also developed to validate the proposed idea. The results obtained from the simulations and the experimental prototype are also presented herein. The studies were carried out with open loop configuration.

Keywords: DC to DC converters; High Voltage gain DC to DC converters; Modified Watkins Johnson Converter; Watkins-Johnson converter

1 INTRODUCTION

DC to DC converters are indispensable power electronic converters which have numerous applications [1-7]. There are many configurations of DC to DC converters available, typically, the generic buck, boost and the buck boost converters. It is necessary for certain applications that the available DC voltage is boosted out with a large voltage gain and that the converter system is stable as well [8-12].

The Watkins Johnson Converter (WJC) is a DC to DC converter, offering high voltage gain, with just a few storage elements [13]. The WJC uses more number of switches with the possibility of increased switching losses. The main advantage of the WJC is that it can give either a positive output voltage or a negative output voltage with just the duty cycle control. For duty cycles less than 0.5 towards 0 the output voltage is negative with respect to the source voltage and with duty cycles greater than 0.5 towards 1 the polarity of the output voltage is the same as that of the input voltage. For changing the polarity of the output voltage, the bridge type WJC does not require a change in the topology.

There have been only a limited number of research articles published on the Watkins Johnson topologies and some milestone contributions have been considered herein. In the research contribution [14] the authors have demonstrated the merits of the Inverse WJC. Similarly, in the work [15], the authors have developed a high buck DC to DC converter suitable for applications in automobiles. In this work a step down WJC has been presented for converting the 42 V DC voltage source into a 3 V DC voltage source. These topologies belonging to the Watkins Johnson family use a taped inductor.

A multi input modified Inverse Watkins Johnson converter (IWJC) with coupled inductors has been presented by the authors in [16]. According to the work in [17] it is claimed that with the WJC the matrix of tapped inductor based DC to DC converters has become complete.

A solar powered base station for communication systems that uses a WJC has been proposed and validated by the authors in [18]. In the work presented in [19] the authors have demonstrated the mitigation of the common mode noise that appears in the WJC. A switched boost inverter has been developed by the authors in [20] and the proposed system uses the IWJC as the core power conversion system. The same work was further modified and an improved version of the inverter that uses the WJC has been presented in [21] by the same authors of [20]. More recently a water pumping system has been developed and demonstrated by the authors in [22].

However there is no single work that has made a topological change by augmenting a third leg to the existing two leg format and enabled the system to render increased voltage gain.

In this work, the topology of the existing two legs WJC is modified by augmenting one more legs with two additional power electronic switches and an additional inductor and a capacitor. The proposed work does not use any taped inductor but uses two separate inductors and they are not magnetically coupled.

A circuit model has been developed in the MATLAB SIMULINK environment and the results have been presented. The transfer function of the proposed Modified Watkins Johnson converter (MWJC) has been obtained and the basic cybernetic studies like the Bode plot and the Root Locus plot have been presented for the open loop system.

A comparison of the voltage gains of the WJC, the IWJC and the proposed MWJC is shown in Tab. 1.

Table 1 Comparison of voltage gain of WJC, IWJC and the MWJC

Topology	Voltage gain	$D = 0.1$	$D = 0.6$
WJC	$M = (2D - 1)/D$	–8	1/3
IWJC	$D/(2D - 1)$	–1/8	3
MWJC	$M^2 – M$(Boost)72	-	-
MWJC	$M – M^2$(Buck)	-	2/9
	Where $M = (2D - 1)/D$		

In this work, an analysis is done on the proposed three legs MWJC. This paper focuses on the derivation of the voltage gain and the methodology of developing a circuit model in MATLAB SIMULINK environment and also the development and testing of an experimental prototype. The paper is arranged as follows. Next to this brief introduction a review of the basic WJC and the topology of the MWJC are discussed in section 2. The circuit model simulations in the MATLAB SIMULINK environment are presented in section 3. The details of experimental verification are

presented in section 4 with a discussion on the results obtained. The Conclusion and the reference sections follow.

2 THE EXISTING AND THE PROPOSED WJCS

2.1 A Review of the Existing Bridge type WJC

Fig. 1 shows the topology of the existing two leg WJC. The WJC can be viewed to have two modes of operation. In mode 1 the Switch module SW1, the inductor L, Switch module SW2 and the capacitor C are connected in series and the whole connected across the input voltage V_{in}. The voltage across the Capacitor C is the output voltage V_{out}. This mode of operation is maintained for a period D in a switching cycle. During the period $1 - D$ the switch modules SW3 and SW4 are turned on while SW1 and SW2 are turned off.

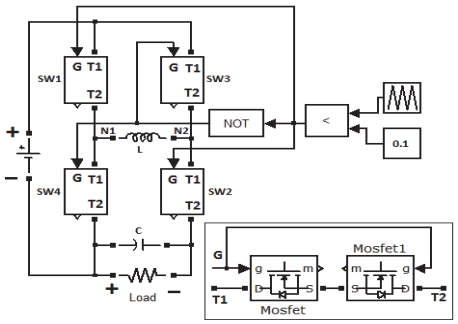

Figure1 The basic Watkins Johnson Bridge type DC-to-DC converter

Thus two voltage Eq. (1) and Eq. (2) are formed.

$$V_{LD} = V_{\text{in}} - V_{\text{out}} \tag{1}$$

$$V_{L(1-D)} = -V_{\text{in}} \tag{2}$$

where V_{in} is the input voltage, V_{out} the output voltage, V_{LD} is the voltage across the inductor L for period D and $V_{L(1-D)}$ is the voltage across the inductor L for period $(1 - D)$. In order to maintain volt second balance:

$$(D)(V_{LD}) = (1-D)\left(V_{L(1-D)}\right) = 0 \tag{3}$$

$$(V_{\text{in}} - V_{\text{out}})D + (-V_{\text{in}})(1-D) = 0 \tag{4}$$

This equation can be reduced to the form shown as Eq. (5):

$$V_{\text{out}}/V_{\text{in}} = (2D-1)/D \tag{5}$$

Going by an example, if $V_{\text{in}} = 12$ V and $D = 0.25$ then:

$$V_{\text{out}} = V_{\text{in}} \times (-2) = -24$$

Thus, for an input voltage of 12 V, the output voltage becomes -24 V for a duty cycle of 0.25. According to the topology, the source and the load share a common terminal. With reference to this common terminal the output voltage is negative as compared to the input or source voltage V_{in}.

2.2 The Proposed Three leg DC to DC Converter

The proposed three leg DC to DC converter referred to as the Modified Watkins Johnson Converter (MWJC) is a development of the basic WJC. Fig. 2 shows the topology of the proposed MWJC converter. The proposed topology consists of the basic WJ converter with an extra leg. In addition to the basic Inductor L and C, used in the two leg topology, now named as $L1$ and $C1$, respectively in the proposed three leg topology an Inductor $L2$ and a capacitor $C2$ are also included.

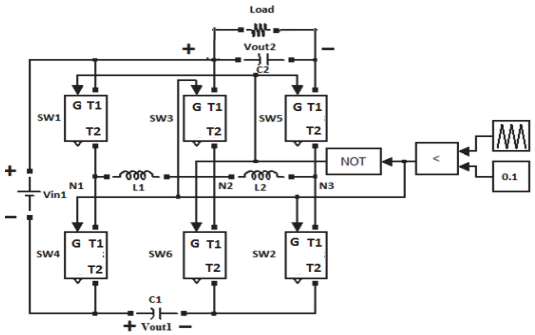

Figure 2 The Topology of the Proposed MWJC Converter

The load is connected across the capacitor $C2$. With reference to the circuit diagram shown in Fig. 2, for the proposed MWJC, let the source voltage be V_{in1} and the output voltage be V_{out2}. The power electronic switch modules $SW1$, $SW6$ and $SW5$ form one set. The power electronic switch modules $SW4$, $SW3$ and $SW2$ form the other set. These two sets are turned on and off in a complementary fashion and this leads to two basic modes of operation.

In the first mode of operation as shown in Fig. 3 the switch modules $SW1$, $SW6$ and $SW5$ are turned on while the other three switch modules are in the off state. In the second mode as shown in Fig. 4 the switch modules $SW3$, $SW4$, and $SW2$ are turned on while the other three switch modules are in the off state. The voltage build up mechanism and the derivation for the voltage gain of the proposed topology are presented in the following section.

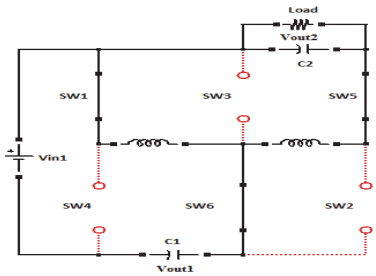

Figure 3 Mode 1 $SW1$, $SW6$, $SW5$ On; $SW2$, $SW3$, $SW4$ Off

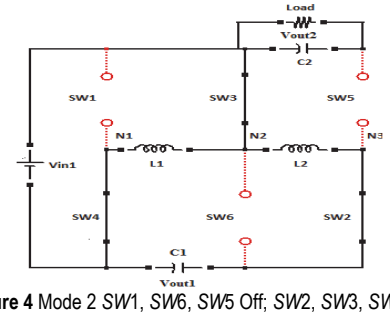

Figure 4 Mode 2 $SW1$, $SW6$, $SW5$ Off; $SW2$, $SW3$, $SW4$ On

2.3 The Steady State Voltage Gain

The steady state voltage gain of a power electronic converter can be obtained using the fundamental volt second balance method applied to the voltage across the inductor or by using the state space model [23-25]. These studies help to get an insight into the open loop characteristics of the converters and also help to design closed loop controllers as well. They are useful for the design of Maximum Power Point tracking when used with renewable energy sources like the solar Photo voltaic energy harvesting systems [26].

The proposed MWJC with three legs can be treated as the extension of the existing *WJC*. Considering the three leg configuration as discussed in this paper, the first two legs may be treated as the two legs of the basic unit, the *WJC*1; the second and the third legs can be treated as the first and the second legs respectively of the second unit, *WJC*2. Since the centre leg is common for the two *WJC*s, when its switch modules operate in complemented form it maintains the two converter stages to be operating simultaneously in the same modes. When the first stage (*WJC*1) is in mode 1 the second stage (*WJC*2) is also in mode 1 and this is true with mode 2 as well. It is to be noted that the capacitor *C*1 of the first stage is in the lower rail while the position of the capacitor *C*2 for the second stage is shifted to the upper rail.

In the existing two leg WJC the DC output is drawn across the capacitor *C*1. In this modification, by a consideration of the topology as shown in Fig. 2 it can be seen that the input voltage to the second stage is the sum of the DC input voltage and the output voltage of the first stage, which appears across *C*1. That is, $V_{in2} = V_{in1} + V_{out1}$. By considering the positive terminal of the source voltage V_{in1} as the reference to the second stage:

$$V_{inw} = -\left(V_{in1} + V_{out1}\right) \tag{6}$$

From Eq. (5) the voltage gain M1 of the first stage is:

$$M = V_{out1}/V_{in1} = -\left(2D-1\right)/D \tag{7}$$

Since the topology for the first and the second stage is similar, the gain of the second stage is the same as that of the first stage and is given by the relation.

$$M2 = V_{out2}/V_{in2} = \left(2D-1\right)/D \tag{8}$$

In Eq. (8) V_{out2} is the output voltage of the second stage of the MWJC converter and V_{in2} is the input voltage to the second stage. The structure of the voltage boost mechanism is clearly shown in Fig. 5. For getting the voltage output of the first stage, Eq. (5) is used and the input to the second stage is:

$$V_{in2} = \left(V_{in1}\left(2D-1\right)/D\right) - V_{in1} \tag{9}$$

$$V_{out2} = \left(V_{in2}\left(2D-1\right)/D\right) \tag{10}$$

$$V_{out2} = \left(\left(V_{in2}\left(2D-1\right)/D\right) - V_{in1}\right)\cdot\left(\left(2D-1\right)/D\right) \tag{11}$$

If the voltage gain $\left(\left(2D-1\right)/D\right)$ of the two stages is denoted by $M1 = M2 = M$ then:

$$V_{out2} = \left(\left(V_{in2}\cdot M\right) - V_{in1}\right)\cdot M \tag{12}$$

Going by an example, if D the duty cycle is 0.1:

$$\begin{aligned} M &= \left(2D-1\right)/D \\ M &= \left(\left(2\cdot 0.1\right)-1\right)/0.1 = -8 \end{aligned} \tag{13}$$

The overall gain of the MWJC will therefore be:

$$V_{out2} = \left(\left(V_{in2}\cdot -8\right) - V_{in1}\right)\cdot -8$$

If V_{in1} = 12 V with a duty cycle of D = 0.1 the output of the first stage is $= 12\cdot -8 = -96$ V . The input voltage to the second stage is $-96-12 = -108$ V . The voltage output of the second stage is:

$$V_{out2} = -8\cdot\left(-108\right) = 864 \text{ V}$$

Also, by recalling Eq. (12):

$$V_{out2} = \left(\left(V_{in1}\cdot M\right) - V_{in1}\right)\cdot M \tag{14}$$

It can be shown that $V_{out2}/V_{in1} = M^2 - M$ and therefore, if G is the overall voltage gain then:

$$G = V_{out2}/V_{in1} = M^2 - M \tag{15}$$

For example, consider D = 0.2:

$$M = \left(2D-1\right)/D = \left(0.4-1\right)/0.2 = -3$$

The overall voltage gain becomes:

$$G = M^2 - M = \left(-3\right)^2 + 3 = 12$$

With V in 1 = 12 and a Duty cycle of 0.2 the output voltage becomes:

$$V_{out2} = G\cdot V_{in1} = 12\cdot 12 = 144 \text{ V}$$

The proposed three leg MWJC was developed in the MATLAB SIMULINK environment. The source voltage, the load resistance and the values of other components are as shown in Tab. 2. With reference to Tab. 3, for a given input voltage of 12 Volts, for a load resistance of 100 Ohms the output voltage for a duty cycle of 0.1 was found to be 864 Volts as compared to the output of the two leg WJC, the proposed MWJC has drastically increased the voltage gain.

Table 2 The list of components

Component	Values
Power Electronic Switch Modules (*S*1, ..., *S*6)	MOSFET
Inductor *L*1 = *L*2	1 milliHenry
Capacitors *C*1 = *C*2	470 Micro Farad
Source voltage	DC 12 V
Load	100 Ohms

All the discussions so far are applicable for the steady state condition. The steady voltage gain of the proposed converter for modulation indices 0.1 to 0.4 has been plotted as shown in Fig. 6.

Table 3 Voltage gain and output Voltage (Vin1 = 12 *V*)

Duty	$M = (2D - 1)/D$(Ref.13.Page261)	$M2 - M$ (Proposed)	V_{out2}
0.1	−8	72	864
0.2	−3	12	144
0.3	−1.33	3	36
0.33	−1	2	24
0.4	−0.5	0.75	09

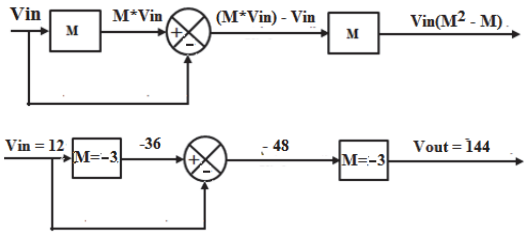

Figure 5 Pictorial representation of the Voltage Boost Mechanism

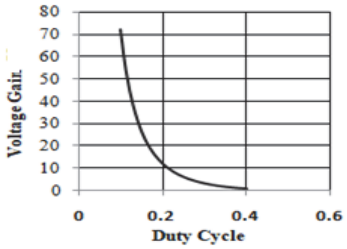

Figure 6 Voltage gain Versus Duty cycle for D from 0.1 to 0.4.

The circuit model of the proposed three leg MWJC was developed in the MATLAB SIMULINK environment and the details are presented in section 3.

3 THE SIMULATION OF THE CIRCUIT MODEL OF THE MWJC IN MATLAB SIMULINK

In this section the open loop performance of the circuit model of the proposed MWJC as realized in the MATLAB SIMULINK environment is presented. In the following sections the operational details of the MWJC are considered for boost operation only for which the duty cycles lie in the range 0 to 0.5 excluding 0.

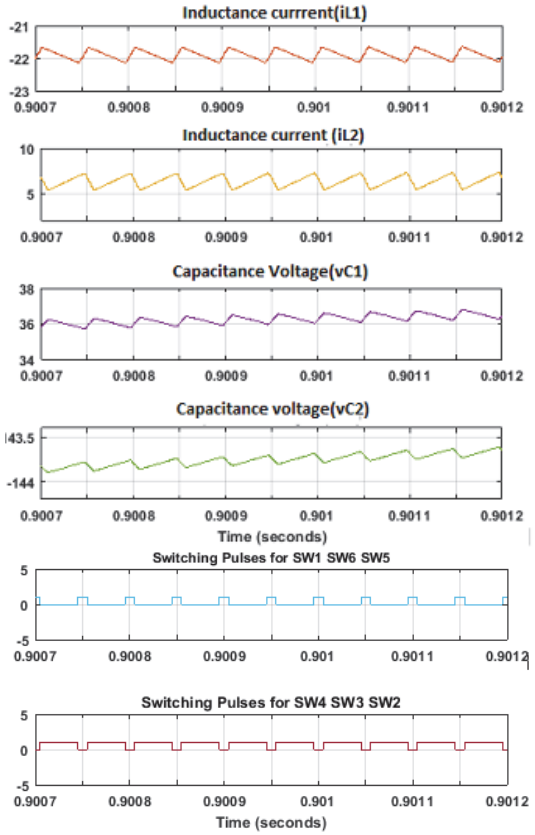

Figure 8 The waveforms obtained from simulation of the Circuit Model.

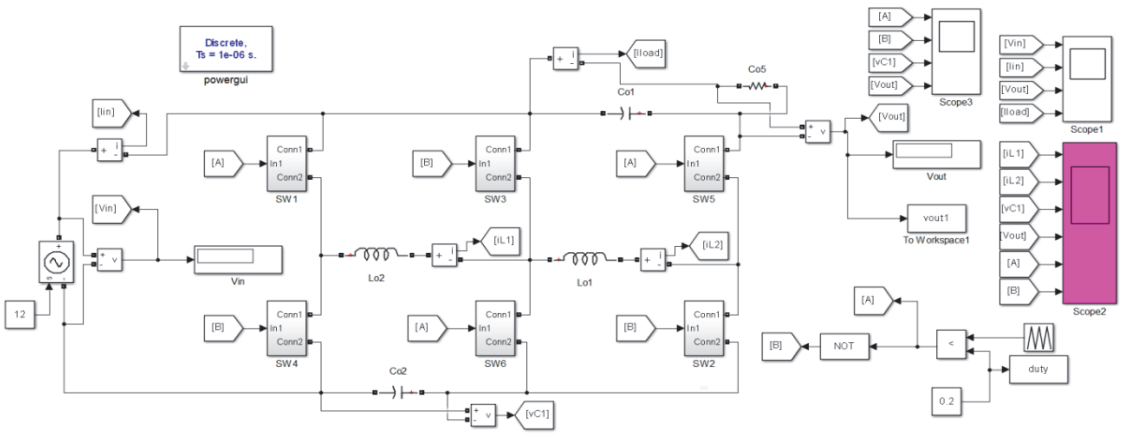

Figure 7 The complete circuit model in MATLAB SIMULINK

The MATLAB SIMULINK based circuit model has been developed and is as shown in Fig. 7 and the results obtained are shown in the wave forms given in Fig. 8. It has been established in Eq. (15) that the overall voltage gain of the converter is $V_{out2}/V_{in1} = M^2 - M$. If D is 0.1 then $M = (2 \times 0.1 - 1)/0.1 = 0.8/0.1 = -8$.

Considering the polarities the input voltage V_{in1} and the output voltage of the first stage V_{out1}, which appears

across capacitor $C1$, V_{in1} and V_{out1} can be added to be the input for the second stage. The overall gain for a duty cycle D of 0.1 is 64 – (−8) = 72. If the source voltage V_{in1} is 12 V then the output of the second stage, which is the overall output will be 72 × 12 = 864 volts.

For a duty cycle of D = 0.5 the voltage gain M of the first stage is $M = (2 \times D - 1)/D = 0$. The overall voltage gain = $M^2 - M = 0$. For boost operation, the duty cycle is to be selected in the range between 0 and 0.5. The plot of the transient and steady state output voltage for a duty cycle of 0.2 is shown in Fig. 9.

The important parameters are Input voltage =12 V; Output Voltage = 144 V; Load R = 100 Ohms and the Switching Frequency = 5 KHz.

4 TRANSFER FUNCTION USING MATLAB SIMULINK

While the circuit model of the proposed MWJC in the open loop mode was simulated in MATLAB SIMULINK, the duty cycle D (denoted as 'duty') and the output voltage V_{out2} (denoted as 'out') were routed to the MATLAB workspace and the transfer function of the proposed MWJC relating V_{out2} and the duty cycle D has been estimated and it is as shown in Eq. (16).

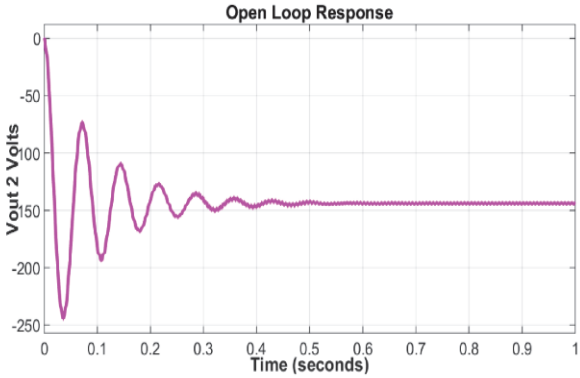

Figure 9 The output voltage of the MWJCwith D = 0.2

The following commands were invoked from the MATLAB command line.

> mysys = iddata(out, duty,.0001)

> sys = tfest(mysys, 4) /////The model approximated to a fourth order system)

The step response of the obtained transfer function is found by the command

> step (12*sys)

The input is 12 V and the step response of the transfer function was compared and found to be in compliance with the step response of the MATLAB SIMULINK circuit model as shown in Fig. 9.

$$sys = \frac{4281s^3 - 1.327\times10^7 s^2 + 9.738\times10^7 s - 5.259\times10^{12}}{s^4 + 24.72s^3 + 9.449\times10^5 s^2 + 1.88\times10^7 s + 7.313\times10^9} \qquad (16)$$

When the circuit model is approximated to a fourth order transfer function as given in Eq. (16) there are four poles and these four poles are found to lie on the left half of the complex plane in the root locus diagram as shown in Fig. 10. The bode plot was also plotted and is as shown in Fig. 11. As indicated by the root locus, the system is stable with all the poles on the left half plane.

However there are singularities at certain frequencies as shown in the bode plot. This issue can be resolved in the closed loop control scheme typically using a Sliding Mode Controller [27-30].

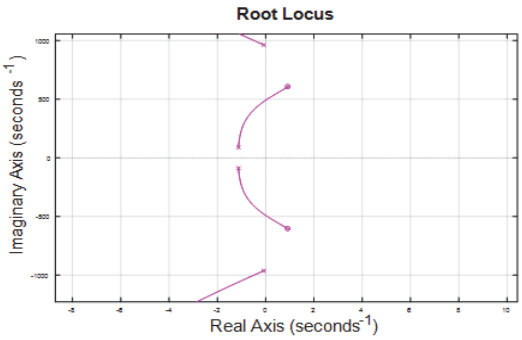

Figure10. The Root Locus of the transfer function

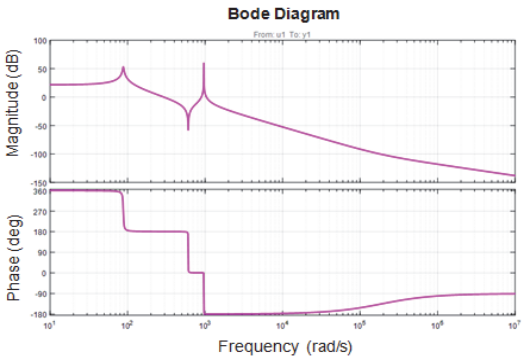

Figure11 The Bode plot of the transfer function

5 EXPERIMENTAL SETUP AND RESULTS

An experimental setup has been constructed and tested to validate the proposed idea. The photograph of the prototype model is shown in Fig. 12.

The specifications of the components used for the prototype are shown in Tab. 4. The PIC micro controller PIC 16F877A was used as the controller for the prototype. The design used the lower order six bits of the total of eight bits of port B of the micro controller. Bits D0 through D5 were used respectively for MOSFETs based switching modules SW1 through *SW*6. Tab. 5 was used to generate the data bits to drive the Switching Modules. The MOSFETs used in the experimental verification have internal body diodes. Therefore, it is sufficient to turn on only three switches for the period D (or $(1 - D)$) and the internal diodes of the other three switches conduct during the complementary period.

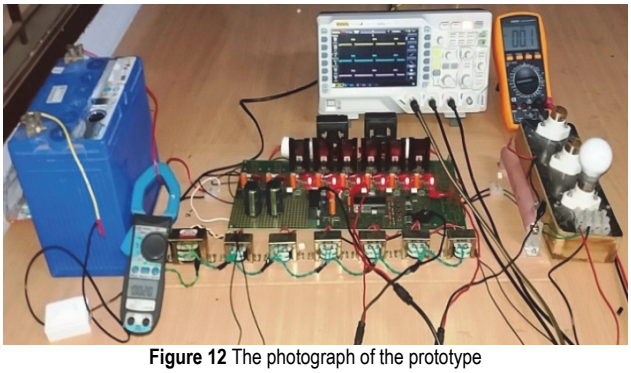

Figure 12 The photograph of the prototype

If a voltage gain of 12 is required, a duty cycle of D = 0.2 is to be applied to switches $SW1$, $SW5$ and $SW6$. This is implemented by the application of a duty cycle of 0.8 (1 − D) to switching modules $SW2$, $SW3$ and $SW4$ as shown in Fig. 13. The internal diodes in switches SW1, SW5 and $SW6$ conduct for the rest of the cycle period. It is not necessary that the two sets of three switches be operated in complementary form by the explicit application of complementary switching pulses.

Table 4 Specifications for Experimental Setup

Component	Specification
Vin	12 V DC
Nominal Vout2	144 V DC
$L1 = L2$	1 milliHenry
$C1 = C2$	470 Micro Farad
Power Electronic Switches	IRF 840
Opto Coupler	MCT 2E
Switch. Freq.	5 KHz
Load	R = 100 Ohms
Nominal Power Output	180 − 200 Watts

Table 5 Switch Modules Turned On for the Boost operation

Duty	$D5$ ($SW6$)	$D4$ ($SW5$)	$D3$ ($SW4$)	$D2$ ($SW3$)	$D1$ ($SW2$)	$D0$ ($SW1$)
$1 - D = 0.8$	0	0	1	1	1	0
$D = 0.2$	0	0	0	0	0	0

The corresponding data bytes used in the micro controller program are shown in Tab. 6.

Table 6 Data Bytes for different Modes

Mode	Byte
Period (1 − D)	0 × 0E
Free Wheel period (D)	0 × 00

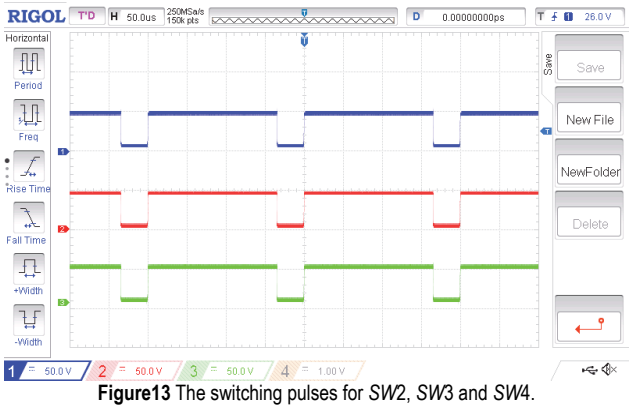

Figure13 The switching pulses for $SW2$, $SW3$ and $SW4$.

With a duty cycle of 0.5, as shown in Fig. 14, the voltages across the inductors L1 and L2 are equal and these two voltages were recorded and are as shown in Fig. 15.

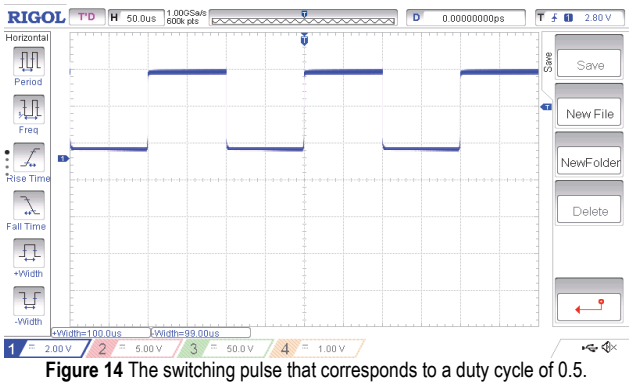

Figure 14 The switching pulse that corresponds to a duty cycle of 0.5.

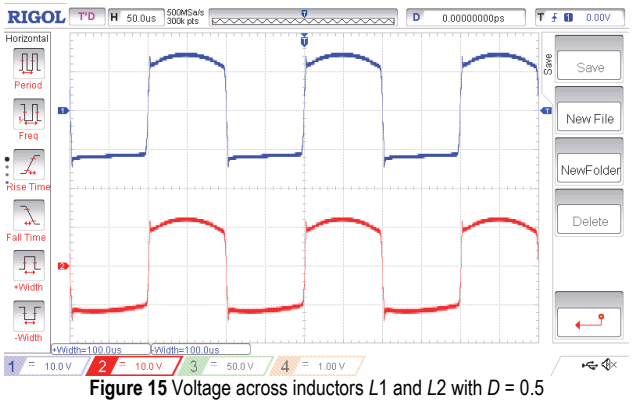

Figure 15 Voltage across inductors $L1$ and $L2$ with D = 0.5

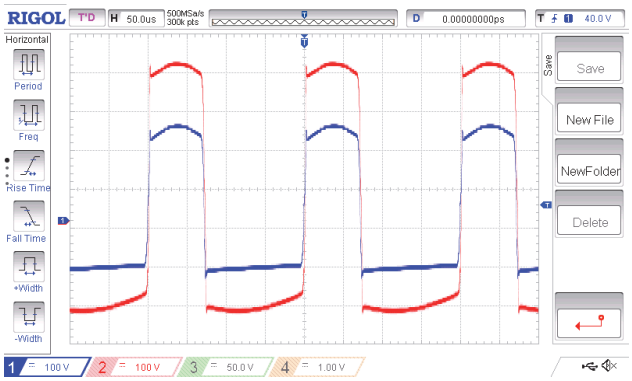

Figure 16 The voltage across the inductors $L1$ and $L2$ with duty cycle = 0.3

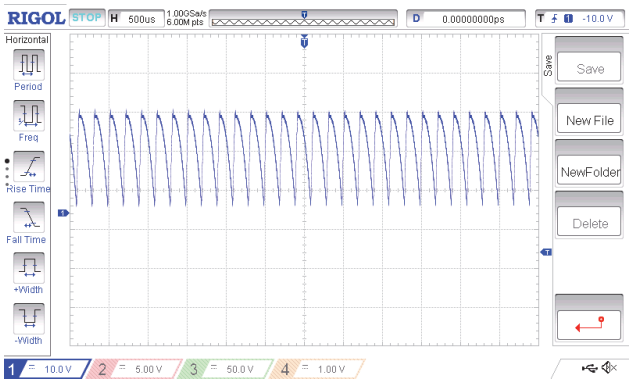

Figure 17 The voltage across the capacitor $C1$ exhibiting a DC average voltage while the duty cycle is at 0.1

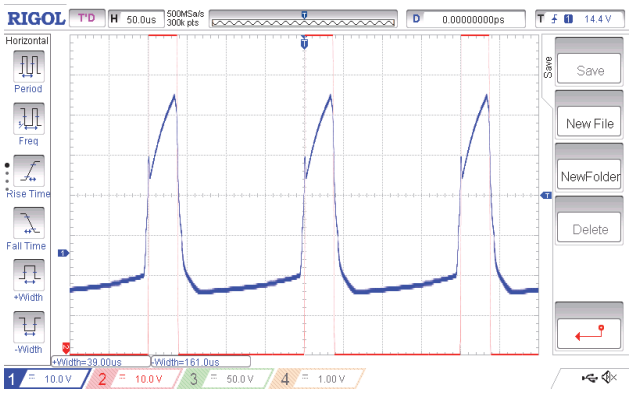

Figure 18 Voltage across inductor $L1$ and $L2$ for a duty cycle of 0.1.

With duty cycle = 0.5 the output voltage of the first stage, across the capacitor $C1$ and the output of the second stage, which is the output of the MWJC, across the capacitor $C2$ were observed to be zero. With a duty cycle of 0.3 the voltages across the inductors $L1$ and $L2$ become unequal and these two voltages were recorded and are as

shown in Fig. 16. It is to be noted that with reference to Fig. 15 and Fig. 16 the average voltage across the inductors $L1$ and $L2$ over every switching cycle is zero. Fig. 18 shows the voltage across the inductor $L1$ in blue and the average value of the voltage across $L1$ is also zero.

The main segment of the control program used is as follows.

```
While (1)
{
PORTB = 0x0E;//Switches SW2, SW3, SW4 ON Mode 1///// (1-D)
Delay (180);
PORTB = 0x00;  //Free Wheel Time////// (D)
Delay (20);
}
```

With reference to the program segment, considering the conduction period of switches SW2, SW3 and SW4 (data:0x0E) corresponding to duty $(1 - D)$ and the freewheeling period D the duty cycle is $20/(180 + 20) = 20/200 = 0.1$ the output voltage for a duty cycle 0.1 will be $M = ((2 \times 0.1) - 1)/0.1 = -8$. And $M^2 = 64$ and $M^2 - M = 72$ and therefore $V_{out2} = 12 \times 72 = 864$. In both simulation and experimental verification it is the period $(1\text{-}D)$ during which the inductor is connected across the source and during the period D the power flows to the load. Therefore in the experimental verification it is only during the period $(1 - D)$ the switches $SW2$, $SW3$ and $SW4$ are turned on whenhe inductor gets charged and during period D the diodes inside $SW1$, $SW5$ and $SW6$ freewheel to drive a part of the stored energy to the load and the remaining part back to the source. Similarly, by considering another set of switch on and freewheel period of 160 and 40 micro seconds respectively the period of conduction $(1 - D)$ will be (160)/200 and freewheeling period $D = 40/200 = 0.2$. In these considerations the total period of 200 Micro Seconds corresponds to 5 KHz switching frequency. The maximum output voltage for the duty cycle 0.2 will be $M = ((2 \times 0.2) - 1) / 0.2 = -3$. This implies $M^2 = 9$ and $M^2 - M = 12$ and $V_{out2} = 12 \times V_{in1} = 144$ V.

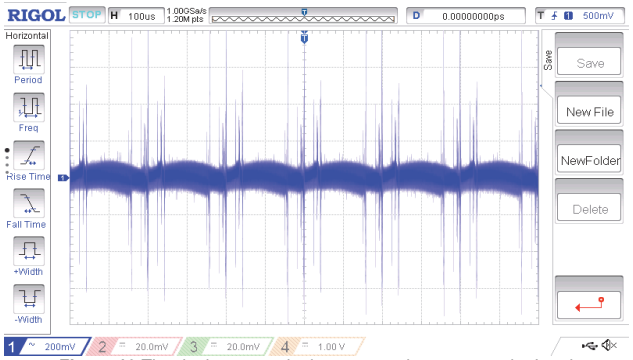

Figure 19 The ripple content in the output voltage across the Load

Further, with a duty cycle of 0.1 the average output voltage across the capacitor $C1$ is DC and the waveform is as shown in Fig. 17. With a duty cycle of 0.1 the voltages across the inductors $L1$ and $L2$ widely differ and they are as shown in Fig. 18. In this case the peak value of the voltage across the inductor $L2$ is much higher than that of the inductor $L1$ as shown in Fig. 18. The ripple that comes along with the overall DC output voltage that appears across the load is shown in Fig. 19. The peak ripple voltage has been observed to be 0.2 V and the actual output voltage observed was 141.6 instead of the theoretical value of 144V.

Yet in another experiment, an output voltage of 96.6V was obtained when it was intended to get 100 V by adjusting the duty cycle D to 0.226, while D = 45 Micro Seconds and $(1 - D) = 155$ micro seconds, for which the value of $M = -2.42$. The theoretical value of the overall voltage gain is 8.3. A drop of about (100 – 96.6) 3.4 V was observed which could be attributed to the voltage drops occurring across the switches and the practical inductors and the approximations in measurements. Fig. 20 shows the DC output voltage that appears across the load.

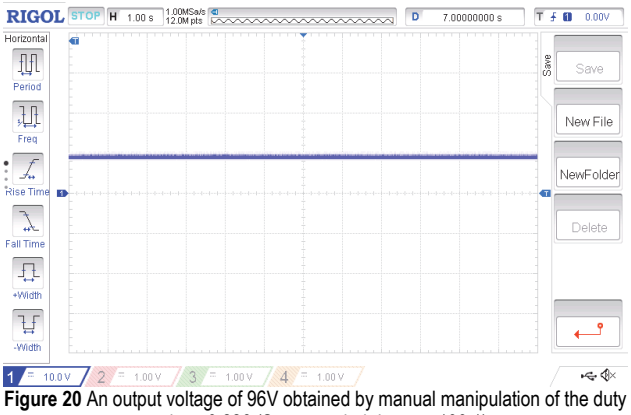

Figure 20 An output voltage of 96V obtained by manual manipulation of the duty cycle to 0.226 (Scope scaled down to 100:1)

6 CONCLUSION

A modified WJC with novel three leg bridge structure has been proposed and validated. The overall voltage gain G of the MWJC, for duty cycles in the range $0 < D < 0.5$ has been found to be $G = M^2 - M$ where M is the voltage gain of the individual stages. Similarly, the overall voltage gain G of the MWJC, for duty cycles in the range $0.5 < D < 1$ has been found to be, $G = M - M^2$. The proposed MWJC gives a very high voltage gain for duty cycles from 0 to 0.5 while it provides a steep buck output for duty cycles from 0.5 to 1. The output is 0 V for duty cycles D = 0.5 and D = 1. The maximum output voltage obtainable in the buck mode is $0.25 \times V$ in for a duty cycle of 0.67.

The proposed MWJC has been validated using simulations of the circuit model in the MATLAB SIMULINK environment and an experimental hardware prototype.

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