ISSN 1330-3651 (Print), ISSN 1848-6339 (Online)
https://doi.org/10.17559/TV-20201006231717
Preliminary communication

A Comparative Study on Applicability of Parallel Resonance Type Fault Current Limiters in Power Systems

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Abstract: In this study the proposed series-parallel resonance-type fault current limiter (SPRFCL) is compared with other parallel resonance-type FCLs (fault current limiter) recommended in the literature for symmetrical and asymmetrical faults to reveal its applicability. The first aim of resonance circuits is to effectively limit the increasing fault current at an allowable value after a fault happened. As a second goal, maintaining the PCC (point of common coupling) voltage at its nominal value during the fault has been handled to carry out the grid code requirements and to protect the sensitive loads connected to this point. Among all FCLs, SPRFCL has been the most efficacious limiter that can successfully suppress fault currents in different fault types and preserve the level of PCC voltage at the duration of the fault. Also, it has an advantageous design in terms of occurred instantaneous power losses on it and the maximum voltage and current levels of semiconductor switches.

Keywords: instantaneous power loss; resonance type fault current limiter; total energy consumed; voltage sag/swell

1 INTRODUCTION

Due to consistently rising demand for electrical energy with developing technology and industrialization in today's world, the concerns about ensuring the reliability and continuity of the interconnected grid become more complicated and compelling for power system operators. New power production units called a distributed generation (DG), realized with renewable resources instead of fossil fuels, besides the advantages they provide, cause the emerging of some problems at many steps from production to consumption. The foremost challenge is the additional fault current originated from DGs at the short-circuit faults [1-4]. High fault currents, which are a result of the tendency to implementing DGs, may provoke the damage to circuit breakers and other system components or shorten their life [5]. The fault current can get to 10 times the nominal current and can breed to overheat in the main equipment of power systems such as power transformers and generators [6]. This will bring about extra costs of disservice apparatus incurred from faults to be added to the already high investment costs. As a solution to diminish fault currents, limiter devices are proposed and attempts are made to achieve them feasible and economical with the new types proffered.

The fault current limiters are planned to be practiced for different purposes in various parts of the power systems as in [7]. For instance, a bridge-type saturated core fault current limiter (BSFCL) has been merely experimented to suppress the fault current with an accurate limiting mechanism [8]. On the other side, applying a superconducting fault current limiter (SFCL) in the HVDC grid has been analyzed to minimize the interruption actions of the HVDC circuit breaker and also to reduce the fault identification time [9]. Implementing a resistive SFCL to an FPSO (floating, production, storage and offloading) power system has been simulated and the results are perused mutually with pyrotechnic fault current limiter (P-FCL) [10]. In [11], a new methodology has been improved to set optimally the directional fault current limiter (DFCL) parameters with the aim of protecting the microgrid.

Solid-state fault current limiters (SSFCL) have recently come to the forefront under the ascending rating of semiconductor switches and assuring with a wide range of functionality. When a fault occurred, SSFCLs keep the abnormal increment of the fault current at a reasonable level depending on the operating principle, the size of the elements used, the control method and its allocation, as well as improve power quality and obviating transient operation issues. Voltage sags and voltage swells are basically power quality problems [12, 13] and these can overwhelm the voltage profile at PCC; hence to protect sensitive loads connected to it, a beneficial approach is provided by maintaining the nominal voltage via FCLs. Instantaneous terminal voltages of power systems based on induction generator (IG) and doubly-fed induction generator (DFIG) wind turbines have been retained close to their nominal with utilizing SSFCL-LR (inductive and resistive) in balanced three-phase fault [14]. In [15], interline bridge-type fault current limiter (IBFCL) is proposed with a second task as hampering the PCC voltage drop in symmetrical and asymmetrical fault conditions. In the fault of one of the two lines connected in parallel, the PCC voltage fluctuation has been prevented and the healthy part with a sensitive load not affected in terms of power consumption and operating voltage with another developed SSFCL[16].

The load on faulty line disengages after a malfunction and to furnish the transient stability, excessive generated power must be consumed. FCLs have the capacity to undertake this task with their high impedance in temporary faults. The topology of diode-bridge-type non-superconducting fault current limiter (NSFCL) has been suggested to improve stability more than other associated circuits via consuming more power [17]. Fault ride-through (FRT) capability improvement performance of fuzzy logic controlled parallel resonance FCL (FLC-PRFCL) is proved with a comparison of PI controlled PRFCL, BFCL, and crowbar through the parameters such as terminal voltage, DC link voltage, machine speed, and active power profile [18]. A non-linear controller-based bridge-type FCL (NC-FCL) has contributed to augment the transient stability dramatically according to the series dynamic braking resistor by consuming further active power [19]. In other researches, various SSFCLs have been

handled to assess transient stability by way of comparing with FRT schemes [20] or operational techniques [21].

This paper presents an investigation about the comparison from several aspects of proposed SPRFCL and five other FCLs having working principles based on limiting the fault current with their parallel resonance impedance. Firstly, the applicability of SSFCLs has been evaluated for restricting the abruptly peaking fault current in different fault types. Then, their ability to maintain the nominal voltage profile at PCC during the fault is indicated for symmetrical and asymmetrical faults. The instantaneous peak power losses on FCLs that may raise warming problems have been obtained from PSCAD simulations. By surveying the contribution of limiters to the enhancement of transient stability using the accumulated energy consumption at the duration of the fault, it has been decided that it gives more accurate results from uncertain instantaneous variations and this parameter has been scrutinized as a new perspective. Finally, a summary of all analyses and the structural advantages and disadvantages of the circuits are presented.

SPRFCL and other inspected parallel resonance type FCLs are introduced in the next section. In Section 3, the power system where the limiters are utilized is shown. The linear control strategy we use in all circuits is described in Section 4. The results for the parameter such as limiting the fault current, maintaining the voltage stability, power losses on FCLs and total energy consumed in fault duration are given in Section 5, respectively. In Section 6, the applicability of resonance type limiter structures is objectively discussed and precious qualifications of SPRFCL are revealed. And the last section concludes this paper with the assessment of the results.

2 PARALLEL RESONANCE TYPE FAULT CURRENT LIMITER STRUCTURES

The phenomena of series and parallel resonance are considerably favoured in solid-state fault current limiters through their specific features with regard to the effects on normal and fault operating conditions in power systems. Series resonance is utilized to hold the current limiting circuit in an ineffective mode on system parameters such as voltage drop, power loss, and stability in non-fault conditions, and it can be basically provided with inductance and capacitor having equal reactance to each other. Thus, the principle of series resonance does not have current limiting function alone and it can be further implemented not only with resonance type fault current limiters but also inside different types of SSFCLs. On the other hand, the high impedance of the parallel resonance is activated to limit the fault current by increasing the falling system impedance after a short-circuit fault happened. Therefore, in the fault current limiters in which these structures are included, it is taken advantage of the zero impedance of the series resonance and the high impedance of the parallel resonance.

There are many studies involving the superior properties of parallel resonance in the literature. Our proposed topology called a series-parallel resonance-type fault current limiter (SPRFCL/Topology a) is compared with five different types of SSFCLs which are referred to with letters from b to f in this study. All circuits shown in Fig. 1 can act as an FCL in the system thanks to parallel resonance with the occurrence of a short-circuit fault.

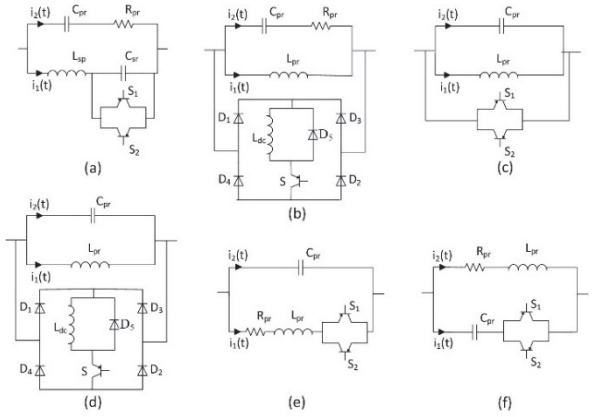

Figure 1 Investigated parallel resonance type fault current limiters: a) SPRFCL (Topology a), [22]; b) Parallel-LC-resonance-type fault current limiter (Topology b), [23]; c) Controlled resonance current limiter (Topology c) [24]; d) Controlled parallel resonance fault current limiter (Topology d), [18]; e) IGBT-controlled resonance current limiter (Topology e), [24]; f) Resonance-type fault current limiter (Topology f), [25]

These topologies have been fundamentally derived according to the point where semiconductor switches are used in the circuit and the components which are allowed to remain in line current path in normal operating conditions. All of them have two operating modes such as normal operation and fault condition. The semiconductor switches are controlled by signals from the control circuit, the fault current is limited by reaching high impedance in this way.

2.1 SPRFCL Configuration

The proposed fault current limiter which is shown in Fig. 1a consists of a capacitor (C_{sr}) connected in series to an inductor (L_{sp}) and a capacitor (C_{pr}) along with a resistor (R_{pr}) shunted to them [22]. The size of L_{sp} and C_{sr} is chosen to provide the series resonance accordingly, and capacitor values are also taken as equal because both resonance states occur with the common element of L_{sp}. Furthermore, the value of R_{pr} has an effect on the voltage stability during the fault and limiting of the fault current at the beginning of the fault, and so its value is determined with respect to these parameters. Also, the R_{pr} resistance yields to consume excessive energy that is generated but cannot be transferred to consumers and in this manner, transient stability of the power system would be retained. Although each circuit component is shown as a single one, more elements will need to be connected in series or be parallel depending on the current and voltage level to which they will be exposed.

Under normal operating conditions, because they constitute a negligible impedance relative to the parallel path, the line current passes completely through L_{sp} and C_{sr} that is in series resonance. The property of being invisible from the point of the system parameters normally expected from an ideal fault current limiter is precisely achieved with this feature. In case of any short-circuit fault, the semiconductor switches connected in parallel to the C_{sr} are turned on and the parallel resonance impedance of the circuit that can be calculated with the values of L_{sp}, C_{pr} and R_{pr} limits the magnitude of fault current. The purpose of implementing two inverse parallel-connected IGBTs is to be able to short-circuit of C_{sr} in the AC grid.

2.2 Other Parallel Resonance Type Fault Current Limiters

Several parallel resonance type fault current limiters proposed previously will be handled to compare with our topology and are explained in detail below.

2.2.1 Parallel-LC-Resonance-Type Fault Current Limiter

Another resonance type fault current limiter that is denominated as the parallel-LC-resonance-type fault current limiter is shown in Fig. 1b [23]. This topology was developed by combining two-branch which consists of parallel resonance and diode rectifier bridge. As long as no malfunction occurs, the semiconductor switch remains turned on and line current passes through L_{dc}, S, and diodes, thus the parallel resonance part of the circuit is bypassed. However, the high impedance value of parallel resonance is used to direct the line current towards the diode rectifier bridge and so only a negligible current flows through the parallel resonance part. After a short-circuit fault is detected in any area of the power system where the limiter is effective, S is turned off, hereby the path of line current starts to be through the parallel branch. The first peak of the fault current is restricted with high impedance and the line current is also prevented from rising until the end of the fault. Upon the system returning to normal, the IGBT switch is turned on, and the line current is provided to flow through the rectifier bridge again.

2.2.2 Controlled Resonance Current Limiter

The next fault current limiter is called controlled resonance current limiter and is shown in Fig. 1c [24]. The parallel resonance impedance of this topology is permanently eliminated by two inverse parallel-connected IGBTs paralleled to high impedance, as with series dynamic braking resistor, till the fault happens. The positive half cycle of the line current is carried on S_1, besides the negative half cycle sustains with S_2. With the occurrence of a fault at the downstream side of the limiter, both semiconductor switches are turned off in such a way that it ensures a path for suppression of high fault current. And so the fault current that will increase to a critical level for the system is limited by parallel resonance impedance. As soon as the fault ends, IGBTs get involved to carry all line current and generated power is delivered to consumers.

2.2.3 Controlled Parallel Resonance Fault Current Limiter

The parallel resonance fault current limiter (PRFCL) shown in Fig. 1d [18] evokes the topology which is illustrated in Fig. 1b, but it fundamentally differs from it in terms of elements constituting high impedance. The parallel resonance part of PRFCL is comprised of only one inductance and capacitor, but the other resonance type limiter has an additional resistor that provides a stability effect on bus voltage and consumes real power in fault conditions. The operating principle of both limiters is similar and line current passes on the rectifier bridge and the semiconductor switch in normal operation, otherwise, it connects the load bus through its parallel resonance branch in a fault situation. Therefore, while IGBTs are normally kept in conduction, they are brought into the cutting mode after a fault.

2.2.4 IGBT-Controlled Resonance Current Limiter and Resonance-Type Fault Current Limiter

Unlike other topologies, these FCLs are not completely ineffective on the system in non-fault conditions. A circuit element which is a capacitor in [24] and an inductance in [25], stays abidingly in the path of flowing line current, and this leads to power losses, and undesirable voltage swells at PCC, respectively. Also, after the fault, the system is unstable and former operational conditions cannot return. To overcome this hurdle, a resistor has been incorporated into the same branch with the inductance and its value is taken as equal with the other limiters to obtain the identical magnitude of impedance at the fault duration.

3 POWER SYSTEM MODEL

SPRFCL and parallel resonance type FCLs have been applied in a power system shown in Fig. 2.

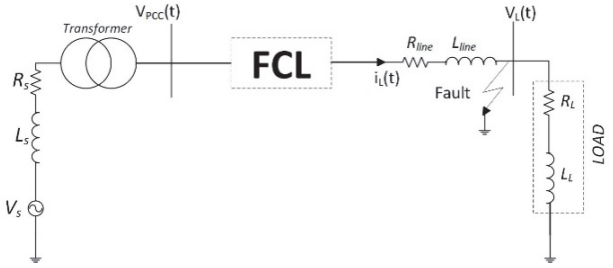

Figure 2 Power system model implemented of FCLs

Two or three-bus networks consisting of source, line, and load have been handled for performance analysis of FCLs in the literature [28-31]. It is illustrated as a single-line diagram but the performance analyses of limiters have been performed for three-phase system.

Table 1 Properties of the power system [26]

Parameter	Value
Network voltage (L-L)	20 kV
Source resistance	1 Ω
Source inductance	0.01 H
Line resistance	2 Ω
Line inductance	0.01 H
Load resistance	48.4 Ω
Load inductance	0.1 H
Network frequency	50 Hz
Fault resistance	0.1 Ω

FCLs have been implemented to the downstream side of PCC for each phase. The properties of the power system are given in Tab. 1.

4 CONTROL STRATEGY

Switching signals obtained from the control circuit given in Fig. 3 have been used to evaluate the transient fault performance of each topology mentioned above. The reason for the control to be achieved from the same circuit is to make a qualified comparison between relevant limiters. However, only an adaptation has been carried out

with the reversing of the control signal because the operation mode of switches in our recommended limiter is different from some others. IGBT switches of SPRFCL are continuously in cutting mode until the power system deteriorates with a fault, but some structures are in conducting mode.

In the power system model, the fault current limiters have been implemented to the downstream side of the point of common coupling. It is assumed that short-circuit faults will occur at the load bus. Therefore, load impedance will not affect the system impedance and so the line current will rapidly increase to a critical magnitude. Thus, the necessity of activating the high impedance of the fault current limiter by detecting the short-circuit immediately is quite obvious.

The first function of the control circuit is to identify the fault and put the limiter into the fault mode. The first peak of fault current is restricted in a short time and so the switchgear is prevented from being damaged by overcurrent. Initially, the identification of fault is started by comparing the impedance values of the transmission section and load side obtained by using PCC voltage (V_{PCC}) and load bus voltage (V_{L}) together with line current (i_{LA}) and load current (i_{L}). The main purpose of this comparison is to constitute a reference value of zero. Because, after the load impedance is out of the system, a voltage drop on the upstream side of the load bus will be seen. Then, this obtained value is compared with the difference between the carried current on the transmission line and load current. At the beginning of the fault, the line current will abruptly increase and the load current will decrease, so the reference value will be exceeded and semiconductor switches of SPRFCL will be turned on.

In addition to limiting the fault current with the proposed control technique, it is expected that the PCC voltage can be sustained at the nominal level during the fault. SPRFCL is also designed to improve voltage stability in accordance with the control circuit throughout the fault. This feature is fairly important in the buses where sensitive loads are connected, in order to prevent the problems of voltage sag and swell until the system normalizes. As will be explained in the next section, these power quality problems are solved in all short circuit faults.

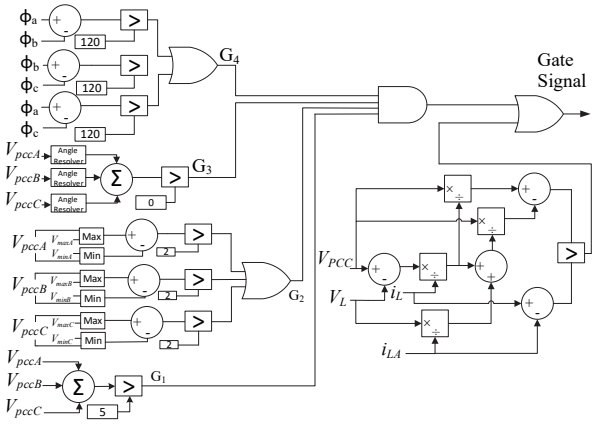

Figure 3 Control circuit

The voltage stability of PCC should be provided with rapid recovery in return back to normal operation. Nevertheless, when some fault current limiter circuits are applied to the power system, it may be difficult to bring the system to the voltage level of the normal condition in the recovery process, especially, in resonance types. This is a considerable drawback that may eliminate all the advantages of the limiter in terms of power quality. So, the virtue of our control strategy can be distinguished via its powerful transient effects on system parameters in the transition phase between two operation modes. It is obtained with using the signals of G_1, G_2, G_3 and G_4 and these are acquired by comparing the sum of the bus voltages of three phases, maximum and minimum levels of PCC voltages in each phase, the sum of the phase angles and angle difference between phases, with appropriate constants, respectively. And a successful recovery is completed and FCL becomes invisible on the system G_{S}.

5 SIMULATION RESULTS

In simulation studies, the proposed limiter circuit and other topologies introduced above have been implemented to the power system which is depicted in Fig. 2. FCLs have been placed on the downstream side of PCC and in each phase. It is presumed that all short circuit faults are at the load bus. The performance of the fault current limiters has been analyzed for three-phase, three phase-to-ground, phase-to-ground, and phase-to-phase faults. It is assumed that short-circuit faults will start at 0.5 s and persist until 0.63 s. The current limiting capabilities, which are primarily the first task of the limiters, are compared below, and then evaluations are made in terms of voltage stability and other parameters discussed. They can be compared with each other in every respect because they are applied under the parameters had tantamount properties such as placement, control method, and element sizes.

5.1 Limiting the Fault Current

In general, the limiters have two modes: normal operation and fault situation, and the transition between two phases is provided by switching actions in controllable structures like solid-state limiters. When the control circuit detects a malfunction in the system, the position of semiconductor switches changes to increase the normally low impedance of FCL and also this is by means of bypassing some circuit components or commuting the current path. The high impedance of the limiter suppresses the rising of the fault current in a short time and prevents it from catching a critical level.

All operating conditions have been taken as equal to facilitate fairly comparing the limiting capabilities of relevant topologies. According to this, the obtained results for three-phase and phase-to-ground faults are given in Fig. 4 and Fig. 5, respectively. If no fault current limiter is used, the significant magnitude of fault current reached is considerably noticeable with a value of 2040 A in symmetrical fault and its maximum gets to 600 A in a single-phase-to-ground fault which frequently happens in power systems. It is clear that keeping the fault current at a permissible threshold is only possible by developing a circuit had a suitable working principle to be activated quickly and also by determining the appropriately sized elements. In investigated parallel resonance circuits, it has been found acceptable to use the capacitor of 100 μF, the inductance of 101.3 mH and resistance of 21 Ohm in terms

of maintaining the voltage stability in fault duration and restricting the fault current to protect the switchgear safely.

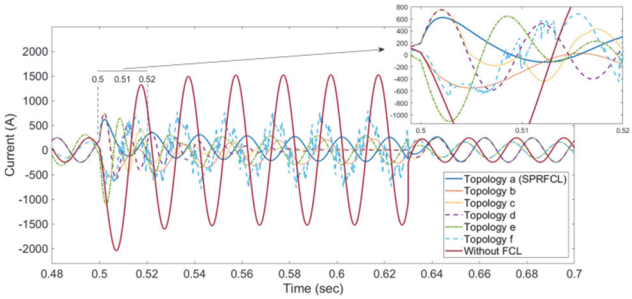

Figure 4 Line current in three-phase fault

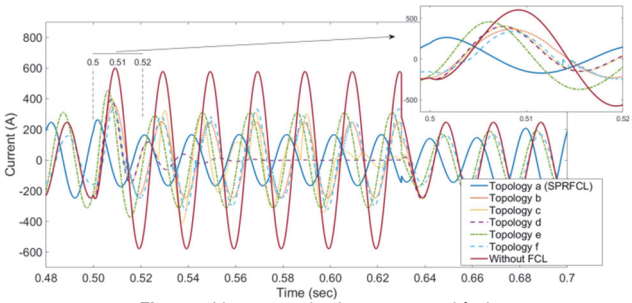

Figure 5 Line current in phase-to-ground fault

In a three-phase fault at the load bus, the circuits other than topology e limit the fault current to percentage rates ranging from 61-73%, but topology e remains at 46%. This drop at the maximum peak of the fault current indicates that the circuits successfully lower the high current at various rates with the signals provided from the control circuit we recommend. SPRFCL and topology b have shown the best current limiting performance for this type of fault. On the other hand, in phase-to-ground fault, SPRFCL has the highest limiting rate with 56% and has been able to retain the fault current almost at the nominal current level. In phase-to-ground fault, it also has once more the worst current limiting performance in topology e.

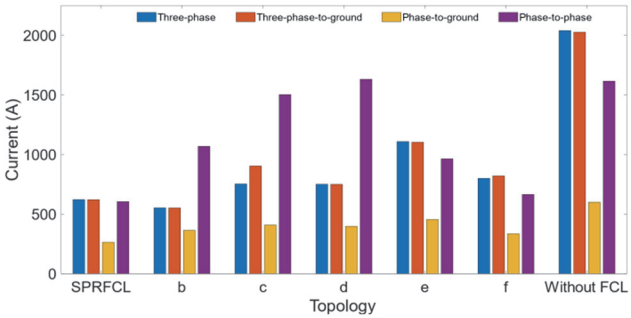

Figure 6 Maximum line currents in different fault types

The current limiting efficiency of the limiters may vary depending on the fault type and in some of them, there might be a considerable difference from others regarding the highest current. Although this is not a generalization, it is a result derived from the studies performed. The maximum line currents in different fault conditions are displayed in Fig. 6 and it is indeed corroborating this assertion because the fault current exceeds abundantly above the allowable safe limit in some topologies for phase-to-phase fault. However, the same circuits can reduce the abnormal current to a reasonable level in other faults. For instance, topology d can limit current up to 751 A in symmetrical fault, while it may restrain at 1632 A in an asymmetrical phase-to-phase fault. This disadvantage exists in the topologies of b, c, and d, besides, fault current limitation activity of topology e seems favourable but it is not enough and its serious drawbacks will be highlighted in the next sections.

Also, the current limitation capacity of topology e is inadequate in other faults except for phase-to-ground fault. Besides, SPRFCL limits resolutely the fault current in all fault types and so its restriction margin is very narrow. Even as the maximum current is 622 A among all faults when SPRFCL is applied, in other circuits it is 1069 A, 1503 A, 1632 A, 1109 A, and 821 A, respectively. Moreover, the maximum value of the line current without limiter in three-phase-to-ground and phase-to-phase faults is 2027 A and 1616 A.

5.2 Maintaining the Voltage Stability

Voltage sag and swell at the point of common coupling (PCC) are power quality problems that can restrict operational flexibility of power system and bring about additional costs, especially in busses where renewable systems and sensitive loads are connected. In order to solve this unfavourable circumstance, voltage quality is started to be standardized with some constraints for power networks that have begun to integrate with distributed generation. Thus, the Danish grid code allows remaining the PCC voltage profile above 20% of nominal value in wind power generation systems, furthermore Spanish and German grid codes necessitate that voltage sag is to be improved in case of faults falling to zero voltage within 0.15 s [31]. Fault current limiters can also enhance the stability of PCC voltage in conjunction with limiting the fault current and so SPRFCL with relevant resonance type limiters has been analyzed concerning maintaining this voltage at the nominal level during the fault.

While the maximum value of the PCC voltage is 15.1 kV under no-fault operating conditions, a sag of 62% arises from the three-phase fault in the FCL situation. The prevention performance of PCC voltage deteriorations of limiter circuits varies depending on the fault type just as their capacity of fault current limiting. Therefore, the profile of PCC voltage in different short-circuit faults has been examined for the cases of implementing the above-mentioned resonance type FCLs.

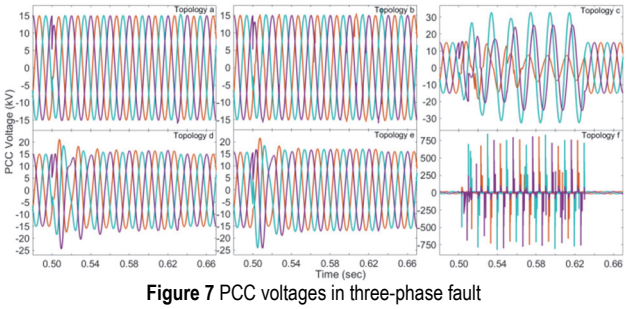

Figure 7 PCC voltages in three-phase fault

Fig. 7 shows the variation of PCC voltage along the transient fault from 0.5 s to 0.63 s. Topology a and topology b appear to be advantageous due to their contribution to the PCC voltage throughout the three-phase

fault, but a purely sinusoidal wave is acquired with proposed topology. Also, the ascending bus voltage at the end of the fault is 16 kV in the first circuit and 17.2 kV in the other. This value is given for other resonance structures in Tab. 2, and unlike these two circuits, it is attained at various times during the fault. Topology f presents the worst performance in a three-phase fault and is far from being applicable.

Table 2 Peak PCC voltage values during the three-phase fault

	Topology					
	a	b	c	d	e	f
PCC Voltage / kV	16	17.2	32.9	24.4	24.3	848

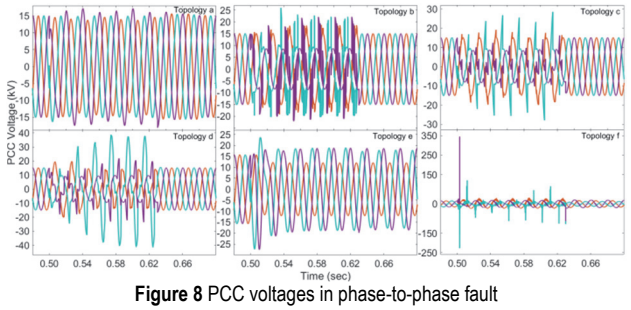

Figure 8 PCC voltages in phase-to-phase fault

Phase-to-phase fault is the most compelling fault to limit high fault currents and sustain the nominal level of the PCC voltage. In Fig. 8, the effects of different fault current limiters on PCC voltage alteration during phase-to-phase fault are illustrated. In this type of fault, SPRFCL can preclude voltage sags and swells at an admissible level and effectively conserve the PCC voltage. Fault current limiters other than SPRFCL cannot both hold the fault current adequately and cause excessive distortion in PCC voltage. Topology e exhibits second efficient operation after SPRFCL, but in this circuit the peak value of the voltage increases to 24 kV which is 6 kV higher. It also has many disadvantages.

5.3 Power Losses on Fault Current Limiters

Loss of power on FCLs at the period of fault is a significant design criterion to determine the amount of released heat and the temperature that the limiter components will reach. The power loss on an ideal fault current limiter should be negligible in normal operating conditions. However, increasing fault current and the high impedance of the limiter included in the system after the malfunction causes a great heat to emerge. Therefore, instantaneous power losses must not be too high to develop a long-life device in terms of fulfilling its missions as well as being economical. The released heat varies depending on the resistive components, the magnitude of the fault current, and the principle of operation and control of the circuit.

Table 3 Instantaneous peak power losses on fault current limiters

Topology	Power losses / MW			
	Three-phase	Three-phase-to-ground	Phase-to-ground	Phase-to-phase
a (SPRFCL)	1.67	1.66	0.99	2.86
b	1.68	1.67	1.59	4.19
c	2.07	3.12	1.91	3.89
d	1.82	1.80	1.22	7.49
e	2.46	2.44	2.55	2.91
f	3.53	3.22	1.12	3.01

The instantaneous peak power losses of resonance type fault current limiters on different fault types are given in Tab. 3. These values are peak power losses happening on the limiters, and losses shortly after the fault inception are lower. The power losses of the limiters differ considerably with respect to fault type, but the least power loss occurs on SPRFCL. It is concluded that our topology will be exposed to minimum thermal stress among all the examined topologies and so SPRFCL provides a great advantage to alleviate the warming problem that is very critical in switchgear devices.

5.4 Total Energy Consumed in Fault Duration

Even though the load is disabled in temporary faults, the system continues to operate and electrical power is generated. This power should be significantly consumed to contribute to the transient stability enhancement until returning to normal operation. FCLs are versatile devices that may provide an effective solution to absorb redundant power with its specific working principles. It is decided that investigation of the total energy consumed by limiter topologies throughout the fault is the correct method to evaluate the effects of them on transient stability. Otherwise, if the comparison is made through the total power losses, it will be rather complicated due to the high power oscillations per each phase.

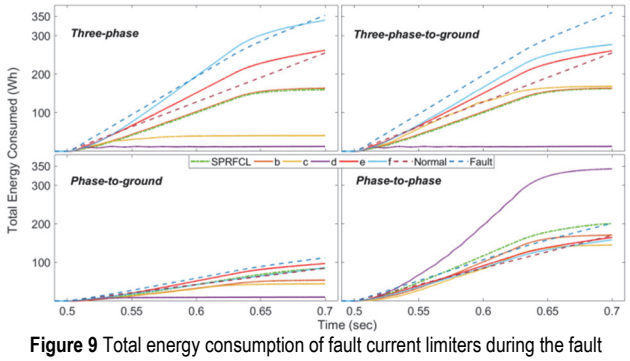

Figure 9 Total energy consumption of fault current limiters during the fault

Fig. 9 depicts the total energy consumption of fault current limiters during the fault, and electrical energy production without FCL for normal and fault situations. The energy expended by the circuits has been accumulated since the inception of the fault and total energy that involves a period of 0.13 s has been obtained. In different faults, the limiters consume varying amounts of energy as they have variable behaviours in terms of parameters such as limiting the fault current, power losses and maintaining the PCC voltage. At the same time, the resultant power of a fault in the situation of no FCL alters depending on the type of fault. The energy value for normal operation and fault situation has been determined according to the number of the faulty line with a linear approximation.

Implementing a limiter device also means preserving normal conditions; hence the total energy consumed should not exceed the acceptable level of energy generation and should not be at a very low level. Accordingly, while topology d has insufficient energy expending in three types of faults, it reaches an excessive value that is a lot higher from the energy generation in case of a phase-to-phase fault. Also, topology c remains at an inadequate amount of

consuming energy in only three-phase fault. Although topology e and topology f seem to be advantageous in respect to energy consumption, they consume more energy than under normal operating conditions in three-phase and three-phase-to-ground faults and this is an undesirable situation to ensure transient stability. SPRFCL and topology b show a proximate performance in two types of three-phase faults, but our circuit is superior with energy consumed closest to the normal level in the other two faults. Finally, SPRFCL has the most ideal energy consumption in all fault types and the loss of power on it also disperses throughout the fault, while in some topologies, instantaneous energy consumption is quite high.

6 EVALUATION OF THE APPLICABILITY OF RESONANCE TYPE LIMITERS

In this paper, the applicability of resonance type fault current limiter topologies in power systems has been investigated by considering many crucial parameters besides the fault current. These are maximum PCC voltage, the quality of PCC voltage, peak power loss on limiters, recovery time after the fault and energy consumed during the fault. It is demonstrated in the previous sections that the performance of the limiter circuits can exhibit enormous differences according to the type of fault and so the results are summarized for four types of faults in Tab. 4.

Table 4 Comparison of performance parameters in different fault types

	Topology	Peak Current / A	Max. PCC Voltage / kV	PCC Voltage Quality	Min. Peak Power Loss	Recovery Time / ms
Three-phase	a (SPRFCL)	619	16.04	✓	✓	10.6
	b	553	17.16	✓	-	143.61
	c	753	32.86	✓	-	10.45
	d	751	24.43	✓	-	906.95
	e	1109	24.26	✓	-	<<
	f	800	848.04	Dist.	-	<<
Three-phase-to ground	a	621	16.04	✓	✓	17.12
	b	552	17.13	✓	-	103.61
	c	904	31.45	Dist.	-	10.42
	d	750	24.37	✓	-	906.95
	e	1103	24.17	✓	-	<<
	f	821	836.71	Dist.	-	<<
Phase-to-ground	a	264	19.68	✓	✓	73.66
	b	364	19.68	✓	-	1380.28
	c	409	29.93	Dist.	-	10.41
	d	398	27.3	✓	-	<<
	e	455	22.82	✓	-	<<
	f	335	511.03	Dist.	-	<<
Phase-to-phase	a	622	18.16	✓	✓	57.31
	b	1069	26.01	Dist.	-	23.61
	c	1503	28.54	Dist.	-	13.7
	d	1632	41.52	Dist.	-	<<
	e	964	24	✓	-	<<
	f	665	379.81	Dist.	-	<<

Our primary aim for relevant resonance type FCLs is to limit the rapidly increasing fault current at the beginning of fault and simultaneously keep the PCC voltage at its nominal level. The logic control technique has been developed following this purpose and this enables us to make comparisons between limiter topologies. Nonetheless, all circuits pass to parallel resonance at the time of the fault, and the size of the circuit elements has been applied as the same magnitudes. The disadvantageous results for some parameters are related to the working principles and structures of topologies.

The frequency of occurrence of each fault type in power systems is different, but for an FCL to be applicable, it must be able to achieve sufficient performance in all types of fault. For instance, SPRFCL limits the fault current to 619 A in a three-phase fault, while this value is 622 A in phase-phase fault. As topology b restricts the peak current to 553 A and 1069 A for these faults, its limiting margin is rather wide and it is not allowable. The peak of the fault current reaches 1503 A and 1632 A with topology c and d in phase-to-phase fault and also topology c cannot avoid the distortions in PCC voltage in three faults. It should be emphasized that resonance type FCLs except SPRFCL have difficulties in phase-to-phase fault either in terms of the magnitude of the peak current and PCC voltage or its quality. Moreover, SPRCL both show the lowest peak power loss in all fault types and contribute to increasing the transient stability with the energy consumption it provides. Topology e and topology f are far from being feasible to apply because the recovery time is too long and topology d attends to them in two types of faults.

When evaluating the applicability of FCLs, it is necessary to consider design criteria as well as performance parameters. It has been decided that the two most important of these are the maximum voltage and current values to which the semiconductor switches used in the limiter circuits are exposed. Semiconductor switches significantly designate the cost of a fault current limiter. As the voltage and current levels with high values reached by switches, it causes to employ higher-rated semiconductors, and eventually, their costs increase. In some malfunctions, semiconductor switches are forced more than other faults, so the ratings must be determined according to the worst situation, since their lifetime may be decreased in a contrary action.

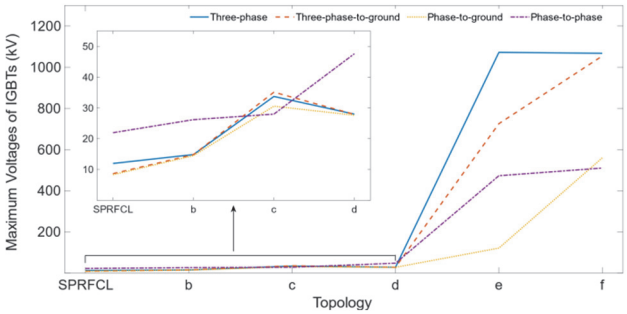

Figure 10 The highest voltage values IGBTs are exposed to

As seen in Fig. 10, IGBTs in SPRCL are exposed to the lowest voltage values compared to other topologies in all fault types. SPRFCL gets its highest value in phase-to-phase fault as 21.95 kV, and there is 4.2 kV difference between topology b which is the closest one. Limiters acquire their maximum values in different faults and also the alteration might be very high in the same topology, for example, the disadvantageous situations are in three-phase-to-ground fault for topology c and for topology d in phase-to-phase fault.

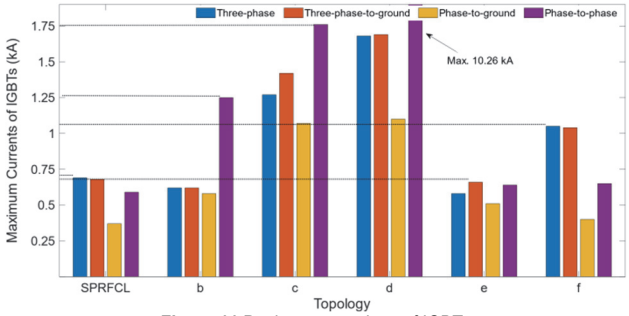

Figure 11 Peak current values of IGBTs

Fig. 11 displays the peak current values incurred by IGBTs during the fault. SPRFCL and the switches of topology e are exposed to the lowest current with a negligible difference. Especially in phase-to-phase fault, many circuits attain very high current levels, this value is 10.26 kA for topology d. SPRFCL can keep the ratings of the switches lower in current as well as in voltage. And the proposed limiter topology presents a convenient and economical structure in terms of design criteria and the performance parameters discussed.

7 CONCLUSION

The phenomenon of parallel resonance with its inherent characteristic of presenting high impedance has gradually got more and more involved in solid-state FCL circuits. Thanks to their simple structure, easy control, and flexibility, parallel resonance type FCLs are very close to being applicable in power systems in the foreseeable future. Therefore, the feasibility of proposed SPRFCL with respect to the other relevant resonance type limiters has been decided considering the foremost critical parameters of the power system besides the magnitude of fault current with the performed simulations. It is considered that the consumption of the excessive energy by FCL and maintaining the stability of the PCC voltage at the duration of fault establish opportunities to sustain the power quality in temporary fault situations. Instantaneous power loss on FCL and current and voltage values to which its switches are exposed are indicators to compose a reliable and economical fault current limiter. The results obtained in this context are as follows:

- SPRFCL can successfully limit the fault current to an allowable value with a narrow margin when its results for all fault types are compared.
- The stability of PCC voltage during the fault is susceptible to the rising of fault current. SPRFCL has a superior contribution to maintaining the PCC voltage closest to its nominal value at the duration of the fault for symmetrical and asymmetrical faults. Some limiters that can perform this goal in symmetrical fault have failed in asymmetrical fault.
- The proposed limiter has incurred the lowest instantaneous power loss in a fault situation and this may be a serious advantage for long-term usage.
- In addition to the above advantages, SPRFCL has balanced energy consumption during the fault and is also very stable in terms of total energy consumed.

Finally, semiconductor switches of SPRFCL being exposed to the lowest current and voltage levels proves its simple and economical structure.

Acknowledgements

This research was funded by The Scientific and Technological Research Council of Turkey (TÜBİTAK) with the project numbered 119E665.

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