

# Design of a Single-Core Digital-to-Analog Converter with Ultra-Wideband and Low Power Consumption for CUWB-IR Applications

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**Abstract:** Data converters are intermediate circuits used to connect between two analog and digital ranges. Data converters are not only used for converting audio into a microphone or speaker, but also for converting audio into a camera or display, transferring information to a computer or digital signal processor. At these times, the need for data converters is not invested in every aspect of life. Digital to analog converters is a leading part of these converters, which are widely used in most audio and video circuits. In this thesis, we have proposed a 4-bit 1GS/s DAC for CUWB-IR usage. To enhance the above performance with superior speed and the need for linearity, every significant block containing the convenient sources, current switches, and deglitcher were designed optimally and a new DAC converter circuit was developed which improves the linearity. The designed DAC was performed using a commercial 130 nm CMOS process. DAC INL/DNL $\leq$ 0.22LSB features more than high Nyquist bandwidth at extremely low power losses of 0.45 mW. The proposed DAC achieves the best FoMs at the right time for advanced DACs.

**Keywords:** Cognitive Ultra-Wide Band; CUWB-IR; differential non-linearity; digital-to-analog converter

## 1 INTRODUCTION

Analog-to-digital converters are one of the most important blocks in software radio and other signal processing systems [1]. With the advancement of technology, the design of analog circuits has become more complex due to the reduction of the inherent gain of the transistor and the voltage of the power supply [2, 3]. Therefore, it is extremely challenging to design a converter with high speed and accuracy [4]. Analog-to-digital tube converters have absorbed a great deal of attention among other analog-to-digital converters due to their relatively incredible speed, low power consumption, and medium to high accuracy, and are widely used in Nyquist sampling. Maybe [5]. In these converters, by reducing the channel length of the transistors in SIMAS technology, it becomes extremely challenging to design an amplifier with significant gain and speed. Recent methods have been proposed to solve the problems of analog-to-digital converters. In some of these methods, by reducing the voltage of the power supply, the converters are designed and as a result, the power consumption is reduced. Broadband (CUWB) comprises a combination of broadband (UWB) and radiography, which represent an emerging approach that allows the use of a highly efficient, low-interference spectrum (as opposed to non-cognitive types that require Has a spectrum band allocation) [6]. Typically, the CUWB system negotiates with nearby radio systems to find available spectrum bands, searches for the spectral range of the negotiations, and then repeats the process in real-time. Given the mentioned fact, it is mostly achievable that the CUWB transmit system could produce compatible UWB waves that are in reach by spectral bands.

The alternative method is a digital-to-analog converter (DAC) generator that can reduce these weaknesses by combining a UWB compatible waveform with the corresponding digital inputs. In the non-cognitive UWB radio waves (UWB-IR), the UWB wave formed is typically produced via a pulse producer using a delay regenerator, oscillator circular, and phase modification diode method. However, the mentioned methods are unsuitable for

Cognitive UWB-IR, mainly since the pulse producers are usually restricted to a single UWB form. When multiple pulse producers can be multiplied to form various pulse shapes, there are problems with excessive hardware shortages, complex pulse producers, or poor compatibility of the on-chip (SoC) CMOS system. [14]

An alternative method is a digital-to-analog converter (DAC) generator that can reduce these weaknesses by combining a UWB compatible waveform with the corresponding digital inputs [7]. It should be noted that the DAC-based pulse producer has three profits. At the first, using the previous signal of the digital signal processor, the UWB signal can be generated with adjustable pulse shapes. Secondly, this feature shows a reduction in the diameter of the pulse waveform ring [8], thus improving power efficiency and noise safety. Ultimately, the system is CMOS compatible with the chip (SoC). Because of these features, the high-speed Nyquist DAC is significantly better for CUWB-IR transmitter pulse generators. Despite these advantages, current DACs are unsuitable for the most advanced CUWB-IR systems for low power consumption. Some high-speed DACs [9, 10] employing exotic fabrication procedures (eg SiGe, BiCMOS, III-V, and HBT) by high-frequency transistors have been proposed. On the other hand, the reported ultra-fast CMOS DACs require soaring cost, excessive complexity, and hardware such as a phase-locking loop (PLL) frequency divider to achieve high conversion rates. In addition, losses lead to more power [11, 12]. For this purpose, in this paper, a high-speed single-core CMOS DAC with low hardware cost is required to build a low-power CUWB-IR system.

## 2 METHOD

### 2.1 1GS/S 4-bit Analog-to-Analog Digital Converter

Fig. 1 depicts the schematic of a digital converter designed for 4-bit analog 1GS/s. The input signal is followed by the deglitched providing digital signals. After that, the conditional digital signals are fed to the current switch at the

outer level. Essential blocks structures - current sources, current switches, and deglitches - are identified in turn.

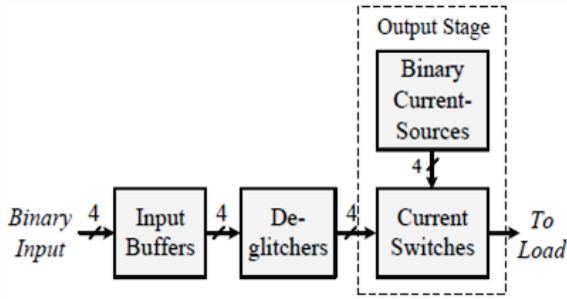


Figure 1 Block diagram of the digital converter to 4-bit analog 1GS/s

A transistor with complex output impedance is critical for low output distortion, and this is achieved by a small transistor for the low noise capacitor. Vice versa, small-sized transistors can degrade the transistor's fit across the array of current sources, leading to high nonlinearity and reduced efficiency [8]. Up and matching a good transistor is essential. Fig. 2 shows a diagram of a cascade current source with current switches. According to the below equations, firstly the impedance resistor is determined, which is sufficient to achieve the 4-bit requirement, and then determine the transistor matching. The optimum output impedance of a completely different DAC is deduced by the  $INL$  and  $SFDR$  specifications.

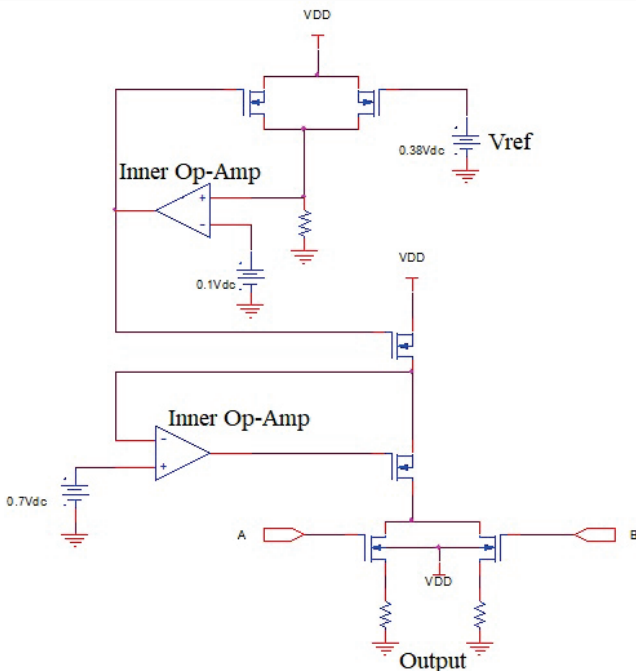


Figure 2 Outline of a source and DAC current switch

As shown in Fig. 3, the link between the apparent input resistance and the  $INL$  for the unit current control topology can be determined. The common binary flow topology is effectively parallel to the multiple units of flow sources. According to the end-of-line  $INL$  calculation [7], the  $INL_k$  for the input code  $k$  is obtained as follows:

$$INL_k = \frac{v_{out, k} - v_{out, 0}}{v_{out, LSB}} - k = \frac{k(M-k)(M-2k)}{2(k+s)(M-k+s)}. \quad (1)$$

The  $INL$  peak value is expressed as follows:

$$|INL| = \frac{(3s^2 + 3Ms - p)\sqrt{6s^2 + 6Ms + M^2 - 2p}}{2(s^2 + Ms - p)}, \quad (2)$$

in this case:

$$r_0 = R_L \left( -\frac{M}{2} + \frac{\sqrt{3}}{18} \sqrt{9M^2 + 8INL^2 + \frac{(3M^2 + 4INL^2)^{3/2}}{|INL|}} \right). \quad (3)$$

Then, assuming that intermodulation proves the third-largest stimulus, the link between apparent output resistance and  $SFDR$  (dB) is obtained in part from the analysis in [9], as follows:

$$r_0 = \frac{R_L M}{4} \left( -2 + \sqrt{3 \times 10^{|SFDR|/20} - 9} \right). \quad (4)$$

Based on the previous equations, the  $R_L$  must obtain 50 ohms and the required  $r_0$  more than one kW ohm to meet the condition  $< 0.25LSB INL$  and  $> 24dBc SFDR$ .

## 2.2 Current Switches

Fig. 2 illustrates the outline of the flow switches in which a simple differential pair topology is tuned to satisfy the conversion rate requirement of 10 GS/s. The current switch model here includes amplifying the dynamic linearization of the DAC reduction in the output errors caused by the capacitive power supply. The effect of capacitive power supply is deduced by minimizing intermittent capacitance between currents and using low voltage fluctuation (excitation) control signals in current switches.

## 2.3 Deglitches

The inverter [8] can reduce the discharge mechanism: by adjusting its output transfer point so that the current switches are never "off" at the same time. To more significantly modify the discharge mechanism, the deglitches (based on inverter M1-M6) are proposed by increasing the high-speed source (M7-M8) and are illustrated in Fig. 4. The amplified source reduces the glitch mechanism by specifying low voltage fluctuations (0.5 VDD) and short transmission times (10 T clock%). In addition, the interference between the two algorithms is reduced by two methods. First, resistive loads, instead of three-dimensional transistors, are used for rapid change, as well as interference and internal interference. Second, the apparent resistance of the output is designed to reduce intersymbol interference due to undesirable overload [10].

### 3 SIMULATION RESULT

The proposed DAC test is rigid, especially because of the digital algorithms,  $4 \times 10$  Gb/s input is required. For Gb/s speeds, the time interference method [11-13] is typically used to reduce I/O requirements. However, this method increases several other challenges, including much larger auxiliary circuits, complex auxiliary circuits (e.g. RF PLLs, frequency dividers), and so on.

Our proposed model maintains three advantages. Initially, it offers dual performance mode (READ) and a fast 25 Mb/s WRITE speed (1 Gb/s). It should be noted that the purpose of the test is incredible speed, and the second makes it attractive for simplicity and low-speed planning. In addition, the proposed tester is relatively easy to implement.

Fig. 3 illustrates a proposed tester designed to produce high-speed digital patterns at 1 Gbp/s. The required rate of one Gb/s is obtained using four devices built into testers with data pattern lengths of up to 4 bits. Fig. 3 shows the execution state data streams:

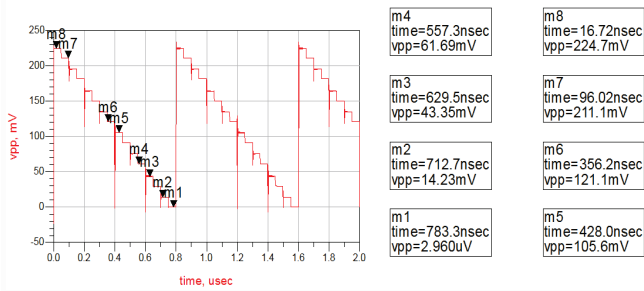


Figure 3 Shows the performance of the proposed circuit

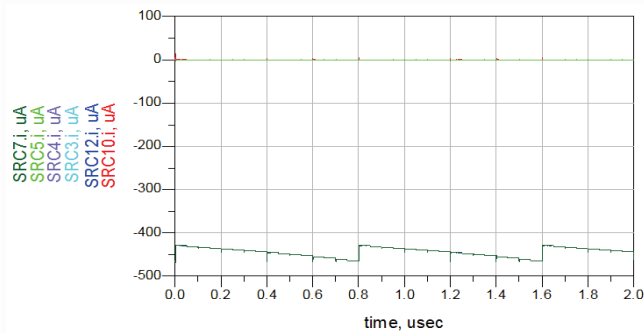


Figure 4 Displays the system consumption current over time

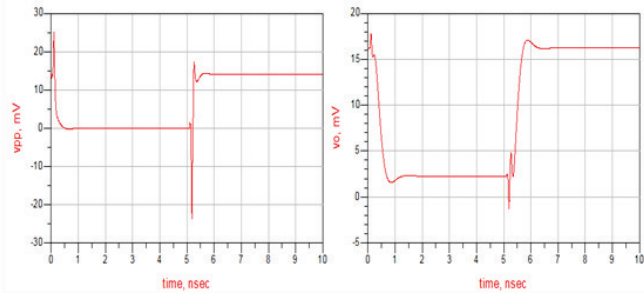


Figure 5 Displays single-bit input change

Generate data loops at speeds above one gigabyte per second. In this section, the output results of the designed

circuit are reported in Fig. 4. Based on the circuit diagram, it is designed for an output range of zero to 240 mV, which for a 4-bit resolution is equal to 15 mV for each phase change (LSB). There is very good linearity in the system. Figs. 4-6 also shows the transient response speed of the converter to change one bit in the input. Finally, Fig. 6 shows the performance of auxiliary operational amplifiers.

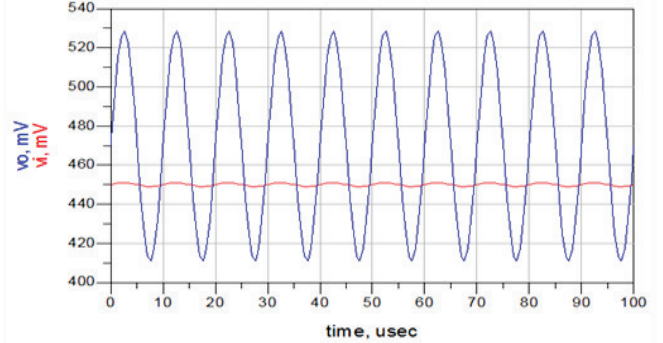


Figure 6 Shows the performance of an auxiliary operational amplifier as a buffer and amplifier

To evaluate the proposed DAC against advanced CMOS-based and non-CMOS-based DACs, we have implemented various schemes in Tab. 1. In this benchmark, the CMOS DAC in [13] has a higher conversion ratio than the proposed one in this research. Chiefly since it uses a 16:1 period. However, it is slower based on a single-core DAC. Multiple approaches to the CUWB-IR application are not considered scheduled to the complex hardware overload for synchronization.

Table 1 Evaluation of the proposed DAC against high-speed super-fast DACs

	This work	[7]	[8]	[9]	[6]
System	CMOS	CMOS	CMOS	Bi-CMOS	InP HBT
Size (mm)	130	28	65	250	500
Resolution (bit)	4	6	6	4	6
$V_{DD}$ (V)	1	2.5/1.4	2.5/1.1	3.5	-4
$f_{conv-1-core}$ (GS/s)	2.1	7	3.5	30	60
$V_{out-swing}$ ( $V_{pp-diff}$ )	0.24	0.5	0.6	0.05	1
$P_d$ (mW)	0.45	145	46.87	455	1800
$INL$ (LSB)	0.16	-	-	0.49	0.31
$DNL$ (LSB)	0.22	-	-	0.57	0.43
$FoM_1$ (pJ)	0.028	0.32	0.21	0.95	0.47
$FoM_2$ (pJ <sup>-1</sup> )	--	1.11	2.30	-	-

### 4 CONCLUSION

Analog-to-digital tube converters are widely used in telecommunication receivers due to their relatively high speed and medium to absolute accuracy. For this reason, currently, many efforts have been produced to reduce its power consumption in various ways. In this paper, we propose a 4-bit 1GS/s DAC for CUWB-IR applications. To achieve the above high-speed performance and the need for linearity, every critical block containing existing sources, current switches, and deglitcher were optimally designed, and a new deglitcher circuit was developed that improves linearity. In addition, a new tester has been developed that provides low-speed programming and high-speed digital pattern generation. The DAC is designed using a commercial

130 nm CMOS processor. DAC INL/DNL $\leq$ 0.22LSB features more than high Nyquist bandwidth at extremely low power losses of 0.45 mW. The proposed DAC obtains the best FoMs at the right time for advanced DACs.

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