

# Design and Implementation of a Fully Flexible Cognitive Radio Modem

Greta A. Vardanyan, Martin Ts. Ayvazyan, and Orbel Zh. Sevoyan

Original scientific article

**Abstract**—Software-defined radio (SDR)-based cognitive communication radio systems are very popular at present, and there have been many investigations on this topic. This paper proposes a new type of cognitive radio transceiver (TRX) that can detect, recognize, and analyze input signals in real-time with minimal data loss. New hardware is designed and manufactured that combines a transmitter and a receiver in a dedicated integrated circuit. For data processing, a field-programmable gate array (FPGA) is used. For each integrated hardware block, appropriate software modules are developed to construct a complex adaptive radiocommunication system as a radio modem that can be configured as a transceiver or repeater. The source coder, channel coder, modulator, spectrum monitoring module, spectrum analyzer, channelizer, symbol rate detector, modulator, modulation type recognition module, demodulator, channel decoder and source decoder are all developed as software modules.

**Index Terms**—blind demodulation, cognitive radio systems, channel coding, symbol rate detection, source coding, software-defined radio.

## I. INTRODUCTION

At present, radio communication is developing so rapidly that every day, an increasing number of services are being offered using various technologies and radio interfaces [1]. In this era of such complex communication, the cognitive ability of a terminal is key for optimizing the use of resources [2], [3]. A cognitive radio system is a radio transmitter (Tx) and/or a receiver (Rx) using a technology that assumes that radio performance parameters, including but not limited to the frequency range, modulation type, and output power, can be set or changed by specially designed systems and algorithms.

The increasing level of demand and the shortage of radio frequency resources are driving a need to develop various approaches and technological solutions aimed at increasing the efficiency of spectrum usage [4]. Hence, research on cognitive radio technologies, which are based on the use of temporarily unused portions of the spectrum, is gaining in importance. While the effective usage of spectrum is the main advantage of

cognitive radio communication systems, other automated processes are also required to achieve a fully intelligent receiver, such as modulation type recognition, symbol rate detection, and coding–decoding processes [5], [6]. Many systems have been developed that can be used as cognitive or adaptive radio transceivers (TRXs), but they usually are large in size (because modulation type recognition algorithms require significant resources), have not been developed beyond the prototyping stage [7], or are limited in the types of modulation that can be used. For example, modems used in unmanned aerial vehicle (UAV) monitoring drones are usually limited to one or two modulation schemes and do not monitor the spectrum for other activity [8].

There are key technical problems for similar modems, which are intended to be used in UAV's, size and capability to work in the presence of interfering signals. The modems proposed in [7], [8] do not deal with these problems. As a spectrum is getting more utilized, and more anti UAV or Electronic warfare systems are being deployed, it is crucial to support cognitive functionality.

The system proposed in this paper has a small form factor that allows it to be installed on small UAVs. It is flexible and fully automated and has the following features: source coding, channel coding, modulation, spectrum monitoring (continuous monitoring with channel sensing and activity classification in the working band), spectrum analysis, channelization, symbol rate detection, signal modulation, modulation type recognition, demodulation, channel decoding and source decoding.

The novelty of the proposed system is that we have been able to fit all of the abovementioned functions into one field-programmable gate array (FPGA) while achieving low power consumption and a small form factor. These features are crucial for small UAVs and will determine their ability to operate in noisy environments when jamming and sniffing sources are present [9].

The paper is organized as follows. This introduction is followed by section II, which is devoted to the description of the novel cognitive TRX architecture, including the Tx and Rx structures. Next, section III describes the interfaces of the communication protocols used to interact with external devices as well as the synchronization architecture that is implemented for proper network operation when multiple TRXs are used. Section IV describes the entire system structure, including the hardware components. Section V addresses data encryption for protection from unauthorized access to the communication systems. Section VI is devoted to the results of tests and measurements and is followed by the conclusion.

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Authors are with the Department of Radioengineering and Communication Systems, The State Engineering University of Armenia, Yerevan, Armenia (greta.vardanyan@gmail.com, aivazyan@mail.ru, orbel.sevoyan@gmail.com).

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## II. NOVEL COGNITIVE TRANSCEIVER ARCHITECTURE

### A. Transmitter Structure

The novelty of the proposed Tx is its adaptability to changes in modulation type, source coding and hopping schemes on the fly based on the system and network parameters. Additionally, all of the abovementioned features are implemented within a small form factor using an FPGA, which makes the proposed device very attractive for UAV applications. The Tx contains two separate channels, which are connected to two antennas that are physically separated from each other, and both channels share the same local oscillator (LO) frequency. This approach of using two Tx paths allows the implementation of a spatial diversity receiver scheme, as in most cases, we will have a signal with a good signal-to-noise ratio (SNR) from at least one antenna. Actual transmission is performed through one of the Tx channels, and the channel decision is made based on the received signal strength indicator (RSSI) level measured at the corresponding antenna. The Tx channels are identical, and they share the same software. This implementation allows better performance to be provided when the radio is installed on a fast-moving object [10]. As a TRX, an AD9361 board (manufactured by Analog Devices) is selected, which has a wide frequency range, a good noise figure and a wide dynamic range [11]. The transmit channel path of the AD9361 consists of multistage filtering modules to reduce out-of-band emission. In addition, this frees up some space on the FPGA because there is no need to perform resampling and filtering before passing the data to a digital-to-analog converter (DAC). A block diagram of the filtering path is presented in Fig. 1.

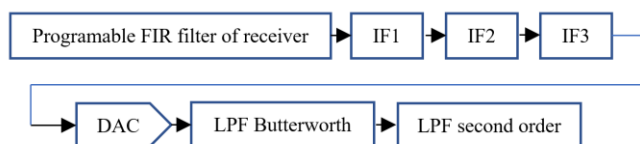


Fig. 1. Filtering path in the transmit channel.

The 12-bit quadrature digital samples from the FPGA core are passed through a programmable interpolation finite impulse response (FIR) filter, and a combination of three filters with fixed interpolation coefficients are fed to the input of the 12-bit DACs [12]. The analog quadrature signals from the DAC output are then subjected to low-pass filtering to suppress spurious spectral components arising from the time-discrete nature of the original data. The low-pass analog filtering stage includes a third-order Butterworth low-pass filter with a cutoff frequency that is programmable between 625 kHz and 32 MHz and a single-pole low-pass filter, the cutoff frequency of which can be varied from 2.7 to 100 MHz. The filtered analog signals are subsequently fed into mixers for frequency conversion and further amplification [13].

### B. Receiver Structure

The novelty of the proposed receiver is its ability to detect the modulation type and symbol rate of the incoming signal without prior information. This approach minimizes synchronization and handshake requirements. Additionally, the Rx is capable of performing continuous spectrum measurements over the entire operating range. All this is

implemented within a small form factor using a Xilinx FPGA, which allows the device to be used on small UAVs, where size, weight and power consumption are strongly constrained.

Like the Tx, the Rx also consists of two different paths, which share the same LO frequency and can be programmed to different gain levels and bandwidths. Both Rx paths work in real time over a full 56 MHz bandwidth. The FPGA performs spectrum monitoring, detects the RSSI for each input and decides which Rx channel should be used [14] [15][16]. The receive path architecture of the AD9361 is shown in Fig. 2.

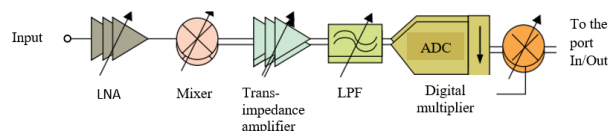


Fig. 2. Block diagram of the AD9361 receive path.

The receive path includes low-noise amplifiers (LNAs), a mixer, matched amplifiers for quadrature signals, analog filters to eliminate spurious mixer components and prevent spectral aliasing, two 12-bit analog-to-digital converters (ADCs) with an adjustable sampling rate, and a set of digital filters.

Because the Rx sampling rate does not change during operation, we have implemented a software module that resamples and channelizes the 56 MHz bandwidth (BW) and brings it down to a required bandwidth and number of channels [17]. The information from the channelized bands, such as the RSSI BW, SNR and center frequency, are used to create a table with all activity information; this table is continuously updated for both receive channels. For example, based on the information in this table, the Tx antenna and modulation type are selected, and the Tx power and center frequency are calculated.

## III. INTERFACE COMMUNICATION PROTOCOLS

The proposed radio system can work with external devices using various types of interfaces, such as local area network (LAN), Serial Peripheral Interface (SPI), RS-232, RS-485 and custom digital input/output (DIO) interface.

Data exchange via a LAN interface occurs at a speed of 10 or 100 Mbit/s; automatic negotiation is supported, so there is no need to select the speed. A full-duplex connection is established, meaning that it is possible to transmit and receive data simultaneously. The data exchange is carried out via the User Datagram Protocol (UDP).

Data exchange via the SPI interface occurs at a speed of 10 Mbit/s, and the TRX acts as the slave device.

### A. Synchronization Structure

For proper network operation when multiple TRXs are used, we have implemented a special synchronization method that does not depend on external synchronization sources such as the Global Positioning System (GPS), Global'naya Navigatsionnaya Sputnikovaya Sistema (GLONASS), or the Galileo navigation satellite system.

As a clock source, a simple, low-cost temperature-compensated crystal oscillator (TCXO) operating at 40 MHz is used (Table I). We have implemented a special algorithm to achieve synchronization at 1 ppb between the TRXs.

Each TRX, after being powered on, starts to monitor the network for any activity in the given frequency band, looking for associated members of the network. If no activity is detected within 3 seconds, the modem starts broadcasting special synchronization frames with hopping between different RF center frequencies at a rate of 1000 hops/s. When each TRX detects a synchronization frame, it checks whether it is from a member of a group that is already working or is just a TRX that is looking for a group. In the first case, the TRX checks whether the group information matches the group assigned to it; if so, using special encryption, it sends a key request, and the network member that receives this request checks whether it is a valid request and a new member is added to the group, and the same is true for all other members joining the group. In the second case, the TRX is looking for a group; again, a special request is shared between the TRXs coded with an encryption key, and a new group is created. Multiple groups can also be joined to create a larger group. Once a member has been added to a group, synchronization between the TRXs is achieved and is continuously corrected during operation.

TABLE I  
PARAMETERS OF THE REFERENCE GENERATOR

Parameter name	Parameter value
Frequency	40.00000 MHz
Output signal type	CMOS
Short-term frequency stability	Not worse than 0.25 ppb
Long-term frequency stability	0.375 ppm

IV. SYSTEM DESCRIPTION

The control block (CB) is responsible for generating commands to govern the modes of operation of the other modules. It is also responsible for the generation of the synchronization signals used for synchronizing modem-to-modem communication. The CB creates a data frame and a specially modulated signal for synchronization. These data are transmitted once every 10–1000 ms; the receiver extracts the data frame and modulated signal, the extracted information is compared against the locally generated information, and any difference is compensated for by the LO. After all communication is completed, the corrected values are used. This process is continuously executed to ensure that the two TRXs are synchronized with each other. The TRX structure is presented in Fig. 3.

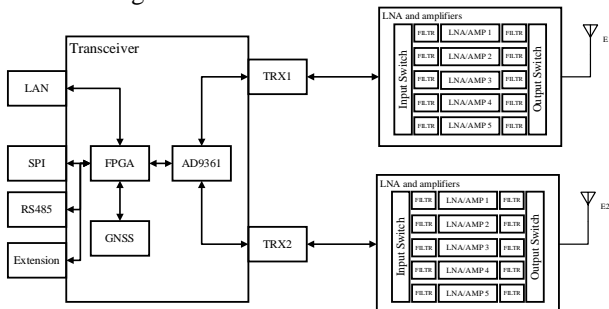


Fig. 3. The TRX structure.

The CB programs and controls the AD9361 TRX in real time. To achieve the minimum delay and support a frequency change

rate of 1000 hops/s, we have created a new driver that operates on the FPGA without utilizing any Linux or Windows platform.

Based on information from the RSSI table, the CB makes a decision regarding which modulation scheme, frequency and hopping speed to use.

As a one-time synchronization source, we use a global navigation satellite system (GNSS) module, which can be used either at the user’s request, only once, or at predefined intervals. The number of pulses per second (PPS) is used to measure the absolute value of the onboard clock. The measured clock value is then stored in electrically erasable programmable read-only memory (EEPROM) by the CB.

For transmission, the CB applies the following procedure. Once sufficient data have been received from external devices to form the transmit frame, the CB on the FPGA starts the source coding process, concatenating different data received from SPI, LAN, RS-232 and other interfaces. Next, technical data are added: the RSSI table, synchronization data, the TRX ID, the final destination of the data and other technical information. All sensitive and user data are encrypted using the AES-256 standard. After all this, channel coding is performed on the data using the Viterbi + Interleaving + Reed–Solomon scheme, as it is simpler than other schemes such as low-density parity-check (LDPC) codes or TPC/TC and thus easier to implement on an FPGA. The coding gain achieved in this modem varies from 4 to 6 dB and depends on the noise type, interleaving depth and modulation scheme.

Further modulation is then performed. The type of modulation, symbol rate and Tx power are selected based on RSSI information from the Rx and Tx sides. Finally, the signal is amplified and fed to the antenna [18].

For reception, the CB performs steps exactly opposite to those for transmission. The general scheme of a TRX is presented in Fig. 4.

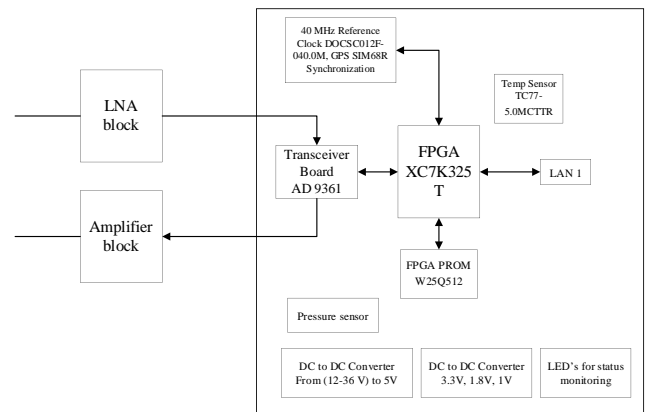


Fig. 4. The general scheme of a TRX.

A. Hardware Components

The TRX module is built using two different printed circuit boards (PCBs): a digital signal processing (DSP) board and a TRX board. The core of the DSP board is an XC7K325T-2FBG6761 FPGA from Xilinx. The technical parameters of this FPGA are shown in Table II [19].

TABLE II  
FPGA TECHNICAL PARAMETERS

Parameter name	Parameter value
Family	Kintex-7
Cells	326080
Registers	25475
Case type	676-BBGA

The analog path is controlled by a CB through a serial interface with a clock frequency of up to 30 MHz.

On the first board are the FPGA, a connector to connect to the TRX board, DC/DC converters, temperature sensors, and a LAN 10/100 physical layer integrated circuit (PHY IC) (the medium access control (MAC) layer is implemented in the FPGA).

The TRX has a gas discharge tube (to protect it from electromagnetic spikes) and low dropout (LDO) to minimize the effect of the DC/DC converter on the TRX noise level.

As the TRX board, an AD9361 board from Analog Devices is selected. The diagram in Fig. 2 shows that the AD9361 has two receive and two transmit channels, a clock module, a digital I/O signal, control interfaces, and auxiliary ADCs and DACs. The presence of two pairs of receive and transmit channels simplifies the construction of multiantenna systems such as a multiple-input, multiple-output (MIMO) system or a spatial diversity receiver for fast-moving objects, where one antenna can be blocked by the body of the object on which the TRX is installed (for example, a UAV, helicopter, or airplane).

For the TRX, a 6-layer PCB buildup is used. For the DSP PCB, a 10-layer buildup is selected due to the high integration of the components and the small size of the board. An overview of the locations of the parts of the board is presented in

Fig. 5.

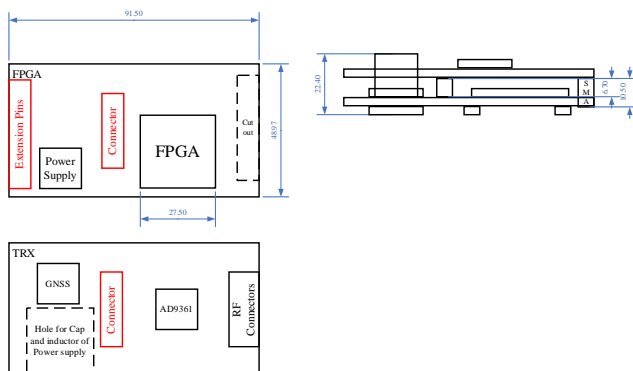


Fig. 5. Overview of the locations of the board parts.

Side and top views of the final developed and manufactured TRX are presented in Fig. 6.



Fig. 6. Side and top views of the TRX.

## V. DATA ENCRYPTION

The protection of data against unauthorized access in communication systems is inevitably associated with the use of cryptographic methods. The original set of applications that used cryptographic protection, mainly for government and military systems, has been significantly expanded in the modern context to numerous day-to-day services, such as automated teller machines (ATMs), cable TV distribution systems, privacy protection systems in computer networks, online payment services, and mobile networks. In cryptographic procedures, the information to be protected is referred to as "plaintext" (or simply the "message"), and the masking operation is called encryption. The encrypted plaintext is called "ciphertext", and the set of rules that govern the encryption process is called the encryption algorithm. The execution of such an algorithm directly depends on an "encryption key", which is provided as an input to the algorithm along with the message. To make it possible to recover the original message from the received ciphertext, a decryption algorithm provided with the corresponding "decryption key" is used. A block diagram of an encryption/decryption system is shown in Fig. 7.

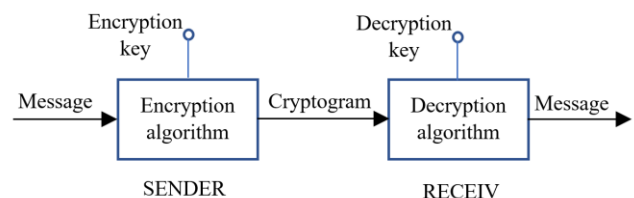


Fig. 7. General scheme for encryption and decryption.

Depending on the adopted concept for key distribution, this type of system can be categorized as symmetric or asymmetric; a symmetric system uses identical keys on both the transmitting and receiving sides, whereas an asymmetric system is based on the use of different keys for each of the two parties participating in communication. In addition, cryptographic algorithms can be classified in accordance with the way in which the data are formatted: encryption can be implemented based on bitwise principles, or groups of related bits (called "blocks") can be regarded as the basic units in an encryption/decryption procedure. Such so-called "block encryption algorithms" are especially popular in modern systems. The most significant algorithm in this class is undoubtedly the Advanced Encryption Standard (AES) algorithm. For the developed TRX, AES-256 was selected as one of the best options for implementing the desired protection level. Moreover, we chose the asymmetric key distribution concept. The key will change on a daily basis,

and any TRX whose key is invalid will not be able to join the network or receive data.

VI. TEST RESULTS

To characterize modem performance and measure the minimum SNR at which the modem can work reliably, we performed tests using attenuators to simulate free-space path loss. The test setup configuration is presented in Fig. 8. We expected the system to work at SNRs below 6 dB.

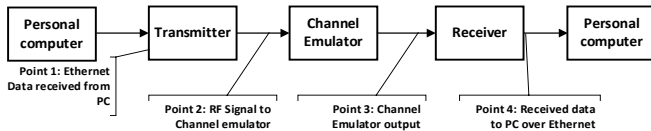


Fig. 8. Test setup configuration.

The proposed modem operates at 4.2 dB SNR for quadrature phase-shift keying (QPSK) demodulated signals, the constellation of which is presented in Fig. 9.

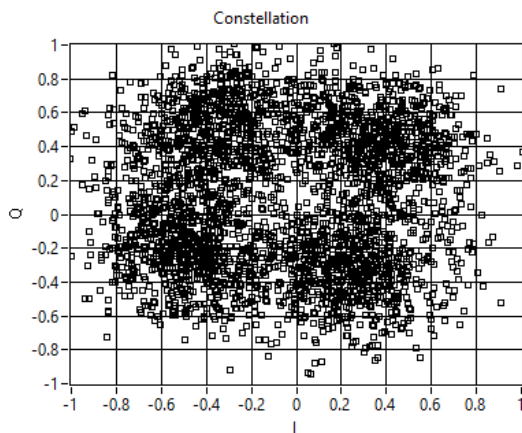


Fig. 9. Demodulated signal constellation when SNR = 4.2 dB.

The measurement results are given in Table III.

TABLE III  
MEASUREMENT RESULTS

Parameter name	Test 1	Test 2	Test 3
Received signal SNR	4.9 dB	4.2 dB	3.2 dB
Modulation type	QPSK	QPSK	QPSK
Symbol rate	10 Ms/s	10 Ms/s	10 Ms/s
FEC status	Enabled	Enabled	Enabled
Tx frequency	1610 MHz	1610 MHz	1610 MHz
Rx frequency	1610.01 MHz	1610.01 MHz	1610.01 MHz
Total bits transmitted	4096	4096	4096
Error bit before FEC	78	95	391
Error bits after FEC	0	0	6

A constellation for signals with a higher SNR is given in Fig. 10.

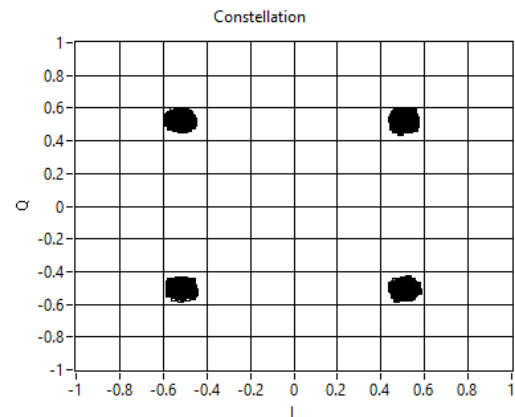


Fig. 10. Demodulated signal constellation when SNR = 33 dB.

The latency was measured as the time elapsed between the time when a frame of 512 data bytes was received from the PC (Fig. 8, point 1) on the transmitter side and the time when the corresponding 512 bytes were ready to be transmitted to the PC on the receiver side (Fig. 8, point 4).

The results achieved during the field tests are presented in TABLE IV.

TABLE IV  
TEST RESULTS

Parameter name	Expected parameter value	Measured parameter value
Operating frequency band	700 MHz to 2.4 GHz	700 MHz to 2.4 GHz
Maximum output power	30 dBm	33 dBm
Noise figure of receiver	4.5 dB	3.8 dB
Maximum bandwidth	20 MHz	20 MHz
Maximum symbol rate	20 Ms/s	20 Ms/s
Maximum bit rate	80 Mbit/s (5 km, LOS, 1 GHz)	80 Mbit/s (5 km, LOS, 1 GHz)
Maximum distance (bit rate = 250 kbit/s)	50 km (LOS, 1 GHz, Tx power =30 dBm)	100 km (LOS, 1 GHz, Tx power =33 dBm)
Modulation types used	BPSK, QPSK, 8-QAM, 16-QAM	BPSK, QPSK, 8-QAM, 16-QAM
Latency (for 512 bytes), this is time between Tx and Rx, measured on Ethernet port side	1.6 ms	1.44 ms
Current consumption (no Tx happening, Rx is receiving data)	700 mA	600 mA
Supply voltage	12 V	12 V

Also, we compare with existing modems, SkyHopper PRO [20] and SOL8SDR2x1W-P [21], and the comparison results are presented in TABLE V.

From the compared results we can see that the proposed system provides continuous coverage of wider frequency ranges, has higher data rate and supports single carrier modulations. Additionally, our system supports cognitive functionality which includes spectrum monitoring and optimal modulation selection.

TABLE V  
THE PARAMETER COMPARISON WITH EXISTING MODEMS

Parameter name	Proposed modem	SkyHopper PRO	SOL8SDR2x1W-P
Standard Frequency range	700 MHz to 2400 MHz	2.4 GHz (ISM) & 5.8 GHz (ISM)	1.14 to 1.5GHz, 1.67 to 2.35 GHz, 1.98 to 2.7 GHz, 4.4 to 5.0 GHz
Output power	2W	Not given	1 W
Distance	Up to 100 km	6 km	Not given
Mesh support	IP MESH	IP MESH	IP MESH
Modulation type	BPSK, QPSK, 8-QAM, 16-QAM	OFDM	COFDM
Maximum data rate	80 Mbps	6 Mbps	Not given
Temperature range	-40°C to +85°C	-20°C to +85°C	-10°C to +55°C
Encryption	AES256	AES128, AES256	AES128, AES256
Sensitivity	-105 dBm for 500 Kbps	-101 dBm	Up to -110dBm
Power Supply	7V to 18V DC	7.5V to 24V DC	8V to 17.5V DC
Cognitive functionality	Support	Not given or do not support	Not given or do not support

## VII. CONCLUSION

In this paper, we present an adaptive radiocommunication system that provides real-time data processing, transmission and reception by means of the following developed modules: a transmitter and a receiver including signal formation, modulation–demodulation, and coding–decoding algorithms, each of which is developed as a separate block and has automated cognitive features.

The main applications for this system are cognitive radiocommunication systems and applications for which customized systems are needed, such as UAVs and airborne applications. As we have used the software-defined radio approach during development, it will be adaptable for future purposes and provide the possibility of onsite software updates for bug fixing or adding new features.

As a continuation of this work, we plan to add amelioration, and the operation range should be increased in the presence of jamming signals. COFDM and Spread Spectrum modulation schemes should be added to mitigate multipath problems for a non-LOS environment. Operation at frequency ranges from 2.7 GHz to 6 GHz should be evaluated and analyzed.

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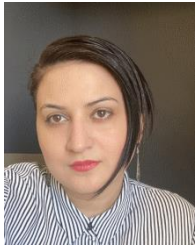
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**Greta A. Vardanyan** was born in Yerevan, Armenia, in 1988. She was awarded a B.S. degree in Physics and Technology of Optical Communication Systems by the State Engineering University of Armenia, Yerevan, Armenia, in 2009 and an M.S. degree in Radioengineering and Communication Systems by the State Engineering University of Armenia, Yerevan, Armenia, in 2011. She is currently pursuing a Ph.D. degree in Communication Systems at the National Polytechnic University of Armenia, Yerevan, Armenia. From 2009 to 2010, she

was an intern at National Instruments (NI), Yerevan, Armenia. From 2010 to 2019, she was a System Engineer at NI, Yerevan, Armenia. From 2019 to 2021, she was a Senior Application Engineer at NI, Yerevan, Armenia. From 2011 to 2015, she was a Research Assistant with the Institute of Radiophysics and Electronics, National Academy Sciences of Armenia, Ashtarak, Armenia. Currently, she is a Senior Systems Engineer at OLYMP Engineering, Yerevan, Armenia.



**Martin Ts. Ayvazyan** was awarded an M.S. degree in Radio Engineering by the Institute of Radio Physics and Electronics of the Armenian Academy of Sciences, Yerevan, Armenia, in 1979; a Ph.D. degree in Radio Electronics by the Institute of Radiotechnics and Electronics of the Academy of Sciences, Moscow, Russia, in 1985; and a Doctor of Technical Sciences (Engineering) degree by the National Polytechnic University of Armenia in 2020.

From 1982 to 1990, he was a senior scientific worker at the Institute of Radio Physics and Electronics of the Armenian Academy of Sciences, Yerevan, Armenia. Currently, he is an Associate Professor and the Head of the 5G Research Group at the Institute of IT and Electronics, National Polytechnic University of Armenia, Yerevan, Armenia. His research interests include millimeter wave communications, radio-frequency component design and mobile communications.



**Orbel Zh. Sevoyan** was awarded an M.S. degree in Radiotechnics and Communication Systems by the State Engineering University of Armenia, Yerevan, Armenia, in 2006 and a Ph.D. degree in Radiotechnics and Communication Systems by the Institute of Radio Physics and Electronics of the Armenian Academy of Sciences, Ashtarak, Armenia, in 2009. From 2005 to 2014, he was an engineer at the Institute of Radio Physics and Electronics of the Armenian Academy of Sciences, Ashtarak, Armenia. From 2007 to 2011, he was a System Engineer at National Instruments,

Yerevan, Armenia. From 2009 to 2015, he was a lecturer at the State Engineering University of Armenia, Yerevan, Armenia. Since 2010, he has been CEO and director of OLYMP Engineering LLC, Yerevan, Armenia.

His work includes the development of radio communication systems, especially hardware design and software communication protocols and algorithms.