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Hybrid multilevel inverter using switched capacitor with boosting and self-balancing capability

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ABSTRACT

Switched capacitor based multilevel inverters with boosting capability are emerging as single stage DC–AC conversion in utilizing low voltage DC sources such as solar PV and fuel cell. This paper proposes a single-phase hybrid multilevel inverter topology based on a switched capacitor that is capable of generating 9-levels along with a voltage gain of 2. The components required to construct the basic module of topology are 11 switches, 1 diode and 2 capacitors. The voltage balancing of the switched capacitors is achieved with the help of a modulation strategy, thereby eliminating the need of sensors. The theoretical loss analysis of the inverter is presented and the nearest level control based fundamental switching frequency modulation technique is employed to study the performance of the proposed inverter. The effectiveness of the suggested topology is validated with the help of a prototype built in the laboratory. The superiority of the proposed topology is assessed with the help of comparison with existing topologies.

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KEYWORDS
Multilevel inverter; switched capacitor; nearest level control

1. Introduction

DC to AC conversion plays a vital role in harnessing renewable power sources, such as solar photovoltaic system, wind energy conversion system and fuel cells. Multilevel inverters are proposed for the above-mentioned applications owing to inherent advantages including reduced dv/dt, reduced voltage stress across the switch, improved voltage and current THD, fault-tolerant operation and reduced common mode voltage [1–3]. The conventional multilevel inverter topologies include diode clamped multilevel inverter, flying-capacitor multilevel inverter and cascaded H-bridge multilevel inverter. The main limitation of conventional multilevel inverter topologies is that as the number of levels increases, the total number of components required also increases drastically [4]. To overcome the above-said limitation, various multilevel inverter topologies with Reduced Device Count (RDC) are proposed in the literature. Comprehensive comparisons of the various multilevel inverters with reduced device count are discussed in [5–7]. RDC multilevel inverters with reduced sources or with a single source using switched capacitors are gaining attention these days. The voltage balancing of a switched capacitor is done with an appropriate switching sequence to maintain the voltage across it without any additional voltage sensor and closed loop control. As a result, the voltage across the switched capacitor is self-balanced. The various multilevel inverters using switched capacitor units without boosting capability are discussed in [8–10].

The conversion of low voltage DC supply from sources such as solar PV, fuel cell and hybrid electric vehicle batteries into AC requires a two stage conversion or *Z*-source inverter. The two stage conversion has its own limitations such as reduced reliability and large voltage stress in the second stage. On the other hand, *Z*-source inverters are bulkier due to the inductance used in them. The switched capacitor based multilevel inverter with boosting capability is proposed as an alternative for the above applications as a single stage solution.

Self-balancing type compact switched capacitor multilevel inverter with a voltage gain of 2 was proposed in [11]. To extend this topology for higher levels by cascade connection, it requires two floating capacitors.

The dual T-type 7-level inverter with boosting capability is proposed in [12] with a boosting factor of 1.5. The main limitation of this topology is that it requires four floating capacitors.

Symmetric/asymmetric hybrid multilevel inverters with boosting capability are proposed in [13]. This basic module of topology requires three switched capacitor units along with a bidirectional switch to realize the 7-level with a voltage boost of 1.5.

In [14], Sing Lee *et.al* proposed two new switched capacitor based 7-level boost inverter topologies with a boosting factor of 1.5. But this topology needs three capacitors and a bidirectional switch.

In [15], boosting inverter based on a separate level and polarity generation module is discussed. However,

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its polarity generation module has to withstand high voltage stress for realizing higher voltage levels which limit the number of levels to be realized.

A 9-level step-up inverter with a voltage gain of 4 is proposed in [16]. However, voltage stress across some of the switches used in the topology is twice the supply voltage, and the rating of one of the switched capacitors is also twice the supply voltage.

According to the literature, a boosting inverter with fewer power semiconductor switches and capacitors, as well as uniform voltage blocking capabilities, is required. In addition, a boosting inverter that does not use a bidirectional switch is required to improve the efficiency of topology. The higher blocking voltage requirement can also be reduced by using an inverter topology that does not include a separate polarity generation module.

This paper proposes a hybrid 9-level inverter topology with a voltage boosting factor of 2, which is greater than [11–13] and [14]. Four different methods are suggested to extend the proposed topology for a higher number of voltage levels and boosting. The basic sub module of the proposed topology employs two switched capacitors and both the capacitor voltages are regulated naturally without the need of a sensor. Elimination of the sensor and voltage balancing without a closed loop control improves the reliability of the circuit and reduces the cost. As the suggested topology needs only half bridge modules and does not require a bidirectional switch, the standard half bridge driver circuit can be employed, thereby reducing the complexity.

Also, it is designed in such a way that each switch has to block voltage equal to or lesser than the input supply voltage. A hardware prototype is fabricated in the laboratory and its performance is studied with the help of a fundamental switching frequency based nearest level modulation technique.

2. Proposed 9-level hybrid boost inverter

The power circuit diagram of the suggested 9-level inverter with boosting capability is shown in Figure 1. The proposed topology basically consists of an H-bridge module, a boosting module based on H-bridge and a two level switched capacitor (2L-SC) module supplied from a single DC source. Thus, the realization of the proposed multilevel inverter is possible with an existing half bridge module. The proposed topology can generate nine voltage levels with voltage levels: $\pm V_{DC}/2$, $\pm V_{DC}$, $\pm 3V_{DC}/2$, $\pm 2V_{DC}$ and 0. The different working states of the inverter along with capacitor charging and discharging status are given in Table 1. The switches S_x and $S_{x'}$ (where x ranges from 1 to 5) are complementary to each other.

The blocking voltage requirement of switches S_1 to S_4, S_1' to S_4' and S_6 is equal to input DC voltage V_{DC} and switch S_5 and S_5' has to block half the input voltage

Table 1. Different switching states of the proposed inverter.

Voltage levels	S_1	S_2	S_3	S_4	S_5	S_6	Capacitor (C_1)	Capacitor (C_2)
$+2V_{DC}$	1	0	0	1	0	0	↓	–
$+3V_{DC}/2$	1	0	0	1	1	0	↓	↑
$+V_{DC}$	1	0	1	1	0	1	↑	–
$+V_{DC}/2$	1	0	1	1	1	1	↑	↑
0	0	0	0	0	0	0	–	–
$-V_{DC}/2$	1	1	1	1	1	1	↑	↓
$-V_{DC}$	1	1	1	0	0	1	↑	–
$-3V_{DC}/2$	0	0	1	0	1	0	↓	↓
$+2V_{DC}$	0	1	1	0	0	0	↓	–

↓ Discharging; ↑ Charging; – No effect.

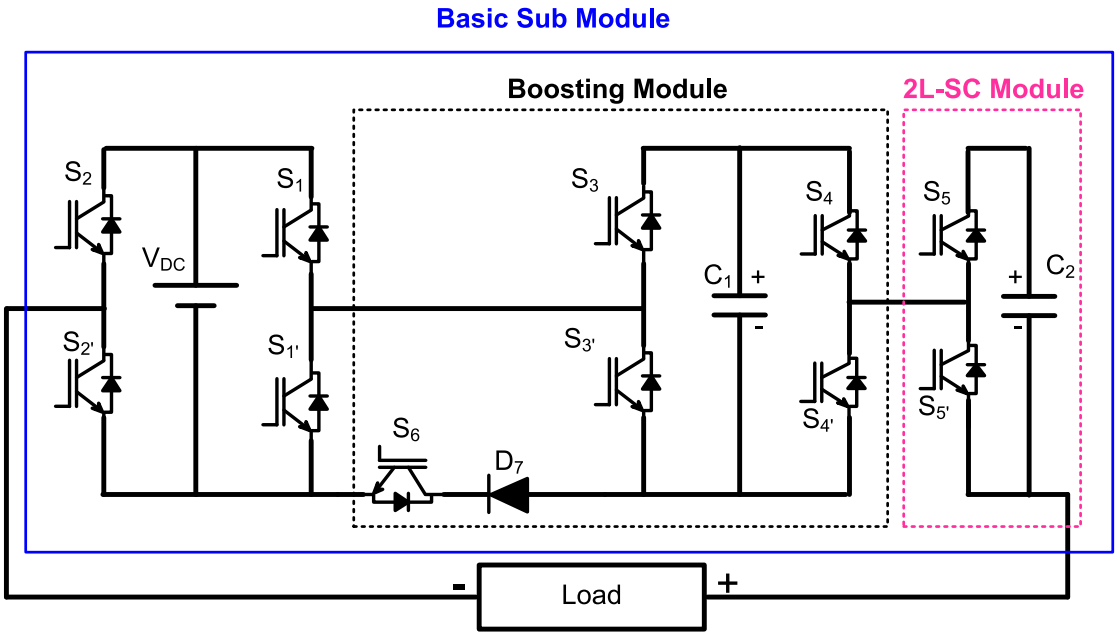

Figure 1. Circuit diagram of the proposed hybrid multilevel inverter.

$V_{DC}/2$. The diode D_7 is required to avoid short circuit of capacitor C_1 voltage when switch S_3 and S_1' are conducting.

As evident from the switching states of the inverter, when switch S_6 is turned ON, the capacitor C_1 and DC source are connected in parallel and they charge instantly to the DC source voltage as the parasitic associated with the charging path is minimum. Thus the steady state voltage across switched capacitor C_1 is equal to the DC source voltage. The voltage boosting is achieved by connecting the source voltage and capacitor voltage in series across the load.

To regulate the voltage across the capacitor C_2 to half the DC source voltage, it is charged during the positive half cycle of output voltage and discharged during the negative half cycle of output voltage. The average current flowing through the capacitor is made to zero by keeping the charging and discharging intervals identical over each half of the AC output voltage. The average current flowing through the capacitor during voltage levels $\pm V_{DC}/2$ and $\pm 3V_{DC}/2$ with load impedance Z is given by the following equations:

$$\begin{aligned} i^{+}_{Cavg,\frac{V_{DC}}{2}} &= \frac{V_{DC}-v_C}{Z},\ i^{+}_{Cavg,\frac{3V_{DC}}{2}} = \frac{2V_{DC}-v_C}{Z} \\ i^{-}_{Cavg,\frac{V_{DC}}{2}} &= \frac{v_C}{Z},\ i^{-}_{Cavg,\frac{3V_{DC}}{2}} = \frac{V_{DC}+v_C}{Z} \end{aligned} \tag{1}$$

The net charge across the capacitor for the fundamental period (T) is given by,

$$\begin{aligned} Q_{net} &= \left\{ i^{+}_{Cavg,\frac{V_{DC}}{2}} + i^{+}_{Cavg,\frac{3V_{DC}}{2}} - i^{-}_{Cavg,\frac{V_{DC}}{2}} \right. \\ &\quad \left. - i^{-}_{Cavg,\frac{3V_{DC}}{2}} \right\} T \\ &= \left\{ \frac{2V_{DC}-4v_C}{Z} \right\} T \end{aligned} \tag{2}$$

At the steady state, due to the symmetry of the current waveform, the net charge through the capacitor C_2 is zero. By substituting net charge to zero in Equation (2), a steady state voltage across the capacitor C_2 is found to be half the supply voltage.

3. Recommended extension methods

For extending the basic module to realize a higher number of levels, four different methods have been suggested. The extension method-1 is used to realize higher levels and boosting, with the help of a single DC source, whereas extension method-2–4 facilitates integrating multiple sources. The details of the four methods are explained in the following sub-sections.

3.1. Extension method-1

In method-1, "n" number of boosting modules is connected in cascade to realize a higher number of voltage levels as shown in Figure 2. In method-1, along with an increase in output voltage levels, the voltage gain of the inverter is also increased. The number of boosting modules required to realize "N_L" voltage levels in output with method-1 is given by (3) and voltage gain (G) obtained is given by (4).

$$N_L = 4n + 5 \tag{3}$$

$$G = n + 1 \tag{4}$$

3.2. Extension method-2

In method-2, "p" number of basic sub-modules are connected in a cascade manner; while doing so only the first stage requires boosting and 2L-SC modules, and the remaining "p-1" stage does not require a 2L-SC module. This method employs symmetrical sources as shown in Figure 3. This method can produce the maximum output voltage equal to twice the sum of all input voltages. The number of levels obtained by this method is given by,

$$N_L = 8p + 1 \tag{5}$$

3.3. Extension method-3

Asymmetric sources are proposed for cascaded multilevel inverters to realize higher voltage levels with a lesser number of switches [5]. The extension methods 3 and 4 are based on asymmetric sources. The extension method-3 is similar to extension method-2, but it employs multiple sources with binary configuration, in which, the DC source voltage magnitude vary by geometric progression with a factor of 2 (i.e. $V_{DCn} = 2^{\wedge(n-1)} V_{DC}$). The number of levels obtained with "p" number of extension modules in cascade is given by,

$$N_L = 2^{(p+3)} - 7 \tag{6}$$

3.4. Extension method-4

In method-4, "p" number of basic sub modules are connected in a cascade manner by employing multiple sources with trinary configuration, in which, the DC source voltage magnitude vary based on geometric progression with a factor of 3 (i.e.$V_{DCn} = 3^{\wedge(n-1)} V_{DC}$) as shown in Figure 4. The number of levels obtained is given by,

$$N_L = 4 \times \{3^p - 1\} + 1 \tag{7}$$

4. Sizing of switched capacitors

The size of the switched capacitor plays a significant role on the weight, volume and cost of the proposed inverter. The calculation of capacitance for switched capacitors C_1 and C_2 are given in the following sub-sections.

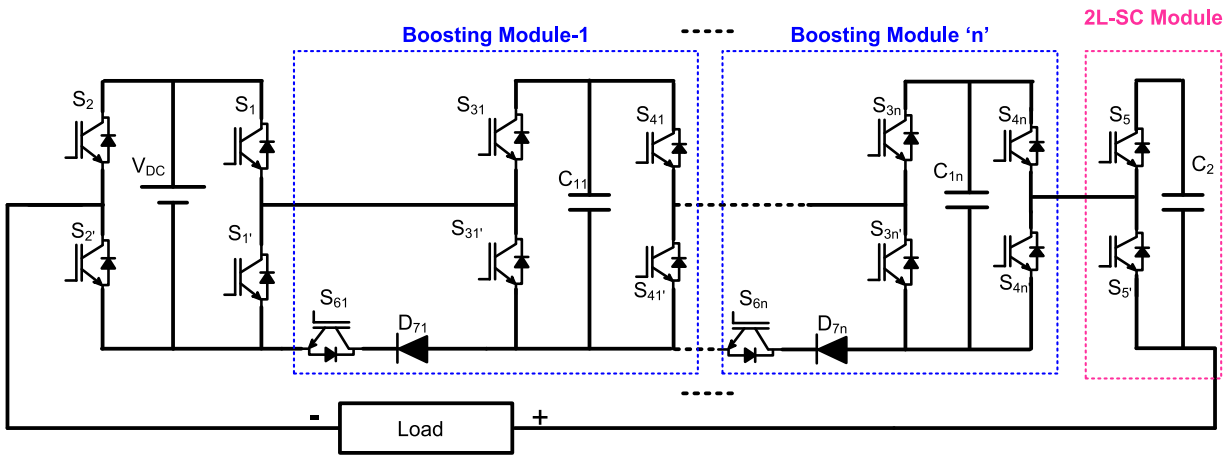

Figure 2. Extension for higher levels using method-1.

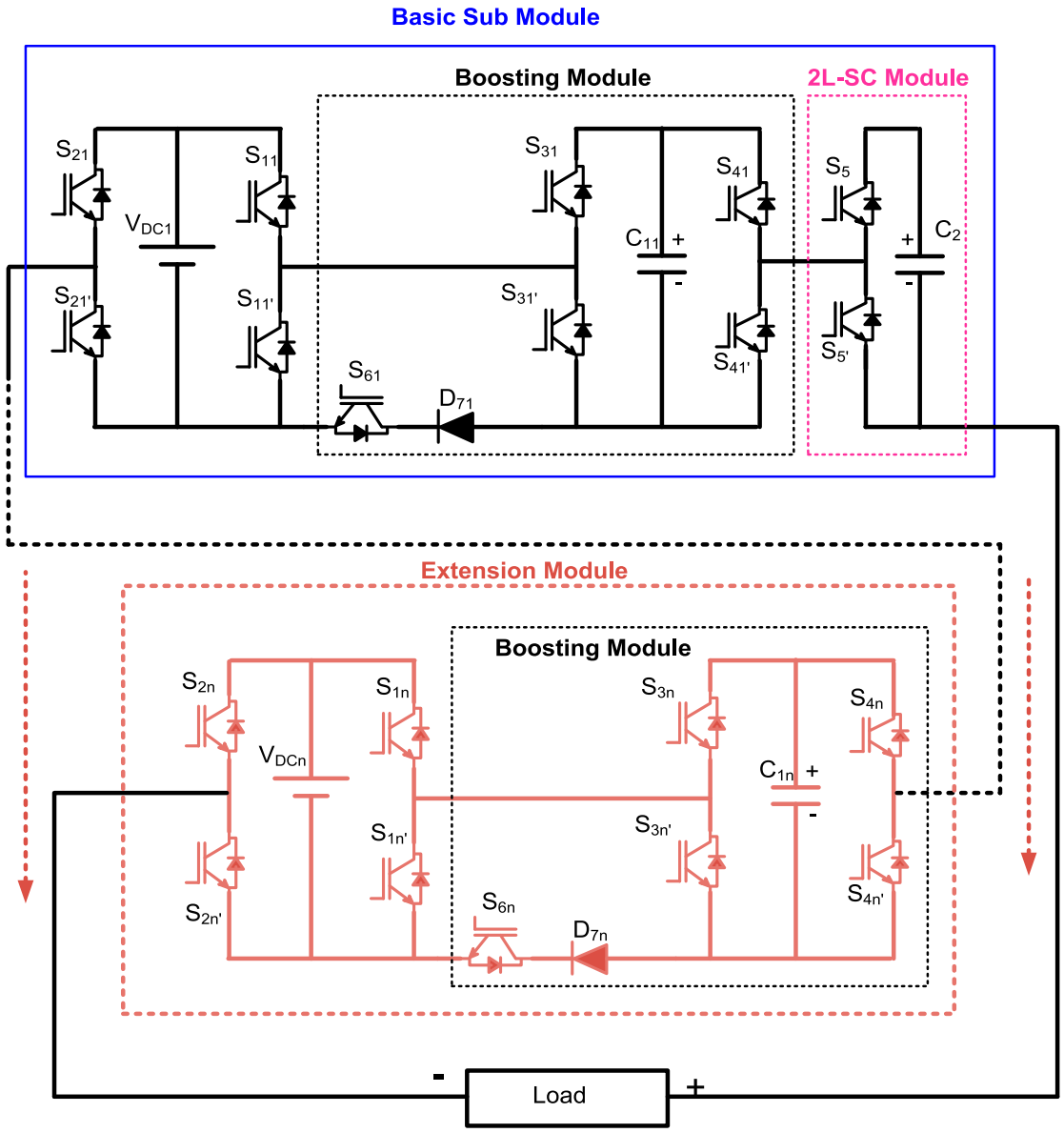

Figure 3. Extension for higher levels using method-2.

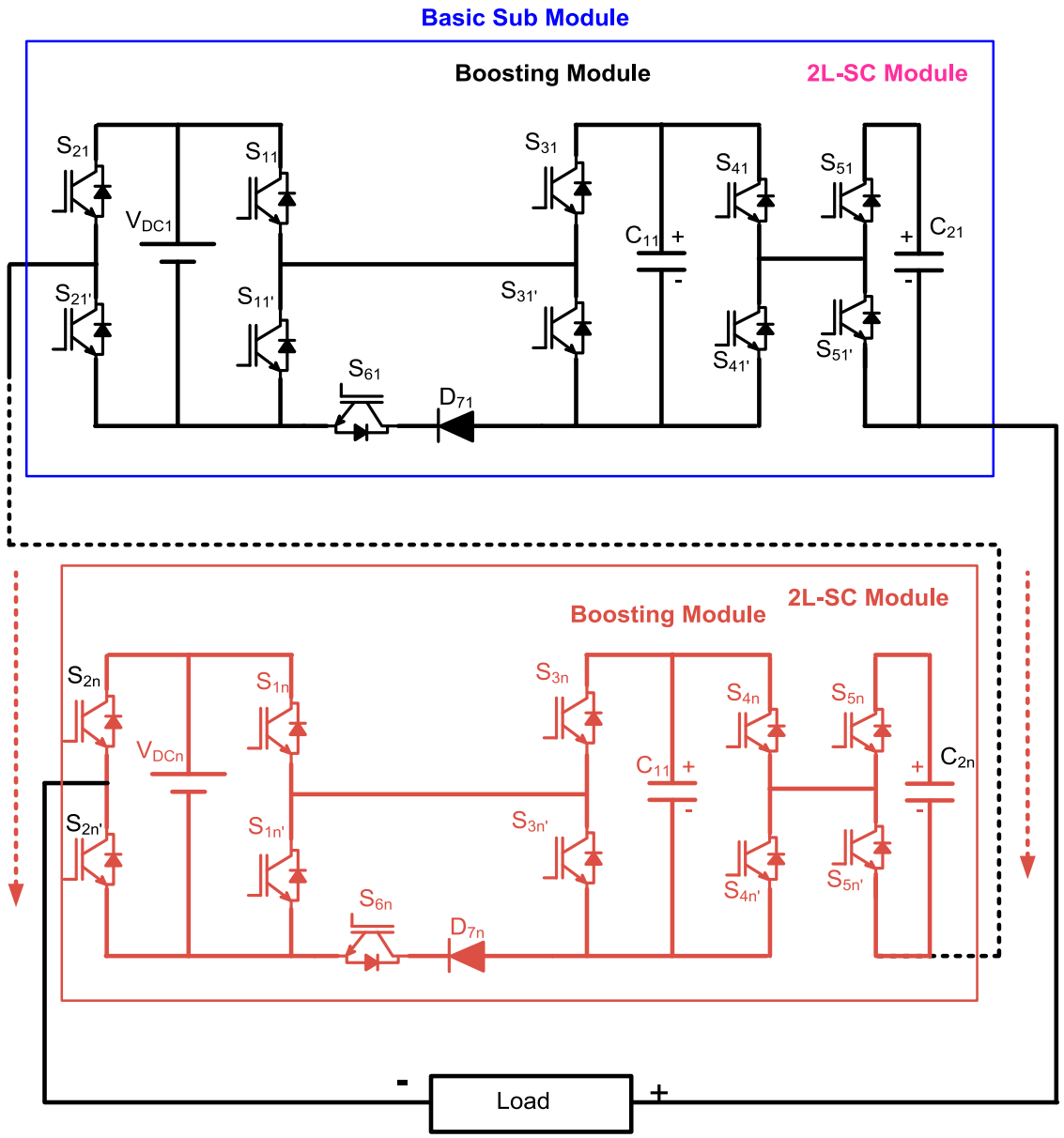

Figure 4. Extension for higher levels using Method-4.

4.1. *Calculation of capacitance C_1*

When the voltage levels are $\pm V_{DC}$ and $\pm V_{DC}/2$, the capacitor C_1 is charged from the DC source. During the above-said voltage levels, capacitor C_1 is charged to input DC voltage instantly as the parasitic of charging path is very low. Also, capacitor C_1 discharges when voltage levels are $\pm 2V_{DC}$ and $\pm 3V_{DC}/2$. The value of capacitance C_1 is calculated based on the prolonged discharging period as described in [13]. The longest interval for which the capacitor C_1 discharges is between the interval α_3 to π-α_3, as shown in Figure 5.

The amount of electric charge discharged by capacitor C_1 is given by,

$$\Delta Q_{C1} = \frac{1}{\omega}\int_{\alpha_3}^{\pi-\alpha_3} I_m \sin(\omega t - \phi)d\omega t$$

$$= \frac{I_m}{\omega}[-\cos(\omega t - \phi)]_{\alpha_3}^{\pi-\alpha_3}$$

$$= \frac{I_m}{\omega}[-\cos(\pi - (\alpha_3 + \phi)) + \cos(\alpha_3 - \phi)] \quad (8)$$

On simplifying the above Equation (6), the expression for ΔQ_{C1} is given by,

$$\Delta Q_{C1} = \frac{2I_m}{\omega}[\cos\alpha_3 \times \cos\phi] \quad (9)$$

From the above equation, the expression for voltage ripple is calculated by,

$$\Delta V_{C1} = \frac{\Delta Q_{C1}}{C_1} = \frac{2I_m}{\omega C_1}[\cos\alpha_3 \times \cos\phi] \quad (10)$$

The minimum value of capacitance required for the given voltage ripple and peak load current is given by the expression,

$$C_1 = \frac{2I_m}{\Delta V_{C1}\omega}[\cos\alpha_3 \times \cos\phi] \quad (11)$$

where $\omega = 2^*\pi^*$fundamental frequency of inverter and $\cos\phi$ = power factor of the load. Hence, it is

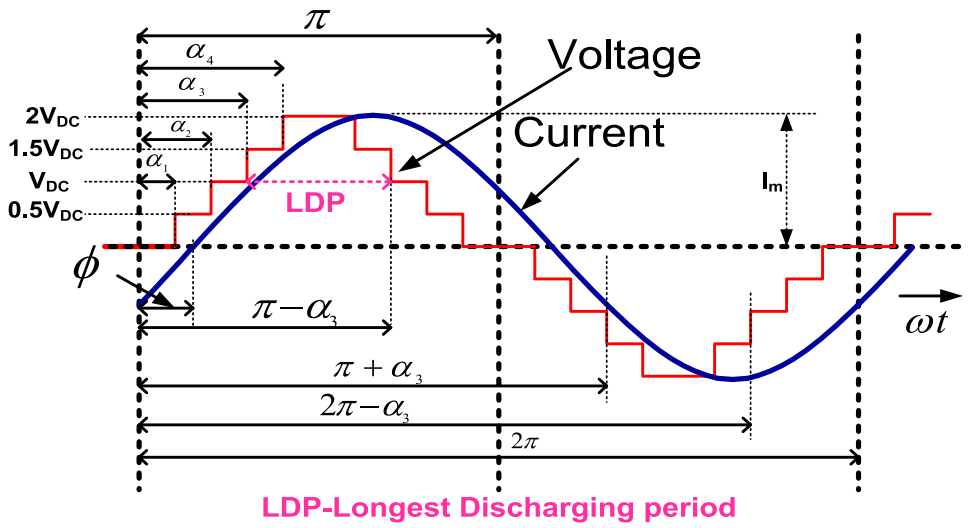

Figure 5. Discharging intervals of the capacitors.

inferred that the capacitance value is directly proportional to peak load current and the operating power factor of the load.

The value of capacitance required to regulate the voltage within 5% of rated voltage (60 V) using the above formula is arrived to be 1662 μF for the load with $R = 50\,\Omega$ and $L = 90$ mH, and peak load current of 1.6 A. In the prototype built, the nearest available capacitance of 1600μF is employed.

4.2. Calculation of capacitance of C_2

The value of capacitance C_2 is calculated based on the electric charge associated with capacitor C_2 during discharging given by,

$$\begin{aligned}\Delta Q_{C2} &= \frac{2}{\omega}\left\{\int_{\pi+\alpha_1}^{\pi+\alpha_2} I_m \sin(\omega t-\phi)d\omega t \right.\\ &\quad \left. + \int_{\pi+\alpha_3}^{\pi+\alpha_4} I_m \sin(\omega t-\phi)d\omega t\right\}\\ &= \frac{2I_m}{\omega}\{[-\cos(\omega t-\phi)]_{\pi+\alpha_1}^{\pi+\alpha_2}\\ &\quad + [-\cos(\omega t-\phi)]_{\pi+\alpha_3}^{\pi+\alpha_4}\}\\ &= \frac{2I_m}{\omega}[\cos\phi(\cos\alpha_4+\cos\alpha_2-\cos\alpha_3\\ &\quad -\cos\alpha_1)-\sin\phi(\sin\alpha_4+\sin\alpha_2\\ &\quad -\sin\alpha_3-\sin\alpha_1)] \qquad (12)\end{aligned}$$

From the above equation, the expression for voltage ripple is calculated by,

$$\begin{aligned}\Delta V_{C2} &= \frac{2I_m}{\omega C_2}[\cos\phi(\cos\alpha_4+\cos\alpha_2-\cos\alpha_3\\ &\quad -\cos\alpha_1)-\sin\phi(\sin\alpha_4+\sin\alpha_2-\sin\alpha_3\\ &\quad -\sin\alpha_1)] \qquad (13)\end{aligned}$$

The minimum value of capacitance required for the given voltage ripple and peak load current is given by the expression,

$$\begin{aligned}C_2 &= \frac{2I_m}{\omega\Delta V_{C2}}[\cos\phi(\cos\alpha_4+\cos\alpha_2-\cos\alpha_3\\ &\quad -\cos\alpha_1)-\sin\phi(\sin\alpha_4+\sin\alpha_2-\sin\alpha_3\\ &\quad -\sin\alpha_1)] \qquad (14)\end{aligned}$$

The value of capacitance required to regulate the voltage within 5% of rated voltage (30 V) using the above formula is arrived to be 1534μF for the load with $R = 50\Omega$ and $L = 90$mH, and peak load current of 1.6 A. In the prototype built, the nearest available capacitance of 1600μF is employed.

5. Loss analysis

The theoretical loss analysis of the proposed converter is presented in this section by assuming the load to be a unity power factor. The total loss in the converter is the sum of switching loss, conduction loss in semiconductor switches, and power losses of the capacitor during charging and discharging.

5.1. Switching losses

Switching loss occurs when a switch is turned ON and OFF. The number of times a switch is turned ON and OFF during one full cycle of output voltage waveform greatly affects the switching loss of the converter. With the linear approximation of voltage across the switch and current through the switch, the energy loss occurring during turn on and turn off is given by (15) and (16), as briefed in [17,18]. The power loss occurring in the *i*th switch during switching in one fundamental cycle is given by (17).

$$E_{ON,i} = \int_0^{t_{ON}} v(t)\, i(t)dt$$

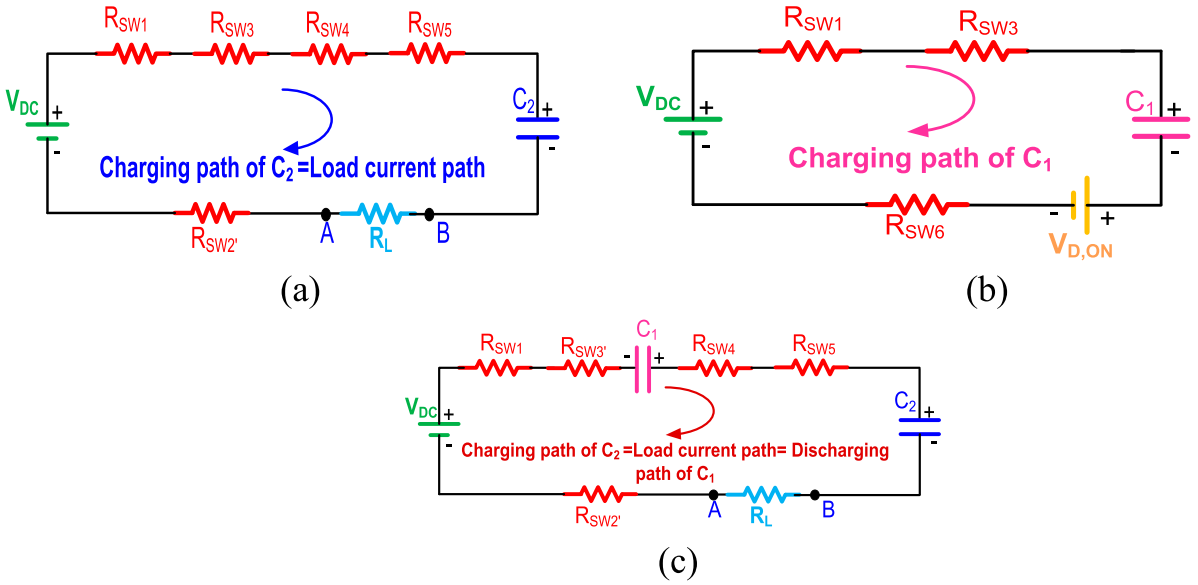

Figure 6. Charging paths of capacitors for the proposed converter (a) Charging path of C_2 when the output level is $+0.5V_{DC}$, (b) Charging path of C_1 when the output level is $\pm 0.5V_{DC}$ and V_{DC} (c) Charging path of C_2 and discharging path of C_1 when the output level is $+1.5V_{DC}$.

$$= \int_0^{t_{ON}} \left\{ \left(V_{SW,\,i,\,\mathrm{ON}} \frac{t}{t_{ON}} \right) \times \left(\frac{-I_i}{t_{ON}} (t - t_{ON}) \right) \right\} dt$$

$$= \frac{1}{6} \times V_{SW,\,i,\,\mathrm{ON}} \times I_i \times t_{ON} \tag{15}$$

$$E_{OFF,i} = \int_0^{t_{OFF}} v(t)\, i(t) dt$$

$$= \int_0^{t_{ON}} \left\{ \left(V_{SW,\,i,OFF} \frac{t}{t_{OFF}} \right) \times \left(\frac{-I_i^-}{t_{ON}} (t - t_{OFF}) \right) \right\} dt$$

$$= \frac{1}{6} \times V_{SW,\,i,OFF} \times I_i^- \times t_{OFF} \tag{16}$$

$$P_{SW,Loss,\,i} = \frac{1}{6T} \left\{ \sum_{j=1}^{j=N_{ON}} V_{SW,\,i,\,\mathrm{ON}} \times I_i \times t_{ON} + \sum_{j=1}^{j=N_{OFF}} V_{SW,\,i,OFF} \times I_i^- \times t_{OFF} \right\} \tag{17}$$

The total switching losses in 11 switches used in the basic sub-module is given by,

$$P_{\mathrm{SW,Total\ loss}} = \sum_{i=1}^{i=11} P_{SW,Loss,\,i} \tag{18}$$

where $V_{SW,i,\mathrm{ON}}$ = voltage across the ith switch before turn ON, $V_{SW,i,\mathrm{OFF}}$ = voltage across the ith switch after turn OFF, I_i = current through ith switch after turn ON, $I_i^{'}$ = current through ith switch before turn OFF, t_{ON} = turn on time of switch and t_{OFF} = turn off time of the switch. In a case of resistive load, the current through the switches at different voltage levels "L" can be expressed as:

$$|I_i| = |I_i^-| = L \frac{V_{DC}}{R_L} \quad L = 0.5,\ 1,\ 1.5,\ 2 \tag{19}$$

Using the above formula, the total switching loss obtained is given by,

$$P_{SW,Total\,loss} = \frac{1}{6} \times \frac{42.5}{T} \times \frac{V_{DC}^2}{R_L} \times (t_{ON} + t_{OFF}) \tag{20}$$

5.2. Conduction loss

The conduction losses of the proposed converter are the sum of the losses occurring in semiconductor switches in load current path at different output voltage levels and losses occurring during charging and discharging of the capacitors as discussed in [19].

The capacitor C_1 is charged by the input DC source when the output voltage level is $\pm 0.5V_{DC}$ and $\pm V_{DC}$ through three switches and one diode, its charging path is shown in Figure 6(b). The energy loss occurring during the charging of capacitor C_1 is the difference of energy flowing out of the input DC source, and that following into capacitor C_1 is given by,

$$\Delta E_{C1} = V_{DC} C_1 \Delta V_{C1} - \{(V_{DC} - V_{D,ON}) C_1 \Delta V_{C1} - 0.5 C_1 \Delta V_{C1}^2\} \tag{21}$$

During one cycle of fundamental voltage, the capacitor C_1 is charged twice; thus, the power loss occurring

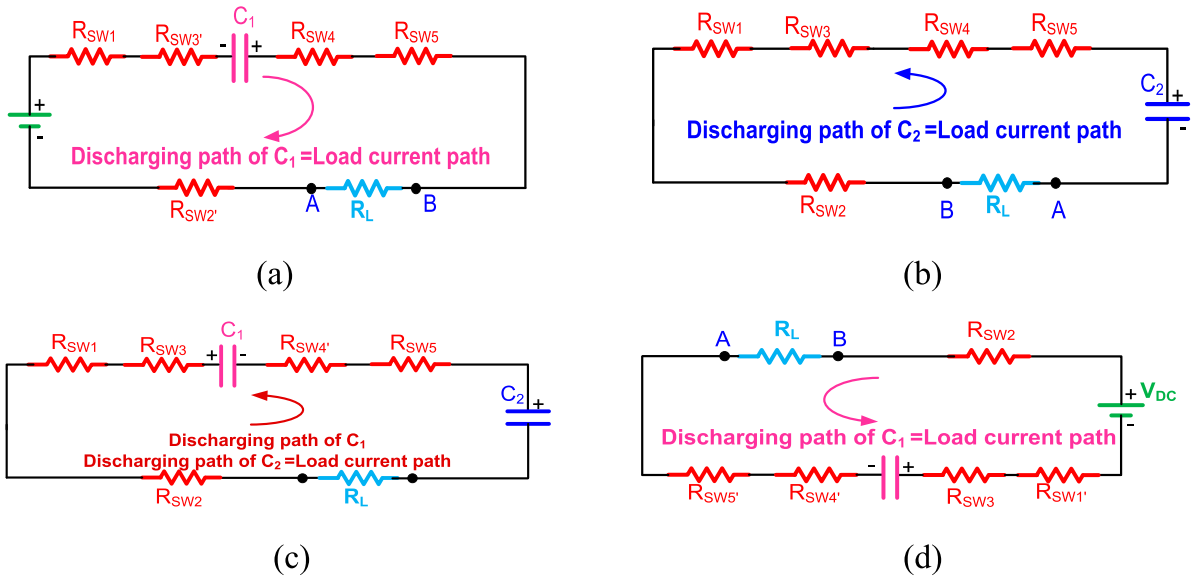

Figure 7. Discharging paths of capacitors for the proposed converter (a) Discharging path of C_1 when the output level is $+2V_{DC}$, (b) Discharging path of C_2 when the output level is $-0.5V_{DC}$, (c) Discharging path of C_2 and discharging path of C_1 when output level is $-1.5V_{DC}$ (d) Discharging path of C_1 when output level is $-2V_{DC}$.

Table 2. Comparison of performance parameters between proposed topology with existing topologies.

Topology	Source configuration	N_L	N_{SW}	N_D	TBV	V_{peak}	Possible number of capacitors
Proposed method-1	Single Source	$4N_C+1$	$5N_C+1$	N_C-1	$5N_C$	$V_{DC}N_C$	2,3,4...
[20] Method-1	Single Source	$2N_C+3$	$5N_C+4$	0	$5N_C+4$	$V_{DC}(N_C+1)$	1, 2, 3...
[13]	Single Source	$4N_C-5$	$5N_C-6$	N_C-2	$5N_C-7$	$\frac{2N_C-3}{2}$	3, 4, 5...
[21]	Single Source	$4N_C-3$	$5N_C-3$	0	$5N_C-3$	$V_{DC}(N_C-1)$	3,4,5...
Proposed method-2	Symmetric multiple sources	$8N_C-7$	$9N_C-7$	N_C-1	$9N_C-8$	$2V_{DC}(N_C-1)$	3, 4, 5...
Proposed method-3	Asymmetric multiple sources	$2^{(N_C+2)}-7$	$9N_C-7$	N_C-1	$(9\times 2^{(N_C-1)})-8$	$\frac{V_{DC}}{4}(2^{(N_C+2)}-8)$	3, 4, 5...
Proposed method-4	Asymmetric multiple sources	$4\times\left\{3^{\frac{N_C}{2}}-1\right\}+1$	$\frac{11N_C}{2}$	$\frac{N_C}{2}$	$5\times\left\{3^{\left(\frac{N_C}{2}\right)}-1\right\}$	$V_{DC}\times\left\{3^{\frac{N_C}{2}}-1\right\}$	2, 4, 6...
[11]	Symmetric multiple sources	$4N_C+1$	$\frac{11N_C}{2}$	0	$5N_C$	$V_{DC}N_C$	2, 4, 6...
[12]	Symmetric multiple sources	$\frac{3N_C}{2}+1$	$\frac{5N_C}{2}$	0	$\frac{11N_C}{4}$	$\frac{3V_{DC}N_C}{8}$	4, 8, 12...
[20] Method-2	Symmetric multiple sources	$4N_C+1$	$9N_C$	0	$9N_C$	$2V_{DC}N_C$	1, 2, 3...
[22]	Symmetric multiple sources	$\frac{8N_C}{3}+1$	$4N_C$	0	$\frac{11N_C}{3}$	$\frac{2V_{DC}N_C}{3}$	3, 6, 9...

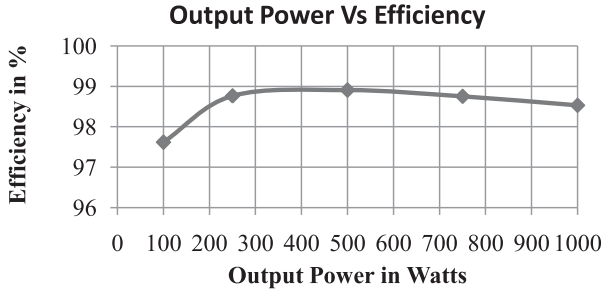

Figure 8. Output power vs. efficiency.

in charging of capacitor C_1 is:

$$P_{C1,Loss}=2\frac{\Delta E_{C1}}{T}=\frac{1}{T}\{C_1\Delta V_{C1}(2V_{D,ON}+\Delta V_{C1})\} \tag{22}$$

The capacitor C_2 is charged by the input DC source when the output voltage level is $+0.5V_{DC}$ and charged by the sum of DC source voltage and capacitor C_1 voltage when the output voltage level is $+1.5V_{DC}$ as illustrated in Figure 6(a) and (c), respectively. The energy loss occurring during the charging of capacitor C_2 is the difference of energy flowing out of the input DC source and that following into capacitor C_2 is given by,

$$\begin{aligned}\Delta E_{C2}=&V_{DC}C_2\Delta V_{C2}-(V_{DC}C_2\Delta V_{C2}\\&-0.5C_2\Delta V_{C2}^2)+2V_{DC}C_2\Delta V_{C2}\\&-(2V_{DC}C_2\Delta V_{C2}-0.5C_2\Delta V_{C2}^2)\end{aligned} \tag{23}$$

During one cycle of fundamental voltage, the power loss in charging of capacitor C_2 is:

$$P_{C2,Loss}=\frac{\Delta E_{C2}}{T}=\frac{2}{T}(0.5C_2\Delta V_{C2}^2) \tag{24}$$

During discharging process of the capacitor, the energy loss occurring in it is equal to the difference of energy flowing out of the voltage source and the capacitor and that absorbed by the load. The discharging path for the state $\pm 2V_{DC}$ of capacitor C_1 is given in Figure 7(a) and (d), the energy loss occurring during this is given by,

$$\Delta E_{D1,2V_{DC}} = \left\{ 2V_{DC} \frac{2V_{DC}}{R_L + R_{eq}} - R_L \left(\frac{2V_{DC}}{R_L + R_{eq}} \right)^2 \right\} \times \frac{\pi - 2\alpha_4}{2\pi f} \tag{25}$$

where $R_{eq} = 5R_{SW}$ is the total parasitic resistance of semiconductor switch, f = output frequency and $R_{SWX} = R_{SWX'} = R_{SW}$ = on state resistance of semiconductor switch (X = 1 to 6 & X' = 1 to 5).

The total power loss occurring during one fundamental cycle of output voltage when output is $+2V_{DC}$ and $-2V_{DC}$ is given by,

$$P_{Loss,\pm 2V_{DC}} = \frac{2}{T} \left\{ 2V_{DC} \frac{2V_{DC}}{R_L + R_{eq}} - R_L \left(\frac{2V_{DC}}{R_L + R_{eq}} \right)^2 \right\} \times \frac{\pi - 2\alpha_4}{2\pi f} \tag{26}$$

The discharging path for the output voltage level $+1.5V_{DC}$ and the output voltage level $-1.5V_{DC}$ is illustrated in Figures 6 and 7(c), respectively. The energy loss occurring during discharging path for the state $+1.5V_{DC}$ of capacitor C_1 and $-1.5V_{DC}$ of capacitors C_1 and C_2 is given by,

$$\Delta E_{D,\pm 1.5V_{DC}} = \left\{ 1.5V_{DC} \frac{1.5V_{DC}}{R_L + R_{eq}} - R_L \left(\frac{1.5V_{DC}}{R_L + R_{eq}} \right)^2 \right\} \frac{\alpha_4 - \alpha_3}{2\pi f} \tag{27}$$

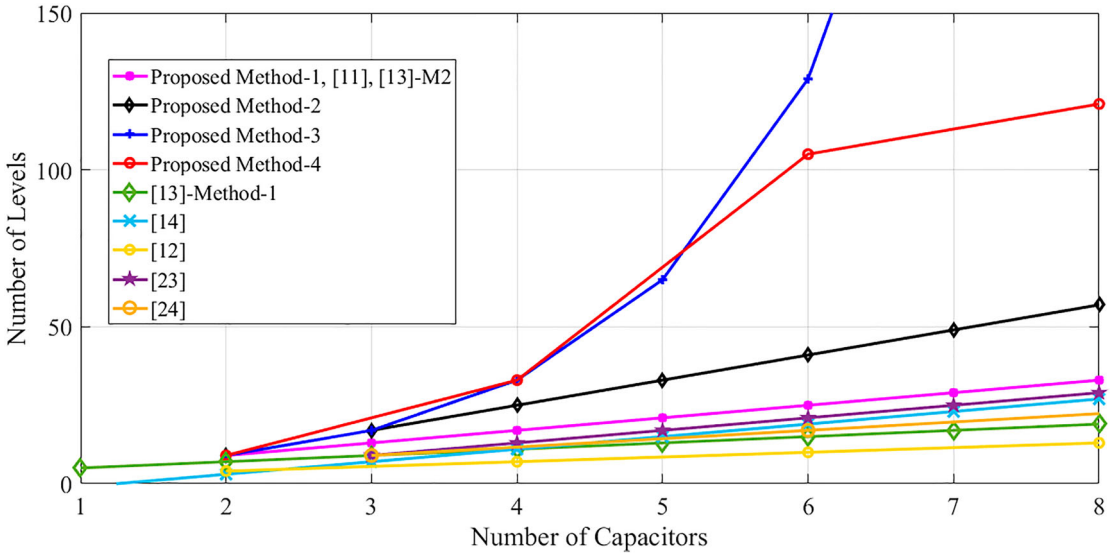

Figure 9. Comparison of the number of capacitors against the number of levels obtained.

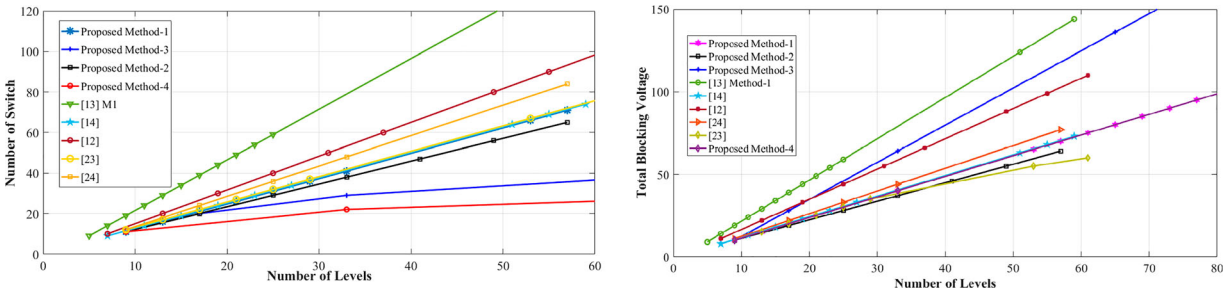

Figure 10. Comparison of the number of levels against (a) number of switches required (b) total blocking voltage.

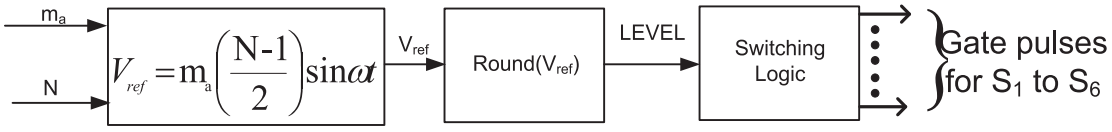

Figure 11. Nearest level control realization.

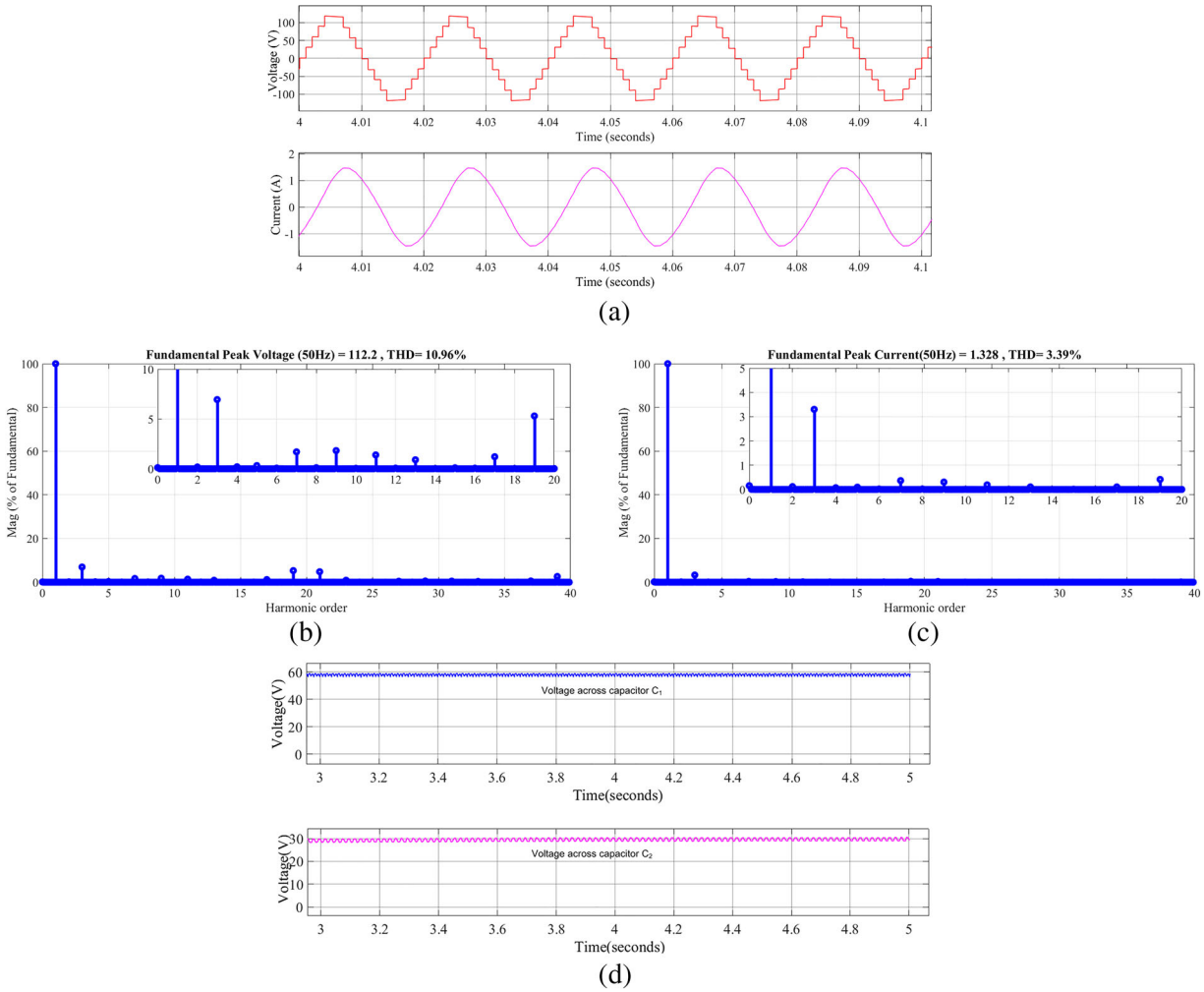

Figure 12. Simulation results with $R = 50\,\Omega, L = 120$ mH for $m_a = 1$: (a) Output voltage and current waveforms (b) FFT analysis of voltage waveform (c) FFT analysis of current waveform (d) Voltage across the capacitors C_1 and C_2.

Thus, the total power loss occurring during one fundamental cycle of output voltage when output is $+1.5V_{DC}$ and $-1.5V_{DC}$ is given by,

$$P_{Loss,\pm 1.5V_{DC}} = \frac{4}{T}\left\{1.5V_{DC}\frac{1.5V_{DC}}{R_L + R_{eq}} - R_L\left(\frac{1.5V_{DC}}{R_L + R_{eq}}\right)^2\right\}\frac{\alpha_4 - \alpha_3}{2\pi f} \quad (28)$$

The discharging path for the output voltage level $-0.5V_{DC}$ is illustrated in Figure 7(b). The energy loss occurring during discharging for the state $-0.5V_{DC}$ of capacitor C_2 is given by,

$$\Delta E_{D2} = \left\{0.5V_{DC}\frac{0.5V_{DC}}{R_L + R_{eq}} - R_L\left(\frac{0.5V_{DC}}{R_L + R_{eq}}\right)^2\right\}\frac{\alpha_2 - \alpha_1}{2\pi f} \quad (29)$$

The total power loss occurring during one fundamental cycle of output voltage when output is $-0.5V_{DC}$ is given by,

$$P_{Loss,-0.5V_{DC}} = \frac{2}{T}\left\{0.5V_{DC}\frac{0.5V_{DC}}{R_L + R_{eq}} - R_L\left(\frac{0.5V_{DC}}{R_L + R_{eq}}\right)^2\right\}\frac{\alpha_2 - \alpha_1}{2\pi f} \quad (30)$$

In addition to the above, there are losses in semiconductor switches in the load current path during output voltage level $+0.5V_{DC}$ and $\pm V_{DC}$ which is given by,

$$P_{Loss,+0.5V_{DC}} = \frac{2}{T}\left\{0.5V_{DC}\frac{0.5V_{DC}}{R_L + R_{eq}}\right.$$

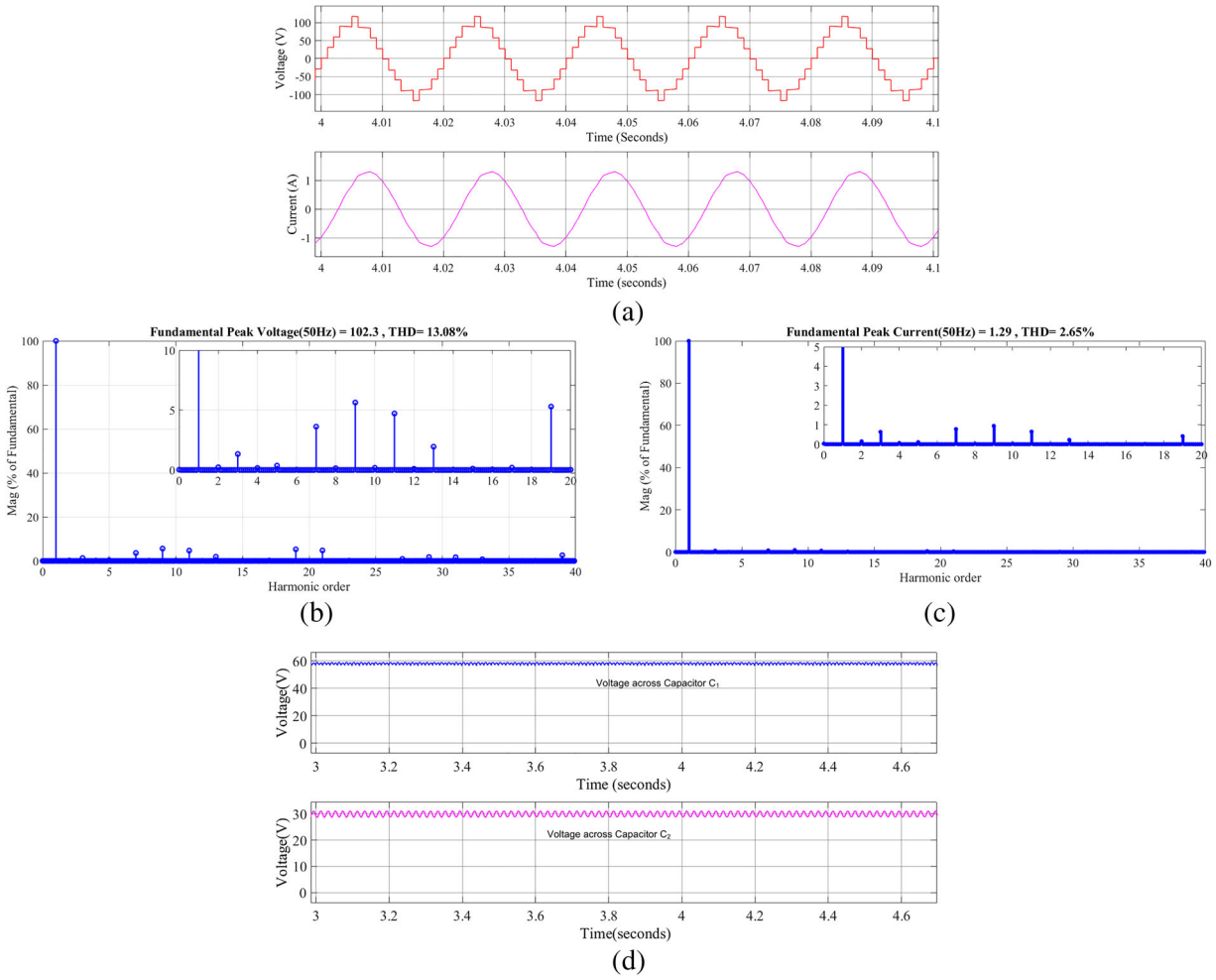

Figure 13. Simulation results with $R = 50\,\Omega$, $L = 120$ mH for $m_a = 0.9$: (a) Output voltage and current waveforms (b) FFT analysis of voltage waveform (c) FFT analysis of current waveform (d) Voltage across the capacitors C_1 and C_2.

$$-R_L\left(\frac{0.5V_{DC}}{R_L+R_{eq}}\right)^2\Bigg\}\frac{\alpha_2-\alpha_1}{2\pi f}$$

$$P_{Loss,\pm V_{DC}} = \frac{4}{T}\Bigg\{V_{DC}\frac{V_{DC}}{R_L+R_{eq}}$$

$$-R_L\left(\frac{V_{DC}}{R_L+R_{eq}}\right)^2\Bigg\}\frac{\alpha_3-\alpha_2}{2\pi f} \quad (31)$$

The total conduction loss is given by the sum of the above losses and is given by,

$$P_{Cond,Loss} = P_{C1,Loss} + P_{C2,Loss} + P_{Loss,\pm 2V_{DC}} + P_{Loss,\pm 1.5V_{DC}} + P_{Loss,\pm V_{DC}} + P_{Loss,+0.5V_{DC}} + P_{Loss,-0.5V_{DC}} \quad (32)$$

The total losses and efficiency of the converter is given by,

$$P_{Total\ Loss} = P_{SW,Total\ loss} + P_{Cond,\ Loss} \quad (33)$$

$$\eta = \frac{P_{output}}{P_{output} + P_{Total\ Loss}} \quad (34)$$

Based on the above equations, the efficiency is calculated for various output power ratings by considering the load to be pure resistive load. The graph plotted between the output power and efficiency is shown in Figure 8.

6. Comparative evaluation of proposed boosting MLI

To study the potential advantages (improvement) provided by the proposed topology, it has been compared with other topologies presented in the recent past. In the literature, the performance parameters used for assessing the multilevel inverter include the number of switches (N_{SW}), number of capacitors (N_C), number of diodes (N_D), maximum voltage obtained (V_{peak}) and total blocking voltage (TBV).

The above-said parameters have a direct impact on the size, initial cost, reliability, losses and efficiency of the inverter. The size, number of levels, number of switches, total blocking voltage and maximum voltage obtained in a case of the switched capacitor based multilevel inverter topology depends on the number of switched capacitors used in a particular topology.

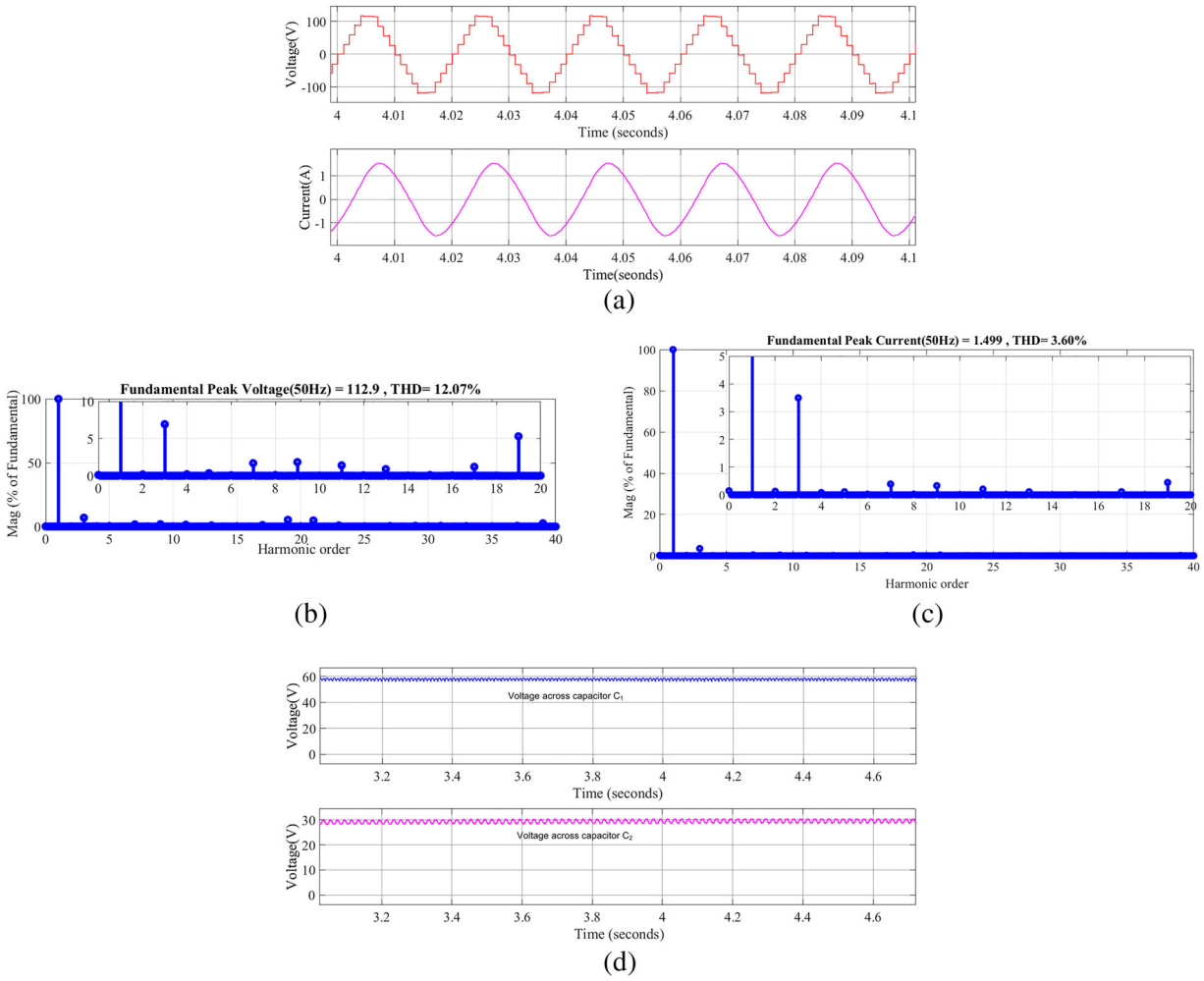

Figure 14. Simulation results with $R = 50\,\Omega$, $L = 90$ mH for $m_a = 1$: (a) Output voltage and current waveforms (b) FFT analysis of voltage waveform (c) FFT analysis of current waveform (d) Voltage across the capacitors C_1 and C_2.

Hence, a comprehensive comparison of number levels obtained, number of switches required, total blocking voltage and maximum voltage obtained for the proposed hybrid multilevel inverter with different existing topologies for a given number of switched capacitor units is provided in Table 2.

As illustrated in Figure 9, the proposed extension method-3 produces more number of levels compared to other extension methods and other existing topologies for a given number of switched capacitors. As demonstrated in Figure 10(a), the proposed inverter with extension method-4 has a high level-to-switch ratio (LSR); thus it can generate more number of levels with a reduced number of switches with multiple sources. Also, among the single source topologies [20] M1, [13] and proposed extension method-1, LSR for the proposed inverter with extension method-1 is very competitive and compared to [13], it is able to realize more number of levels for a given number of capacitors. To realize higher levels for a given number of levels, the total blocking voltage requirement of the proposed topology with extension method-2 is low compared to the other topologies as demonstrated in Figure 10(b). Thus, the proposed hybrid topology is better than the existing topologies – to realize higher levels with less number of switches and total blocking voltage for a given number of switched capacitors.

7. Pulse width modulation

Many pulse width modulation techniques are presented for multilevel inverters in the literature [6]. The modulation techniques are broadly categorized into low switching frequency and high switching frequency techniques based on the switching frequency. To study the operation and performance of the proposed inverter, the nearest level control (NLC) based modulation technique has been used [23,24]. The nearest level control falls under the category of low switching frequency type in which switching frequency is equal to the fundamental output frequency. In this method, a sinusoidal reference voltage whose peak amplitude equals to the maximum voltage level that can be generated by an inverter is sampled at the desired frequency. Each sampled voltage is converted to the nearest voltage level which can be realized by the multilevel inverter using the round function. With the help

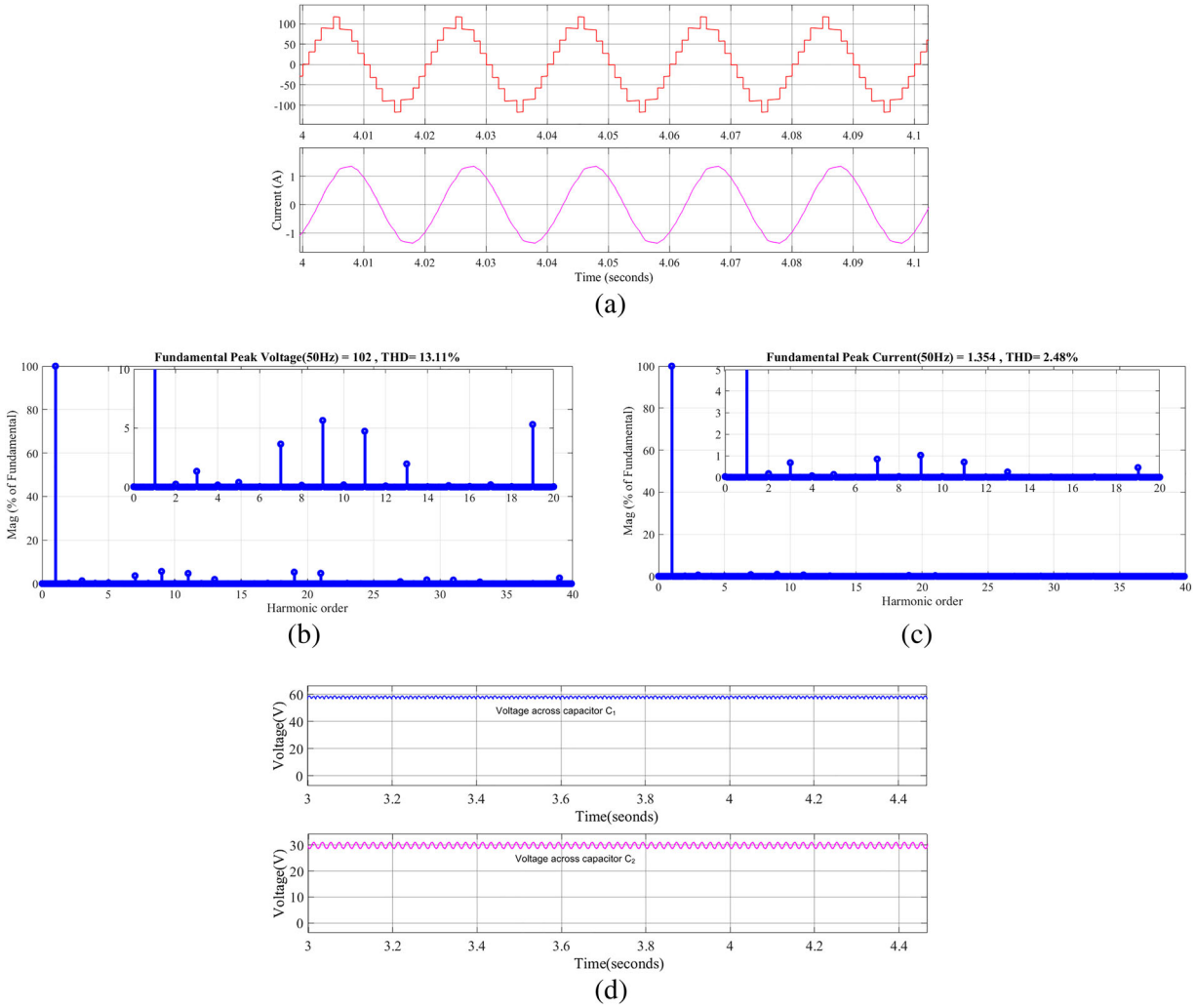

Figure 15. Simulation results with $R = 50\,\Omega$, $L = 90$ mH for $m_a = 0.9$: (a) Output voltage and current waveforms (b) FFT analysis of voltage waveform (c) FFT analysis of current waveform (d) Voltage across the capacitors C_1 and C_2.

of switching logic, desired switches to realize a particular level are turned ON. Suppose the level information obtained is L_1^+, L_2^+ , $L_3^+$and L_4^+ for $0.5V_{DC}$ to $2V_{DC,}$ respectively, and L_0, L_1^-, L_2^- , $L_3^-$and L_4^- for 0 to $-2V_{DC}$, then the gate signal for switch S_1 is given by the following expression:

$$S_1 = L_1^+ + L_2^+ + L_3^+ + L_4^+ + L_0 + L_1^- + L_2^- \qquad (35)$$

In the above expression, "+" indicates the logical OR operation, in the same manner using the switching state given in Table 1, switching expression can be derived for other switches. Alternatively, the switching logic can also be employed using a switch function available in the math library of the C-program. The equation governing the nearest level control is given by (36) and (37). The block diagram to realize the nearest level control is given in Figure 11.

$$V_{\text{ref}} = m_a \left(\frac{N-1}{2}\right) \sin \omega t \qquad (36)$$

where m_a = amplitude modulation index and N = number of levels in the inverter

$$\text{Level} = \text{round}(V_{\text{ref}}) \qquad (37)$$

Table 3. Details of the hardware prototype built.

Parameters	Values
Input DC bus voltage	60 V
Capacitor rating	$C_1 = 1600\,\mu$F/100 V and $C_2 = 1600\,\mu$F/100 V
Load details	$R = 50\,\Omega$ and $L = 120$ mH, 90 mH
Output frequency	50 Hz
Switches S_1 to S_6 and $S_{1'}$ to $S_{5'}$	IRFP460
Diode	MUR460
Driver IC	IR2111

The nearest level control is implemented in a low cost microcontroller ARDUINO and the switching pulse for each switch is obtained from the output ports of the microcontroller.

8. Simulation and experiment results

The suggested topology has been initially studied with the help of simulation using MATLAB-SIMULINK. The input voltage to the inverter is set to 60 V, the values of capacitance C_1 and C_2 is set to 1600μF and the load is series-connected RL-load. The output voltage and current waveform along with their FFT analysis for

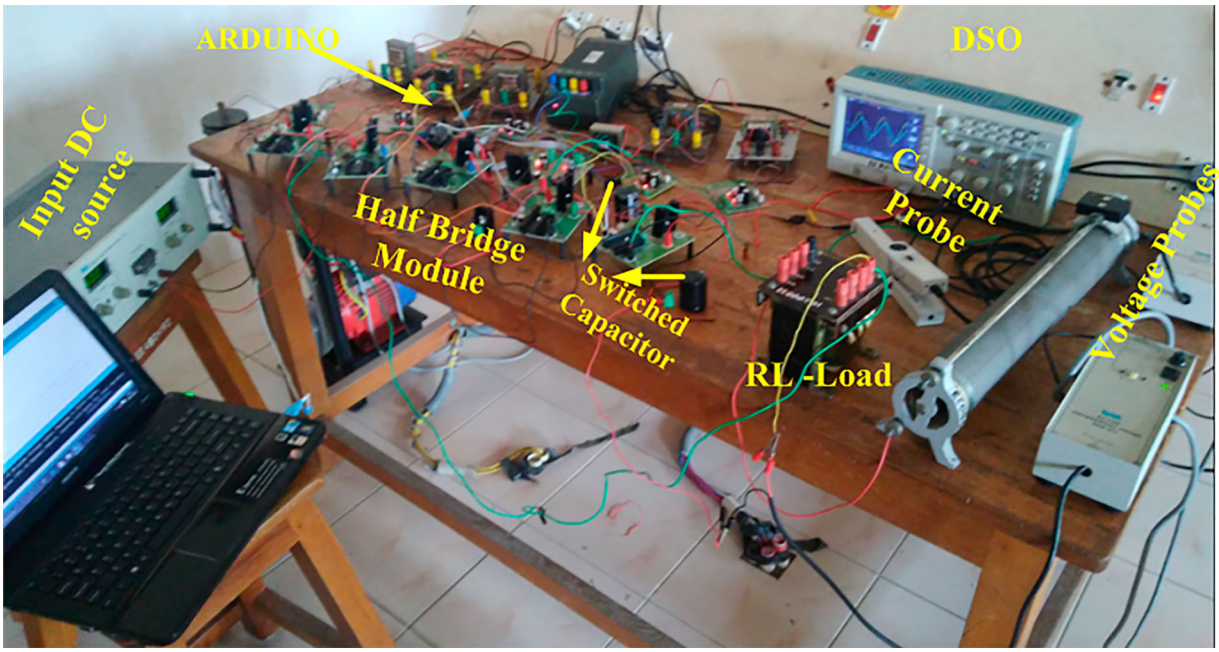

Figure 16. Hardware prototype fabricated in the laboratory.

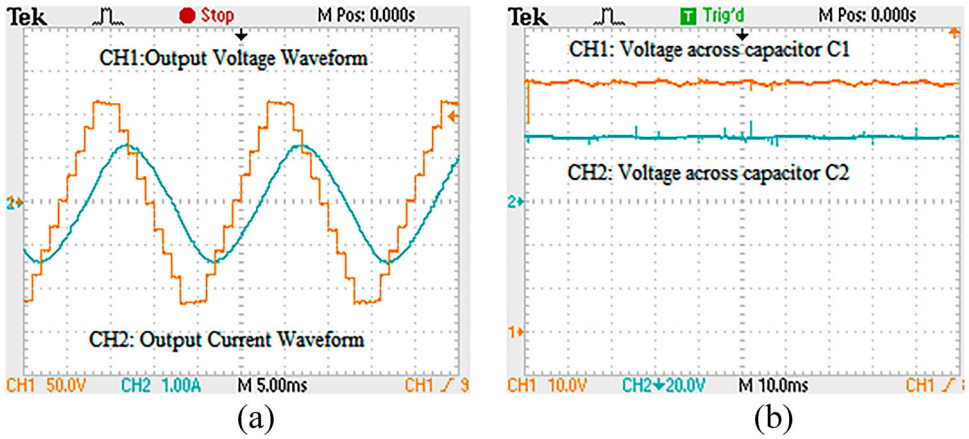

Figure 17. Prototype results with $R = 50\,\Omega$, $L = 120$ mH for $m_a = 1$: (a) Output voltage and current waveforms (CH1: 5 ms/div, 50 V/div and CH2: 5 ms/div, 1 A/div), (b) Voltage across the capacitors C_1 and C_2 (CH1: 10 ms/div, 10 V/div and CH2: 10 ms/div, 20 V/div).

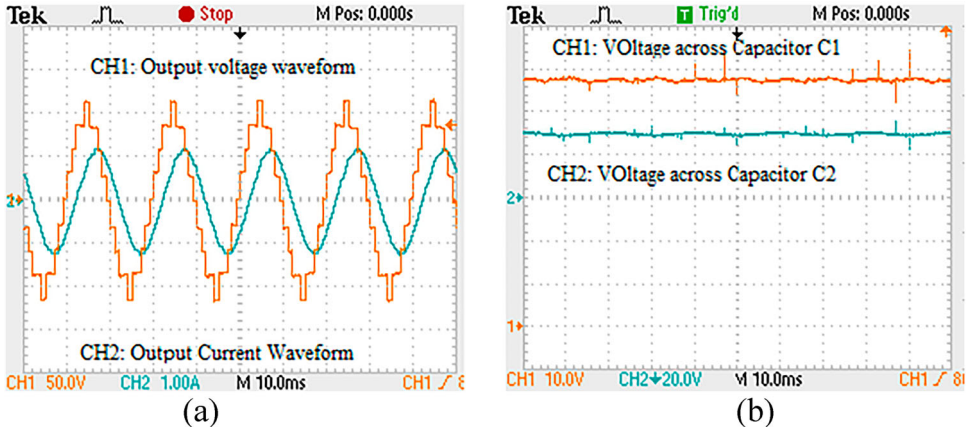

Figure 18. Prototype results with $R = 50\,\Omega$, $L = 120$ mH for $m_a = 0.9$: (a) Output voltage and current waveforms (CH1: 10 ms/div, 50 V/div and CH2: 10 ms/div, 1 A/div), (b) Voltage across the capacitors C_1 and C_2 (CH1: 10 ms/div, 10 V/div and CH2: 10 ms/div, 20 V/div).

a modulation index of 1 with RL-load, $R = 50\,\Omega$ and $L = 120$ mH, is shown in Figure 12.

The simulation is repeated for a modulation index of 0.9 and the corresponding waveforms obtained are illustrated in Figure 13.

Furthermore, the simulation has been also performed by varying the load from $R = 50\,\Omega$ and $L = 120$ mH to $R = 50\,\Omega$ and $L = 90$ mH. The results obtained are revealed in Figures 14 and 15 for a modulation index of 1 and 0.9, respectively.

To further validate the feasibility of the proposed multilevel inverter, a laboratory scale prototype is fabricated. The input voltage and capacitance values used in the hardware prototype are the same as those used in the simulation. Other specifications of the prototype built in the laboratory are given in Table 3 and the details of the experimental set up are given in Figure 16.

The gate pulses obtained from input-output ports of the microcontroller are isolated using an optocoupler

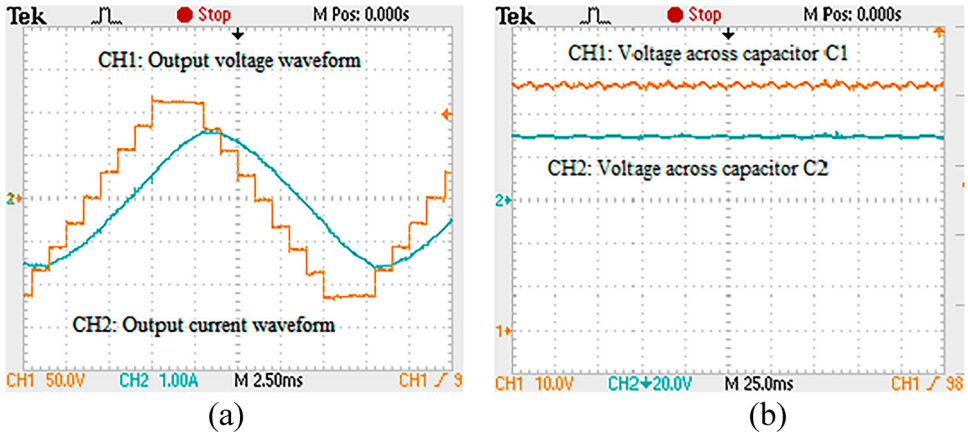

Figure 19. Prototype results with $R = 50\,\Omega$, $L = 90$ mH for $m_a = 1$: (a) Output voltage and current waveforms (CH1: 2.5 ms/div, 50 V/div and CH2: 2.5 ms/div, 1 A/div), (b) Voltage across the capacitors C_1 and C_2 (CH1: 25 ms/div, 10 V/div and CH2: 25 ms/div, 20 V/div).

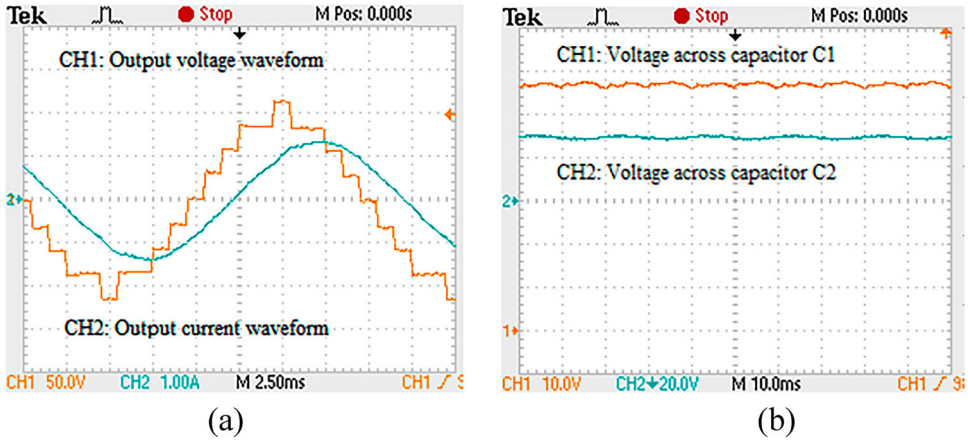

Figure 20. Prototype results with $R = 50\,\Omega$, $L = 90$ mH for $m_a = 0.9$: (a)Output voltage and current waveforms (CH1: 2.5 ms/div, 50 V/div and CH2: 2.5 ms/div, 1 A/div), (b) Voltage across the capacitors C_1 and C_2 (CH1: 10 ms/div, 10 V/div and CH2: 10 ms/div, 20 V/div).

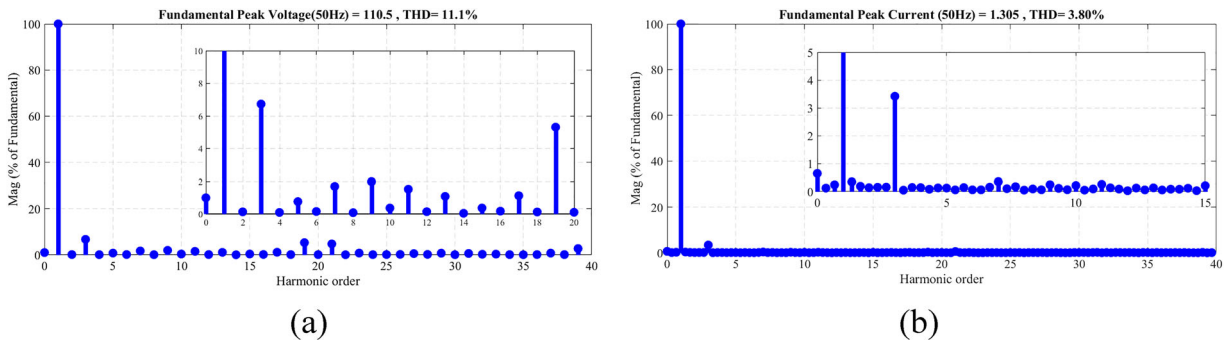

Figure 21. Harmonic spectrum obtained from a prototype built with $R = 50\,\Omega$, $L = 120$ mH for $m_a = 1$:(a) FFT analysis of voltage waveform (b) FFT analysis of current waveform.

and given to the driver IC IR2111. The IR2111 has the capability to generate a complimentary pulse output with a dead band. Thus, the microcontroller generates only six pulses. The dead band offered by IR2111 between the upper and lower switch gate pulses is 800 ns. The output voltage, current and capacitor voltage waveforms are acquired from hardware prototypes developed in the laboratory for various modulation indexes and various loading conditions to validate the performance of the proposed hybrid multilevel inverter. The voltage, current waveforms and capacitor voltages obtained with a load of $R = 50\,\Omega$ and $L = 120$ mH, for modulation indexes of 1 and 0.9 are shown in Figures 17 and 18, respectively. The waveforms of voltage, current and capacitor voltages with another load of $R = 50\,\Omega$ and $L = 90$ mH with modulation indexes of 1 and 0.9 are provided in Figures 19 and 20, respectively.

With the help of MATLAB-SIMULINK, the harmonic spectrum of the output voltage waveform and current waveform has been plotted using data acquired from recorded waveforms. The harmonic spectrum from the prototype built with $R = 50\,\Omega$ and $L = 120$ mH for a modulation index of 1 and 0.9 are depicted in Figures 21 and 22 respectively, whereas Figures 23 and 24 illustrate the harmonic spectrum of output voltage and current waveform with $R = 50\,\Omega$ and $L = 90$ mH for a modulation index of 1 and 0.9, respectively. Also, the total harmonic distortion (THD) of the output voltage waveform and current waveform has been determined by the data acquired from recorded waveforms with the help of MATLAB and it is found to be 11.1% and 3.8%, respectively, for a modulation index of 1. The switching angles, which are defined by the modulation index, affect the THD of the output voltage. The THD of the current waveform is marginally improved at 0.9 modulation index on account of reduction in lower order harmonics compared to unity modulation index.

From the output voltage waveforms, the 9-levels obtained from an inverter can be validated. The steady state voltage across the capacitors C_1 and C_2 for various modulation indexes and loading conditions shown in prototype results prove the self regulation of voltage across the switched capacitor with the help of modulation alone. The voltage across the capacitors C_1 and C_2 is regulated around 60 and 30 V, respectively, with allowable ripple for an input voltage of 60 V.

The voltage stabilization of switched capacitors C_1 and C_2 to their steady state values under a dynamic condition when the DC input voltage to the inverter is switched ON is illustrated in Figure 25, which demonstrates the effectiveness of sensor less voltage control. The maximum voltage across the load is 120 V for an input of 60 V, which confirms the voltage gain of the topology to be 2. Table 4 compares the performance of the hardware prototype with simulation findings, demonstrating that the hardware and simulation results are in agreement. The current THD obtained is lesser than 5% without any external additional filter. The efficiency of the inverter is obtained by measuring the input and output powers of the inverter. The efficiency

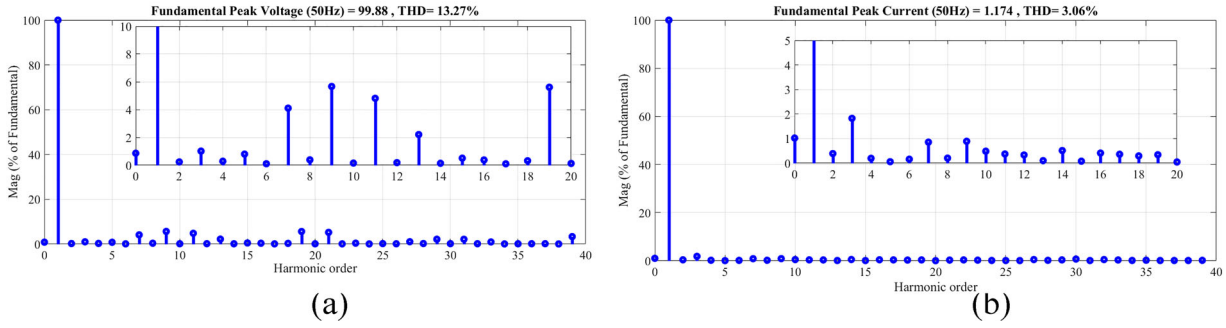

Figure 22. Harmonic spectrum obtained from a prototype built with $R = 50\,\Omega, L = 120$ mH for $m_a = 0.9$:(a) FFT analysis of voltage waveform (b) FFT analysis of current waveform.

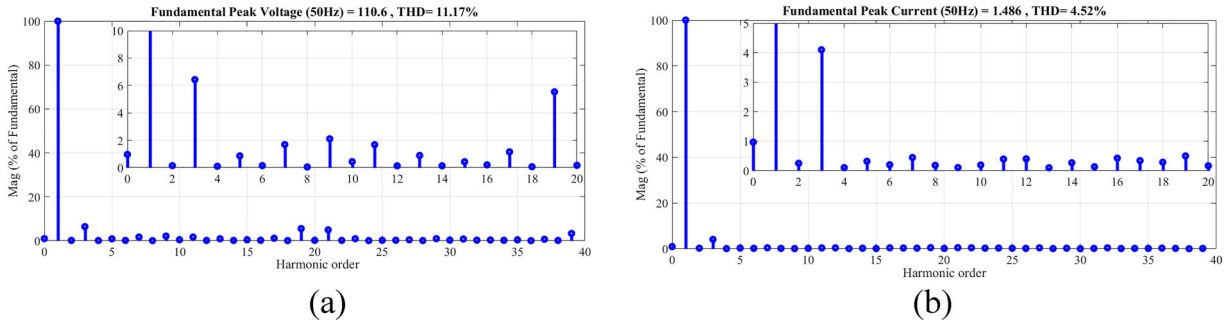

Figure 23. Harmonic spectrum obtained from a prototype built with $R = 50\,\Omega, L = 90$ mH for $m_a = 1$:(a) FFT analysis of voltage waveform (b) FFT analysis of current waveform.

Table 4. Comparison of the simulation and hardware prototype results.

		Load with $R = 50\,\Omega$ and $L = 120$ mH		Load with $R = 50\,\Omega$ and $L = 90$ mH	
Modulation index	Performance indices	Simulation result	Experimental result	Simulation result	Experimental result
1	Peak fundamental output voltage (V)	112.2	110.5	112.9	110.6
	% THD of output voltage	10.96	11.1	12.07	11.17
	% THD of output current	3.39	3.8	3.60	4.52
0.9	Peak fundamental output voltage (V)	102.3	99.88	102	99.76
	% THD of output voltage	13.08	13.27	13.11	13.3
	% THD of output current	2.65	3.06	2.48	3.16

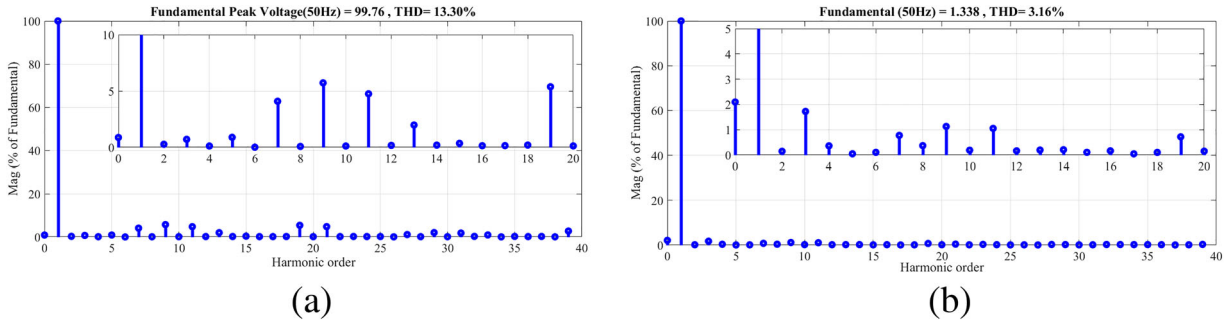

Figure 24. Harmonic spectrum obtained from a prototype built with $R = 50\,\Omega$, $L = 90$ mH for $m_a = 0.9$:(a) FFT analysis of voltage waveform (b) FFT analysis of current waveform.

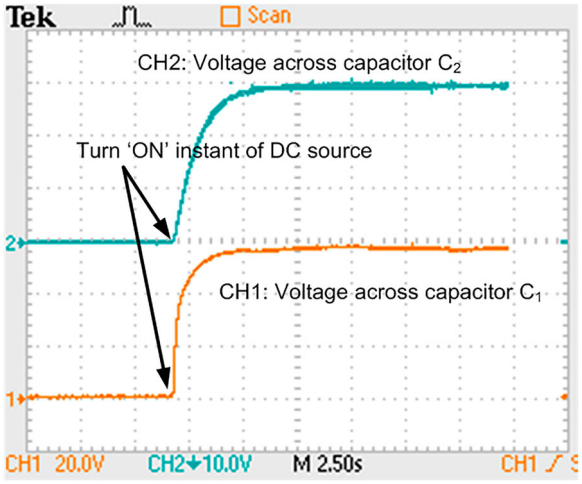

Figure 25. Transient response of voltage across capacitors C_1 and C_2 during turning ON DC source with $R = 50\,\Omega$ $L = 120$ mH for $m_a = 1$ (CH1: 2.5 s/div, 20 V/div and CH2: 2.5 s/div, 10 V/div).

of the prototype with $R = 50\,\Omega$ and $L = 90$ mH is 95.85% and 95.24% for modulation index of 1 and 0.9, respectively, whereas for $R = 50\,\Omega$ and $L = 120$ mH, the efficiency is 95.78% and 95.19% for modulation index of 1 and 0.9, respectively.

9. Conclusion

A hybrid multilevel inverter with boosting capability is suggested in this study, and its basic module can generate nine voltage levels across the load. The key features of the recommended basic module are: 1) It require a single DC source 2) It has a voltage gain of two 3) Voltage across the switched capacitors are self-balanced without any additional control 4) Each switch's blocking voltage requirement is either equal to or half the supply voltage. The proposed topology is easily extendable for a higher number of voltage levels with required boosting by cascading a suitable number of boosting modules with a reduced number of capacitors and switches. Also, by cascade connection of fundamental modules, it is possible to integrate multiple sources.

A detailed theoretical loss analysis is performed and maximum theoretical efficiency is found to be 98.9%. An exhaustive comparison study between the proposed topology against other recently proposed topologies is done to assess its benefits. The gate pulses required for the switches are generated using a low-cost microcontroller. The operation of the suggested multilevel inverter has been validated by a simulation study and experimental results, under different loading conditions and modulation indices. The power quality obtained from the presented topology is illustrated with the help of total harmonic distortion and a harmonic spectrum obtained from the hardware. Thus, the inverter's performance demonstrates its capability for single stage DC–AC conversion which can be utilized with solar PV battery energy storage for feeding AC loads.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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Appendix

The different operating modes of the proposed hybrid multilevel inverter and its current path for resistive load and inductive load is shown in Figure A1(a)–(i).

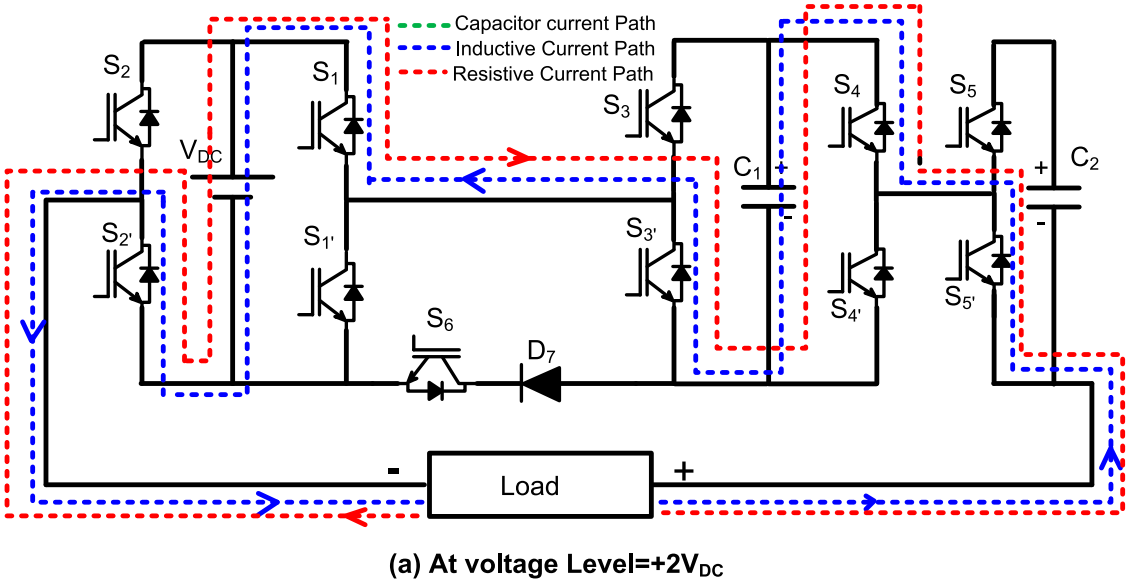
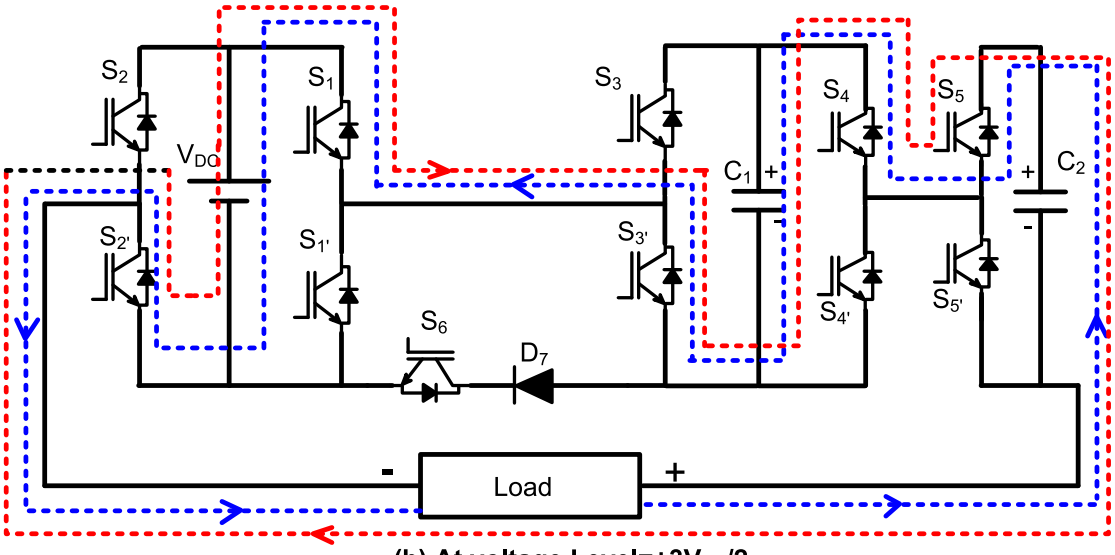
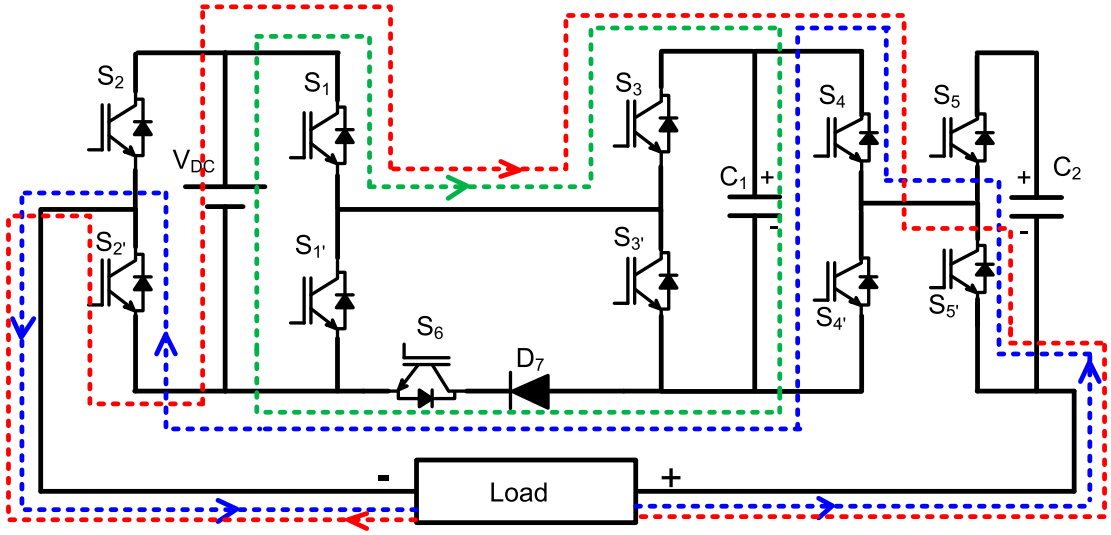


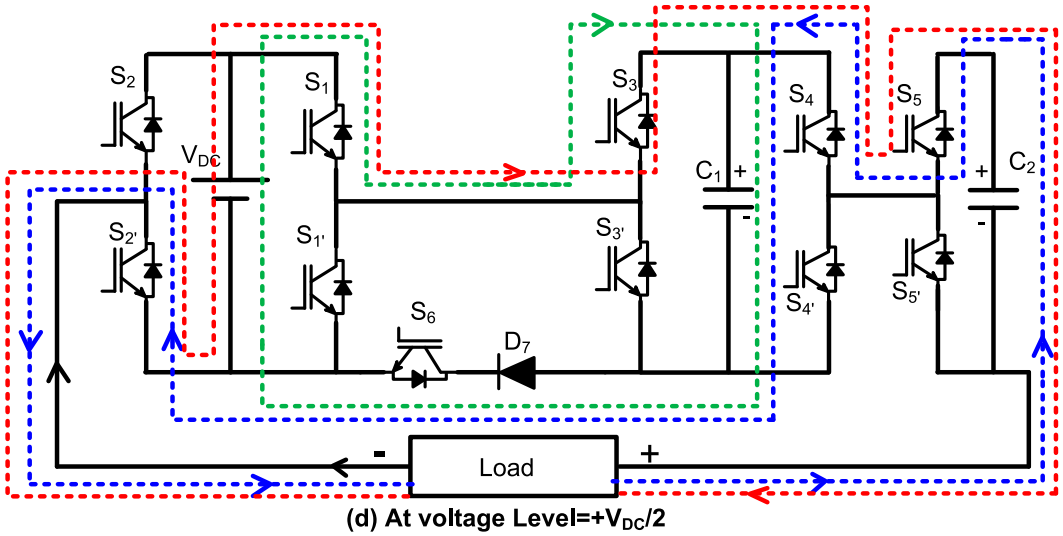
Figure A1. Figure A1. Different operating modes of proposed hybrid 9-Level Inverter (a)–(d) Positive output voltage levels, (e) Zero voltage level (f)–(i) Negative output voltage levels.



(b) At voltage Level=+3V_{DC}/2

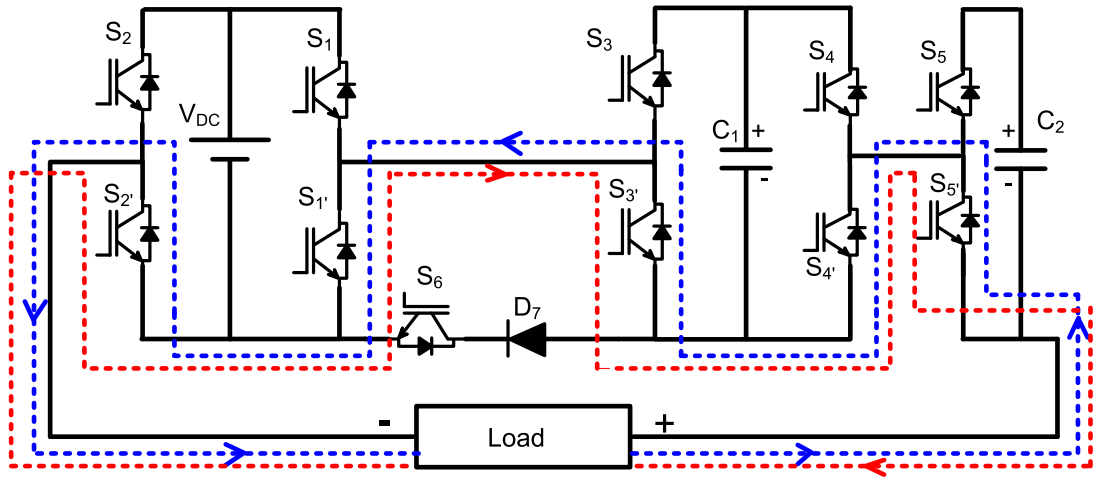


(c) At voltage Level=+V_{DC}

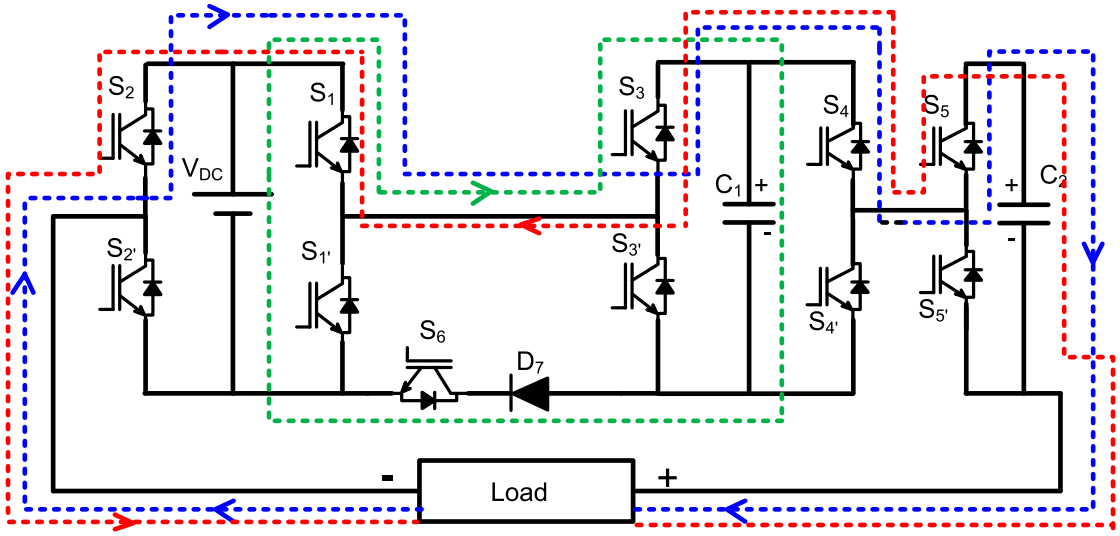


(d) At voltage Level=+V_{DC}/2

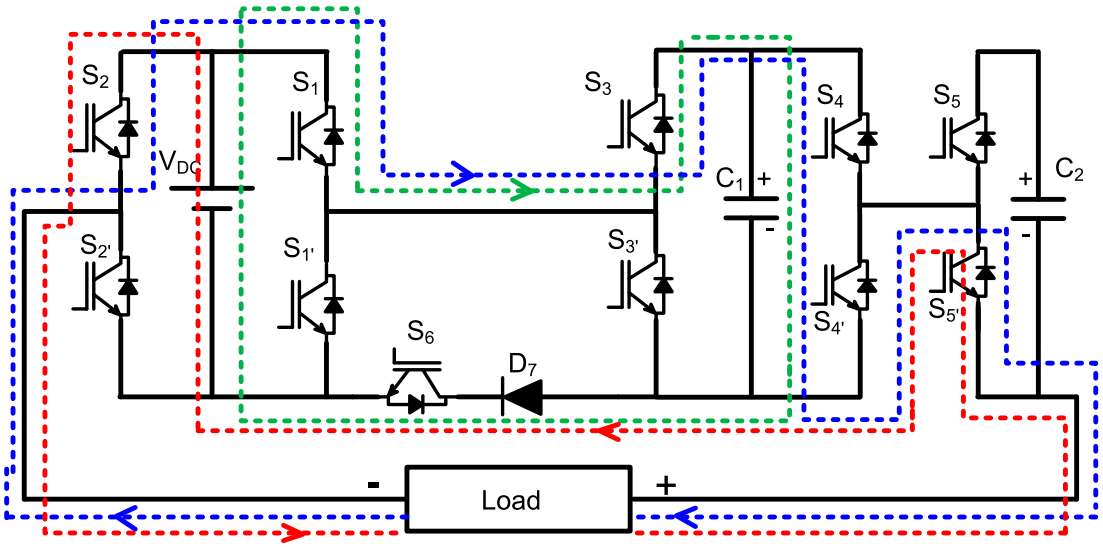
Figure A1. *Continued*



(e) At voltage Level=0

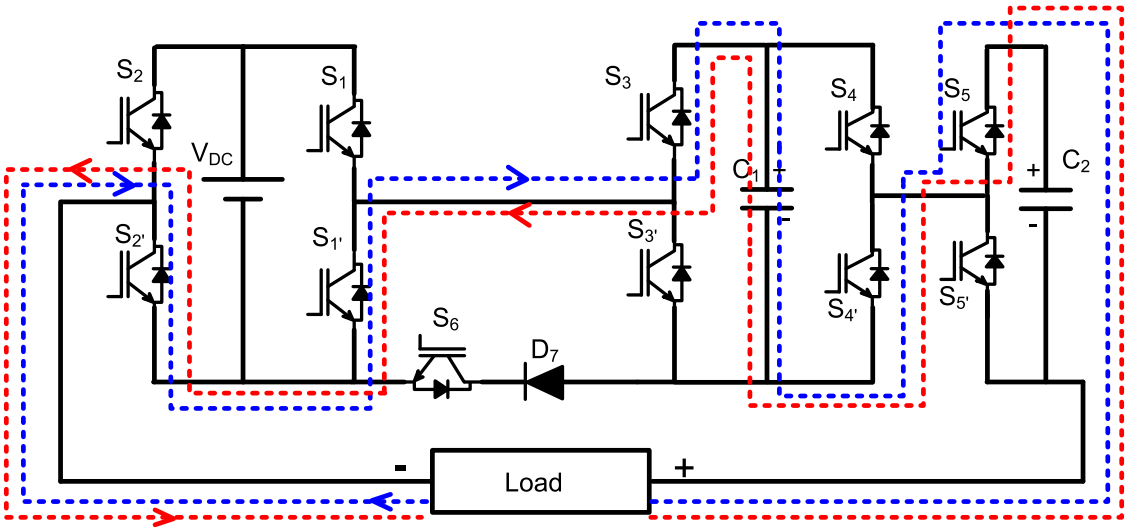


(f) At voltage Level=-$V_{DC}/2$

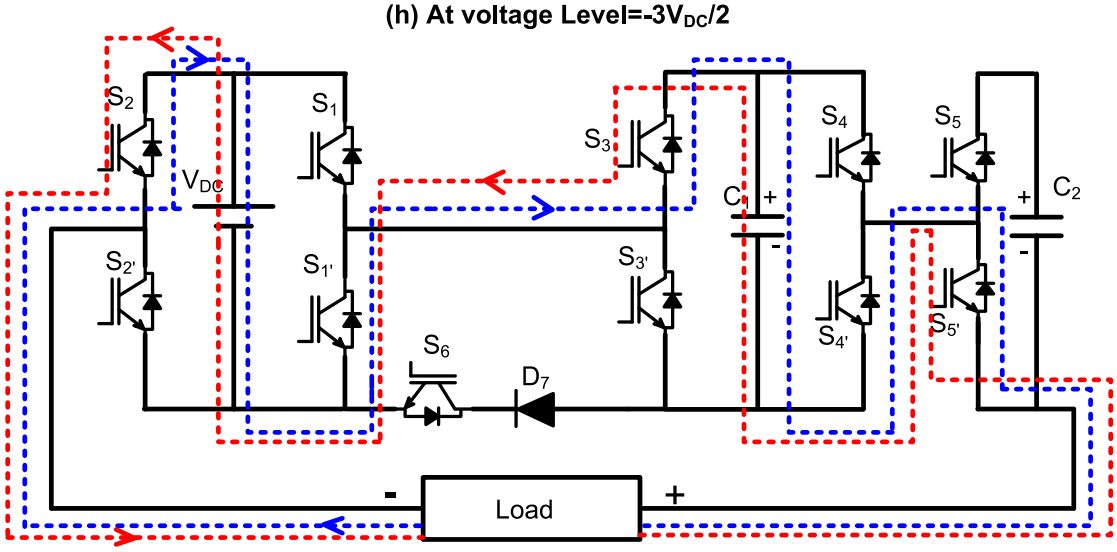


(g) At voltage Level=-V_{DC}

Figure A1. *Continued*



(h) At voltage Level=-3V_{DC}/2



(i) At voltage Level=-2V_{DC}

Figure A1. *Continued*