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USPOREDBA MIKROPROCESORSKIH ALATA U MEHATRONIČKIM RJEŠENJIMA NA PRIMJERU AKTIVNOGA UČINSKOG FILTRA
COMPARISON OF MICROPROCESSOR TOOLS FOR MECHATRONIC SOLUTIONS ON ACTIVE POWER FILTER EXAMPLE

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Sažetak: *Posljednjih godina pojavljuju se mehatronička rješenja podjednako u znanstvenim člancima i gotovim proizvodima. Inženjeri elektrotehnike i strojarstva u potrazi za optmalnim rješenjima pokušavaju optimirati strojeve s unutarnjim izgaranjem, hibridne strojeve, te se također na drugačiji način pristupa problemu kompenzacije vibracija i njegovom elektrotehničkom ekvivalentu kompenzaciji faktora snage. U ovom članku opisan je problem kompenzacije faktora snage koji je riješen algoritmom kliznog upravljanja na različitim mikroprocesorskim sustavima. Oba su mikroprocesorska sustava izgrađena na podlozi mikroprocesora iz iste skupine, proizvođača Texas Instruments (TMSLF24xx). U prvom je slučaju riječ o sustavu s razvijenim korisničkim sučeljem (Matlab/Simulink) dok je u drugom slučaju upotrijebljeno sučelje namijenjeno programiranju u asembleru ili C-u. Oba su rješenja uspoređena te su analizirane njihove prednosti i nedostaci.*

Ključne riječi: - mehatronika
- mikroprocesorski sustavi
- klizni način rada
- aktivni učinski filtar
- TMS320LF240x

Summary: *In recent years, many new mechatronic projects have been appearing both in scientific papers and on the market. Electrical and mechanical engineers are searching for an optimal solution for different mechatronic problems including the optimization of combustion engines, hybrid vehicles, compensation of vibration or its electrical counterpart, power factor correction. In this article, the problem of active power factor compensation is solved with two different microprocessor platforms: both are based on the same family of Texas Instruments microprocessors (TMS240LF24xx). The first one is upgraded with the user friendly Matlab/Simulink interface, and the second with TI Code Composer, low language (assembler, C) interface. In this paper, the advantages and disadvantages of both of these solutions are analyzed in terms of the active power filter (APF) example.*

Key words: - mechatronics
- microprocessor systems
- sliding-mode control
- active power filter
- TMS320LF240

1. UVOD

Programiranje mikroprocesorskih sustava uporabom jezika niske razine koristi se za vrlo zahtjevne primjene kao što je vektorsko upravljanje asinkronih strojeva. U takvim je slučajevima potrebno transformirati osi stroja u realnom vremenu. Računalni jezici (ili točnije sučelja) više razine kao što je primjerice Matlab/Simulink ili slična sučelja koja se koriste za programiranje mikroprocesorskih sustava u programabilnim logičkim kontrolerima (PLC-ima) znatno su jednostavniji za upotrebu, ali ograničavaju frekvenciju do koje ih je moguće koristiti.

1. INTRODUCTION

Low-level language tools for microprocessor programming have been used for very demanding applications as the vector control of induction machines where axes transformation of the machine must be done in real time. High language tools such as the Simulink compiler for microprocessor systems or similar user-friendly platforms which have been used in programmable logic controllers (PLCs) are much easier to handle, but radically limit speed of the microprocessor system and therefore limit usage to slower applications.

To ih čini idealnima za automatizaciju industrijskih (proizvodnih) pogona, programiranje liftova u zgradama i slično. Aktivna kompenzacija vibracija i njezin elektrotehnički ekvivalent – aktivna kompenzacija faktora snage mogu se klasificirati kao srednje do visoko zahtjevne aplikacije. U njihovu slučaju potrebno je koristiti frekvenciju od barem 10 kHz [1], [2], a najbolji rezultati postižu se na višim frekvencijama od 15 kHz do 25 kHz (kompromis između izobličenja signala i djelotvornosti).

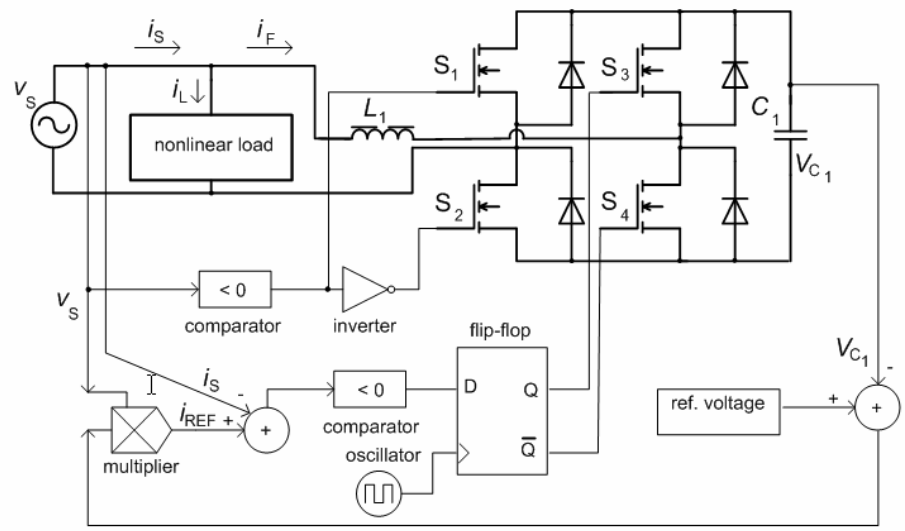
2.JEDNOFAZNI AKTIVNI UČINSKI FILTAR

Jednofazni aktivni učinski filtar (APF) sastoji se od prigušnice, kondenzatora i sklopki [1], [2]. Moguće ga je upravljati programabilnom logikom ili mikroprocesorskim sustavom. Slika 1 prikazuje klasični jednofazni mosni aktivni učinski filtar.

This makes them ideal for demanding applications such as the automation of industrial production, solving elevator logic in large buildings, etc. Vibration compensation and its electrical counterpart – active power filtering – can be classified as middle or middle to high demanding applications. It demands at least 10 kHz [1], [2] switching frequency but the best results (a compromise between distortion and efficiency) are achieved at higher frequencies of between 15 kHz and 25 kHz.

2. SINGLE PHASE ACTIVE POWER FILTER

The single phase active power filter (APF) consists of an inductor, capacitor and four switches [1], [2]. It can be controlled by a logic circuit or a microprocessor system. Figure 1 shows a standard H-bridge single phase active power filter.



Slika 1. Aktivni učinski filtar u kliznom načinu rada [1], [2], [10]
Figure 1. Active power filter with sliding mode control algorithm [1], [2], [10]

Pojedine sklopke filtra označene su oznakom S i indeksima od 1 do 4. U ovisnosti o tome u kojem smjeru teče struja (vodi li struju dioda ili tranzistor unutar sklopke) kondenzator C_1 se puni ili prazni. To znači da pretvarač može slati energiju dvosmjerno što je preduvjet za kompenzaciju faktora snage. Sklopke S_1 i S_2 sklapaju na mrežnoj frekvenciji (50 Hz) a sklopke S_3 i S_4 na frekvenciji sklapanja (10 - 25 kHz) [5], [6], [7], [8].

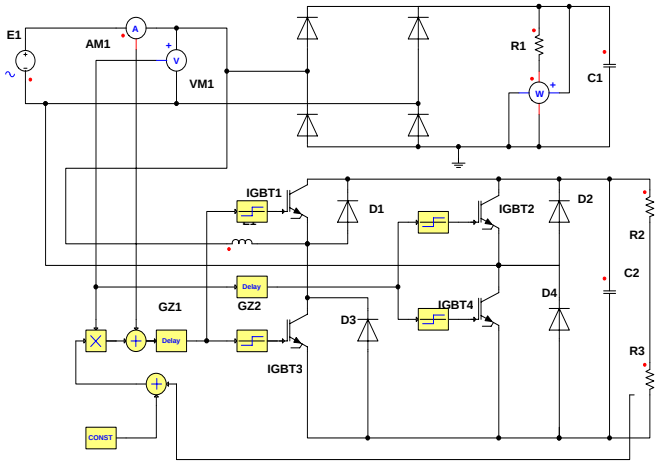
2. REZULTATI SIMULACIJE

Simulacija aktivnoga učinskog filtra može biti izvedena pomoću različitih simulacijskih alata uključujući Matlab/Simulink, Simplorer ili kombinaciju spomenutih programa. Ovdje je odabran program Simplorer zbog svoje jednostavnosti i transparentnosti (Slika 2).

Diodes of each switch noted with S_1...S_4 enable the charging of the capacitor C_1 and anti - parallel transistors enable C_1 discharging. That means that this converter is capable of bidirectional energy flow in order to compensate nonlinear load current and to invert energy stored in the capacitor C_1. Switches S_1 and S_2 switch on network frequency (50 Hz) and switches S_3 and S_4 on switching frequency (10 - 25 kHz) [5], [6], [7], [8].

2. SIMULATION RESULTS

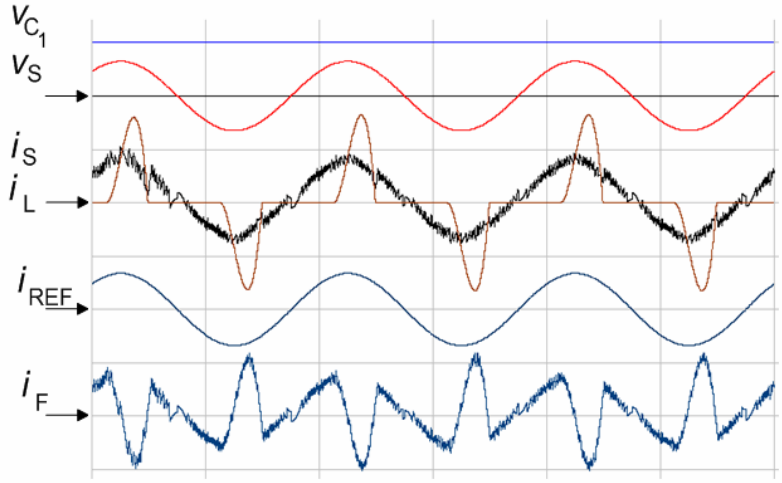
Simulation of an active power filter can be done in different simulation programs including Matlab/Simulink, Simplorer or a combination of these two programs. Here, a simulation in Simplorer was chosen because of its simplicity (Fig. 2).



Slika 2. Simulacijska shema aktivnoga učinskog filtra i njegovih komponenti– Simplorer
Figure 2. Simulation of active power filter and its components – Simplorer

Slika 3 prikazuje odnose stacionarnih struja i napona u aktivnom učinskom filtru tijekom ustaljenog stanja. Može se uočiti da je struja i_S izvora bliska sinusnoj unatoč činjenici da je struja trošila i_L izrazito impulsnoga karaktera.

In Figure 3, the simulated results for the active power filter during stationary operating conditions are shown. It can be noted that the source current is close to the sinus function in spite of the impulsive nature of the load current.



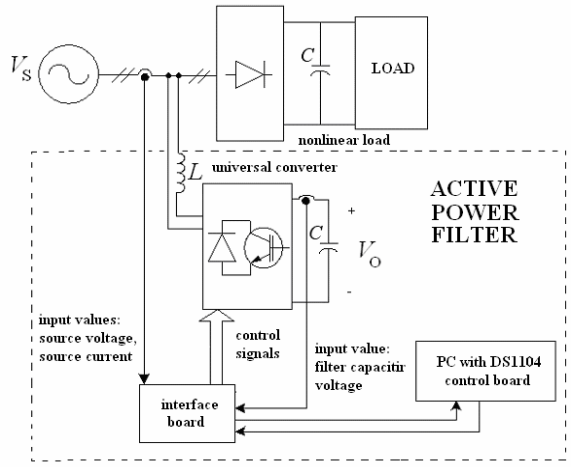
Slika 3. Valni oblici APF-a: napon filterskoga kondenzatora (v_{C1}), napon izvora/napajanja (v_S), struja trošila (i_L), referentna struja (i_{REF}), struja filtra (i_F), k_i = 12,5 A/div k_v = 500 V/div k_t = 10 ms/div
Figure 3. Waveforms in APF: filter capacitor voltage (v_{C1}), supply voltage (v_S), load current (i_L), supply current (i_S), reference supply current (i_{REF}), filter current (i_F), k_i = 12,5 A/div k_v = 500 V/div k_t = 10 ms/div

3. REZULTATI DOBIVENI NA SUSTAVU S TMS320LF240 I d-SPACEOM (SIMULINK)

Na slici 4 dana je blok-shema mikroprocesorskog sustava izgrađenog oko TMS320LF240. Sustav se sastoji od računala s mikroprocesorskom karticom DS1104 koji su povezani sa sklopovljem učinskog dijela pretvarača pomoću komunikacijske pločice.

3. RESULTS OBTAINED WITH TMS320LF240 AND d-SPACE (SIMULINK)

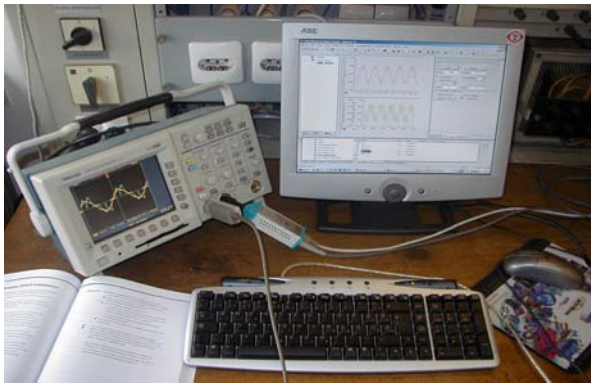
Figure 4 shows a microprocessor system built upon TMS320LF240. It consists of a PC with the microprocessor system DS1104. It is connected with the interface board which collects input signals for the microprocessor system and generates control signals for the power converter.



Slika 4. Jednofazni aktivni učinski filtar s nelinearnim trošilom
Figure 4. Single phase active power filter with nonlinear load

Prednost je ovoga sustava jednostavno korisničko sučelje koje omogućava dijagnostiku i promatranje signala unutar samoga procesa. To uvelike olakšava programiranje i optimizaciju algoritma. Slični sustavi obično imaju ograničenja u tom pogledu, a signali se mjere osciloskopom. Nadalje, prednost je ovoga sustava jednostavno skaliranje signala. Slika 5 prikazuje korisničko sučelje sustava d-SPACE [1].

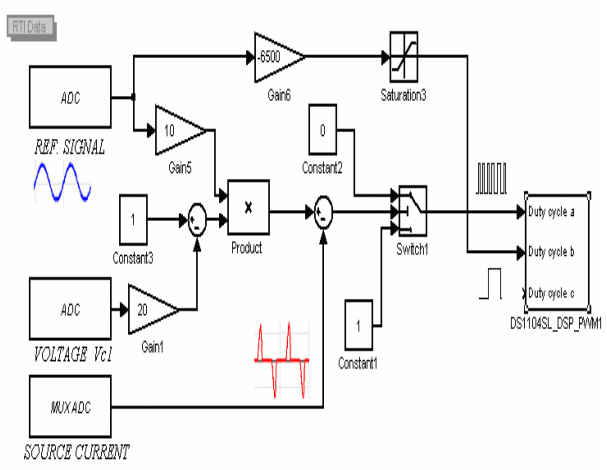
The advantage of this system is its user-friendly interface. It allows system diagnostics from within the process, which simplifies algorithm design and optimisation. Other similar systems have a limitation in the sense of showing numerous system/process variables. In this case, the scaling of signals is simple because each signal can be seen on the screen and then scaled, if necessary. Figure 5 shows the user interface [1].



Slika 5. Mikroprocesorski sustav ACE 1104 i njegovo sučelje dSPACE
Figure 5. Microprocessor system ACE 1104 by d-SPACE and its user-friendly interface

Usporedba upravljačkog algoritma koji se može vidjeti na slikama 1 ili 2 sa slikom 6 može se zaključiti da blok-shema prenesena u Matlab/Simulink predstavlja algoritam u realnom vremenu. Na lijevoj strani mogu se vidjeti signali dobiveni mjerenjem koji se skaliraju i uspoređuju. Signali na sklopnoj frekvenciji dobivaju se usporedbom stvarne i referentne struje, a ostali izravno iz mrežnog napona. Na desnoj se strani posljedično dobiju dva signala na temelju kojih se generiraju još dodatna dva za sva četiri tranzistora APF-a.

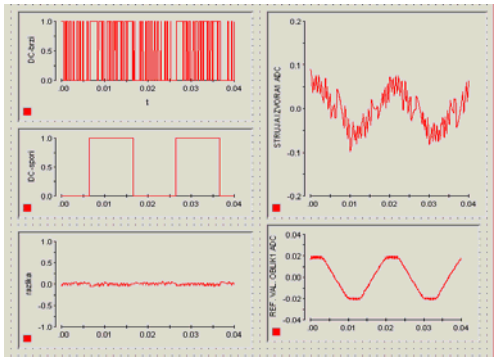
In comparison with the simulating scheme in Figure 2, the APF sliding mode is shown in Figure 6. The input signals are shown on the left side. The signals are obtained through measurement and are scaled. One transistor pair is switched on source frequency and it is generated by source voltage. The others, the fast switching transistors, are obtained by comparing reference current and actual source current. The two of them are then compared in order to achieve all four transistor signals.



Slika 6. Algoritam aktivnog učinskog filtra u programu Matlab/Simulink
Figure 6. Active power filter control algorithm in Matlab/Simulink

Svi spomenuti signali mogu se promatrati u okviru korisničkog sučelja d-SPACE kao što je i prikazano na slici 7. Sklopna frekvencija sklopa bira se po volji od 2 kHZ do 7 kHz. Ako je odabrana frekvencija viša, može se primijetiti da više ne odgovara stvarnoj frekvenciji sklapanja u sklopu.

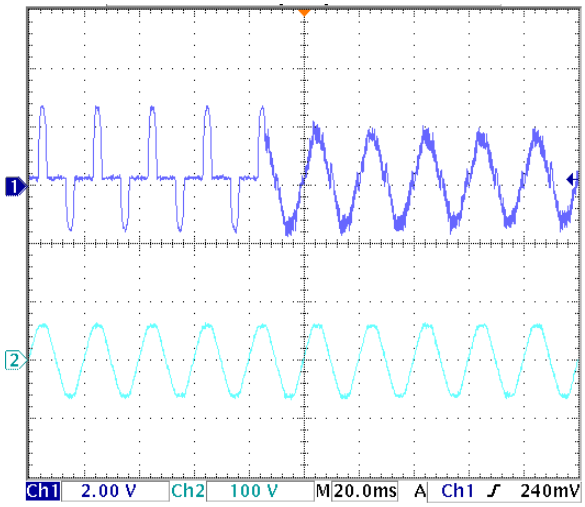
All of these signals can be observed by advanced d-SPACE interface as shown in Fig. 7. Sliding mode or switching frequency can be adjusted between 2 kHz and 7 kHz. If the frequency is higher, the system obviously becomes too slow and cannot operate properly because it no longer applies to the actual switching frequency in the switch.



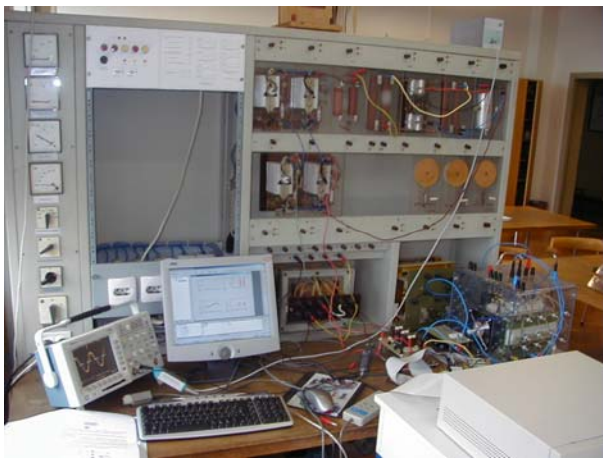
Slika 7. Upravljački signali tranzistora na sklopnoj frekvenciji (gore-lijevo), upravljački signali tranzistora koji sklapaju na mrežnoj frekvenciji (lijevo u sredini), signal pogreške među dvjema strujama lijevo-dolje), struja izvora (desno na vrhu) i referentna struja APF-a (lijevo na dnu)
Figure 7. APF Switching transistor waveforms (left- top), supply frequency transistors that switch to network frequency (left – middle), error of the two compared currents (lower – left), source current (right – top) and APF current reference (left – bottom) at 7 kHz switching frequency

Signali se mogu promatrati na osciloskopu gdje je broj kanala ograničen na 2 (slika 8) što ograničava uvid u to što se događa u sustavu. Može se reći da je to glavna prednost razvijenoga korisničkog sučelja. Slika 9 prikazuje cjelokupan mikroprocesorski sustav s pripadajućim sučeljem i pretvaračem.

The signals can be also observed on oscilloscope. It is interesting to note that Fig. 7 presents five signals. On the other hand, the oscilloscope has only two channels (Fig. 8), which clearly shows the advantage of this microprocessor system and its user-friendly interface. Figure 9 shows the complete APF and design equipment.



Slika 8. Izmjereni signali APF-a: struja izvora (1), referentna struja (skalirani napon napajanja)(2), $V_S = 45$ V, $R = 50$ Ω, $C = 10$ μF
Figure 8. Measured APF waveforms: source current (1), referent current (source voltage) (2); $V_S = 45$ V, $R = 50$ Ω, $C = 10$ μF



Slika 9. Mikroprocesorski sustav s procesorom TMS320LF240 i sučeljem u Matlab/Simulinku, FER, Zagreb, Hrvatska
Figure 9. Microprocessor system with TMS320LF240 core with Matlab/Simulink as the programming interface, FER Zagreb, Croatia

3. REZULTATI DOBIVENI NA SUSTAVU BAZIRANOM NA TMS320LF2407 S KORISNIČKIM SUČELJEM *CODE COMPOSER* (*ASSEMBLER*)

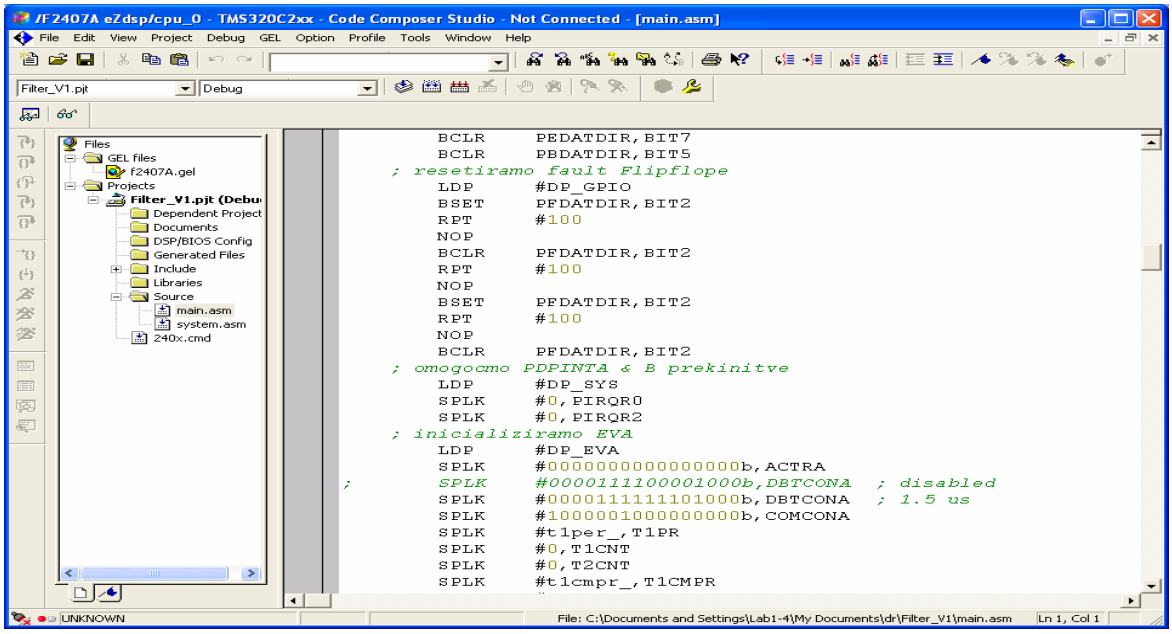
Programiranje na sustavu koji je sagrađen na bazi mikroprocesora TMS320LF2407 korištenjem korisničkoga sučelja *Code Composer* (*Texas Instruments*) ima više nedostataka u usporedbi s prethodnim sustavom. Ne postoji nikakav dodatak (monitor niti prozor) koji omogućava promatranje događaja unutar procesa (algoritma) na način na koji to omugućava osciloskop. Skaliranje signala na taj način postaje upitno, posebno ako je razina šuma u sustavu visoka.

3. RESULTS OBTAINED WITH TMS320LF2407 AND CODE COMPOSER (ASSEMBLER)

The active power filter design with TMS320LF2407 and *Code Composer* (*Texas Instruments*) platform has few disadvantages compared to the aforementioned system (the d-SPACE solution). Fixed point algebra in the assembler programming language demands advanced programming skills. There is no addition (monitor or window) for observing the inner happenings of the process (algorithm) in such a way that it would enable the use of the oscilloscope. Scaling signals in such a way becomes uncertain, especially if there exists a high noise level in the system.

U prethodnom slučaju (d-SPACE) korišten je pretvarač tvrtke Semikron, a u drugom vlastiti prototip tako da su bili prisutni problemi s optimiranjem sklopa (npr. šum).

In the first example (d-SPACE), the Semicron product was used and in the second example a home-built prototype was used, so that hardware problems regarding switch optimization became apparent (e.g. noise level). Fig. 10 shows the *Code Composer* assembly language programming interface.



Slika 10. Korisničko sučelje Code Composer
Figure 10. Code Composer programing interface

Programiranje u jeziku asembler predstavlja izazov već na razini samog definiranja sustava (ulazi mogu biti korišteni kao izlazi i obrnuto, tako da je sve potrebno definirati) što se zove inicijalizacija i konačno programiranje algoritma. U cilju uvida u razliku između jednoga i drugog sučelja (programa) u nastavku je dan manji dio programa u asembleru i to onaj koji se odnosi na uključivanje tranzistora i definiciju PWM-a (inicijalizacija PWM-a).

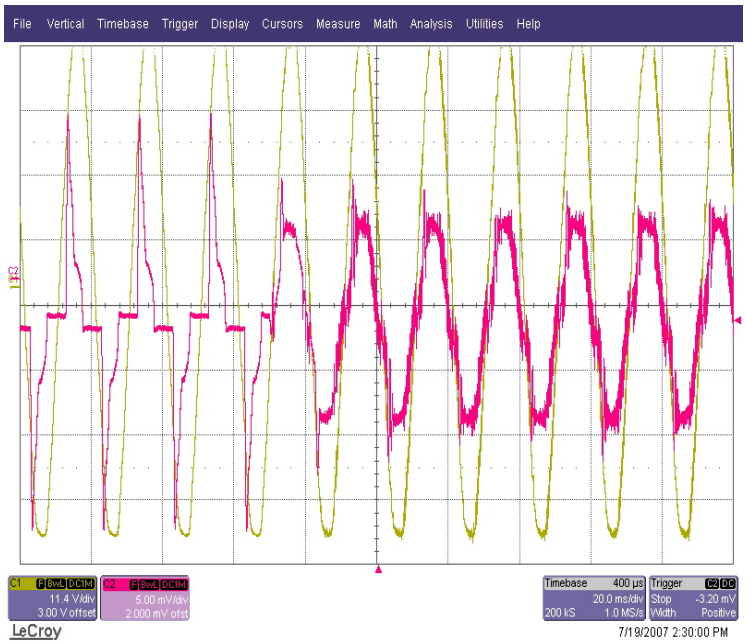
Assembly language programming presents a challenge on the very level of defining the system (inputs can be used as outputs and vice versa, so each channel has to be defined) and this is termed as system initialization and finally programming of the algorithm. In the aim of insight into the difference between one program and another, it follows that only a part of the assembly language code has been given. The presented code refers to transistor switching and PWM definition (PWM registers – CMPR, EVA initialization).

```
LDP  #DP_B1a; odabir dijela memorije u kojem se nalazi akumulator
      ; selecting data page for activating accumulator
LACC   u1  ; pohranjivanje uzorčenog ulaznog signala u akumulator
      ; storing source voltage sampled signal in accumulator
BCND  S1,LT ; sklapanje tranzistora koji sklapa na frekvenciji 50 Hz
      ; logika sporog tranzistora
      ; ukoliko je sadržaj akumulatora po vrijednosti manji od nule
      ; onda skoči na dio programa označen s S1
      ; 50 Hz switching transistor logic or slow transistor comparator
      ; if data in accumulator is less than zero then jump to S1
BCND S3,GT  ; sklapanje tranzistora koji sklapa na frekvenciji 20 kHz
      ; logika brzog tranzistora
      ; ukoliko je sadržaj akumulatora po vrijednosti veći od nule
      ; onda skoči na dio programa označen s S3
      ; 20 kHz switching transistor logic or fast transistor comparator
```

```
            ; if data in accumulator is  greater  than  zero  then  jump  to  S3
      S1    LDP  #DP_EVA
            ; selektiranje  dijela  memorije  u kojoj se nalazi registar za
            ; kompariranje signala i generiranje PWM-a
            ; selecting data page where compare register CMPR2 can be found in
            ; order to define transistor pulse width -> PWM
      SPLK #2000h,CMPR2;
            ; definiranje faktora vođenje unutar perida koji je ranije definiran
            ; u inicijalizacijskom dijelu programa / za ostvarivanje kliznog
            ; načina rada moguće je odabrati faktor opterećenja 1 jer se petlja
            ; izvršava 20 000 puta u sekundi, a moguće je odabrati i manji ili
            ; promjenljiv faktor opterećenja
      B    S4
            ; bezuvjetni skok   na  S4  da nebi  „pregazili“  vrijednost u CMPR2
            ; unconditional jump to S4 to avoid redefinition  of  register CMPR2
S3    LDP  #DP_EVA
            ; aktiviranje pripadajućeg dijela memorije ili čipa ->  PWM  izlaz A
            ; selecting data page for PWM register in event manager A
      SPLK #000h,CMPR2;
            ; stanje  PWM  registra  CMPR2  se  postavlja  na  nulu  tako  da  je
            ; promatrani  tranzistor  za  postavljeni  uvijet  sigurno  isključen;
            ; njegov  komplementarni  tranzistor  je  time  postavljen  u  stanje
            logične jedinice.
S4    NOP   ; naredba koja ništa ne napravi / „empty“ instruction
      LDP  #DP_B1a
            ; selektiranje dijela memorije u kojem se nalazi akumulator
            ; accumulator data page selection
      LACC    u1
            ; pohranjivanje uzorčenog ulaznog signala u akumulator
            ; loading of sampled source voltage in accumulator
;     SFR ; input voltage scaling / skaliranje ulaznog napona
;     SFR ; for obtaining reference current / za dobivanje referentne struje
      MPY  #0002h
      SUB  ib1  ;skaliranje izmjerene struje izvora / source current scaling
;     ADD  #30h ; reduciranje ofseta koji se pojavi na postojećoj opremi
            ; reducing of offset
      BCND P1,LT; sklopni tranzistor, fast transistor comparator
      BCND P3,GT; sklopni tranzistor, fast transistor comparator
      P1  LDP  #DP_EVA
      SPLK #1300,CMPR1 ;1300 1200-1300 zaštita od KS, short circuit protection
      B    P4
P3    LDP  #DP_EVA
      SPLK #300,CMPR1; 250 300
P4    NOP
      SPLK #0000000011100110b,ACTRA  ; definicija PWM moda / PWM mode definition
```

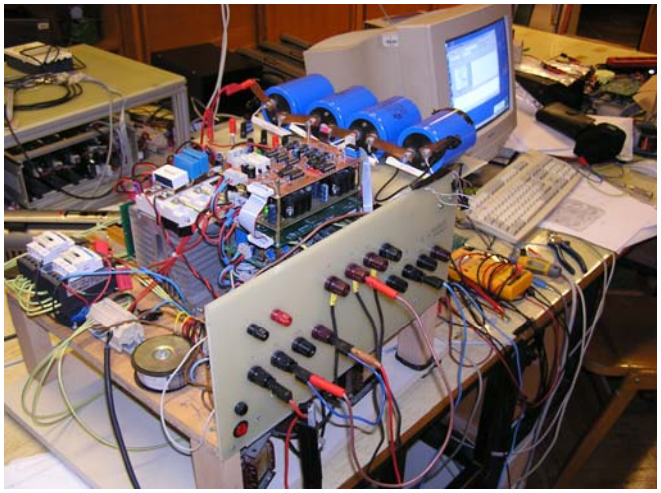
Ovaj pristup predstavlja teži način za postizanje rezultata bliskih onima postignutima sa sustavom iz prvog slučaja (*THD* je sada oko 10% umjesto prijašnjih 15% filtrirajući signal s *THD*-om između 70 i 80%). U ovom slučaju brzina mikroprocesora nije više ograničavajući faktor u brzini sklapanja tranzistora, već kompromis između performansi sklopa i gubitaka na sklopkama. Odabrana je frekvencija sklapanja 25 kHz [9], [10], [11]. Slika 11 predstavlja iste signale na sustavu TMS320LF2407 kao i slika 8 za signale na TMS320LF240 (u prethodnom slučaju).

This option represents a more difficult way of achieving results comparible to those of the first example (*THD* is now approximately 10% instead of the previous 15% filtering signal, with the *THD* between 70% and 80%). The main benefit is a higher switching frequency. In this case, processing speed is no longer a limiting factor for transistor switching speed. In this example, 25 kHz switching frequency was chosen as a compromise between harmonic distortion of source current and transistor (APF) losses [9], [10], [11]. Fig. 11 shows APF response designed in the Code Composer Studio.



Slika 11. Valni oblik napona napajanja sa strujnim signalom u svojem središtu (ekvivalent slike 8), $k_i = 2$ A/div, $k_v = 11{,}4$ V/div , $k_t = 20$ ms/div

Figure 11. Waveform of source voltage intersected by source current before and after APF connection (figure 8 equivalent), $k_i = 2$ A/div, $k_v = 11{,}4$ V/div, $k_t = 20$ ms/div



Slika 12. Mikroprocesorski sustav s TMS320LF2407 i sučeljem Code Composer Studio(Texas Instruments), FE Ljubljana, Slovenija

Figure 12. Microprocessor system with TMS320LF2407 core and Texas Instruments user interface – Code Composer Studio (Texas Instruments), FE Ljubljana, Slovenia

Inicijalizacija procesora, koja predstavlja veći dio programa nije priložena zbog ograničenoga prostora, ali se već i iz priloženog može vidjeti da je za programiranje potrebno detaljno poznavanje cjelokupnog sustava uključujući sučelje, arhitekturu mikroprocesora i sam pretvarač.

Initialization of the processor, which represents a larger part of the program, is not given due to space limitation, although just from listed part of program it can be noted that the assembly programming language demands more programming skills, including knowledge of the hardware, microprocessor architecture and the filter itself.

Posljedično ovaj sustav omogućuje veću fleksibilnost kod programiranja i veću brzinu izvođenja operacija. Jednim dijelom to je posljedica bržeg mikroprocesora (TMS240LF2407 obavlja jednu instrukciju za 33 ns, a TMS240LF240 za 50 ns [3], [4]) ali i optimizacije samoga programa.

4. ZAKLJUČAK

Aktivni učinski pretvarač ostvaren je na dvama različitim mikroprocesorskim sustavima koji su dio iste skupine mikroprocesora (TMS320LF240...). Minorne razlike među tim mikroprocesorima ne opravdavaju nekoliko puta brže računanje u slučaju TMS320LF2407 već to treba pripisati korisničkom sučelju i samom programu. Visokosofisticirano sučelje proizvođača dSPACE ograničava brzinu algoritma na manje od 10 kHz, što kod sustava sa sučeljem *Code Composer* nije slučaj (sklopna frekvencija 25 kHz i više). U tom je slučaju frekvencija sklapanja ograničena gubicima u tranzistorskim sklopkama. Prema mišljenju autora sofisticirana korisnička sučelja imaju prednost u edukacijskim sustavima čak i prilikom razvijanja novih algoritama gdje brzina izračuna nije od ključne važnosti za rad sustava. Programiranje u asembleru u drugu ruku pokazuje svoje prednosti u primjenama energetske elektronike i elektromotornih pogona kada je potrebno postići veliku brzinu rada sustava ali i nižu cijenu sustava. U slučajevima upotrebe i razvoja mehatroničkih rješenja koja obuhvaćaju zahtjevnije elektromotorne pogone (posebno s izmjeničnim strojevima) programiranje nema alternativu u grafičkom sučelju.

5. POPIS OZNAKA

struja izvora ili napajanja	I_s - A	supply or source current
napon izvora ili napajanja	V_s - V	supply or source voltage
struja trošila	I_L - A	load current
struja filtra	I_F - A	filter current
referentna struja	I_R - A	referent current
napon filtarskoga kondenzatora	V_{C1} - V	filter capacitor voltage

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[3] TMS320F240 DSP Controller datasheet, Texas Instruments, SPRS042E, 1996.

[4] TMS320F2407, TMS320F2406, TMS320F2402 DSP Controllers datasheet, Texas Instruments, SPRS094I, 1999.

As a result, this system offers greater programming flexibility and enables higher switching frequencies of the APF and better performance of the circuit. This is partially a consequence of the faster processor speed, but it is also due to code optimization (the TMS240LF2407 instruction cycle is 33 ns, whereas the TMS240LF240 instruction cycle is 50 ns [3], [4]).

4. CONCLUSION

An active power filter has been designed on two different platforms which are members of the same microprocessor family (TMS320LF240...). Minor differences between these processors do not justify the greatly increased speed in the case of the TMS320LF2407, but rather this should be attributed to the user interface of the program itself. The highly sophisticated interface of the manufacturer d-SPACE limits the algorithm speed to less than 10 kHz, which is not the case with the *Code Composer* interface (switching frequency of 25 kHz or more). In this case, the switching frequency is limited by transistor losses. It is the author's opinion that a sophisticated user interface has an advantage in educational and algorithmic developmental applications where switching speed is not crucial to system operation. Assembly language programming, on the other hand, is a better choice for industrial applications (e.g. power electronics or electric motors) where higher speeds, and cost efficiency are key. There is no better alternative to programming in the use of the graphical interface regarding the use and development of a mechatronic solution that undertakes more complex induction motors (especially in terms of alternate machines).

5. LIST OF SYMBOLS

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Pregledni članak

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