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Dual space vector PWM technique for a three-phase to five-phase quasi Z-source direct matrix converter

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ABSTRACT

This article proposes a dual space vector PWM control technique for a three-phase to five-phase quasi Z-source direct matrix converter (QZSDMC). The proposed circuit consists of a quasi-impedance source network along with a five-phase traditional matrix converter. With the observation of bidirectional operating capability and the utilization of shoot-through duty ratio, the proposed converter can ensure both buck and boost operations. This converter overcomes the voltage transfer ratio restriction and poor voltage regulation of the traditional matrix converter. Also, this converter ensures continuous input current with an absence of input LC filter components. The proposed direct AC to AC power converter gives an alternate solution to the multiphase drive system instead of the traditional voltage source inverter. The developed dual space vector PWM control technique for three-phase to five-phase voltage conversion is derived from the basic space vector PWM approach. The proposed dual space vector PWM technique utilizes 90 active states and 3 zero vector states among 243 switching states. The QZSDMC has been analysed with a dual space vector PWM approach along with the distribution of shoot-through state in the zero vector. The proposed topology along with the control strategy has been simulated using MATLAB/Simulink environment.

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KEYWORDS
Direct matrix converter; modulation index; PWM techniques; quasi Z-source DMC; variable frequency

1. Introduction

The matrix converter is a bidirectional power flow converter. It's consisting of semiconductor switches. The switches are arranged like an array or matrix [1]. Recently, the matrix converter attracted more researchers based on its features and advantages such as sinusoidal input and output currents, controlled bidirectional power flow, and operation at unity power factor for all loads [2,3]. The control algorithm plays a major role in the performance of power electronics converters such as AC to AC or AC to DC to AC [4]. There are many modulation schemes are developed for three-phase or more output-based voltage source inverters. In general modulation schemes for matrix, converters are more complex and it's classified based on the circuit configuration like direct and indirect matrix converters [5]. Alesina and Venturini developed a direct PWM control technique for a direct matrix converter (DMC). Initially, this modulation scheme limits the output as half of its inputs [6]. Using the third harmonics injection PWM scheme, this limit is further extended to 0.866. In the linear modulation region, this limit is realized as maximum for a three-phase to three-phase matrix converter [7].

On the other hand, virtual cascaded connections of the three-phase rectifier, imaginary dc-link capacitor and voltage source inverter act as indirect matrix converters [8]. The presence of bulk intermediate capacitor and inductor bank acts as a filtering component will increase the cost, size, weight and switching losses. Also, the reliability of the converter is poor [9]. To overcome these disadvantages, many researchers are choosing the direct matrix converter (DMC). The main advantages of DMC are the absence of an intermediate DC-link capacitor, low switching losses and higher power conversion ratio [10,11]. The limitation of DMC are the voltage transfer ratio of 0.866, the usage of bidirectional switches are more, poor fault ride-through capability, complex power control strategies, increased common-mode voltages and complicated protection circuits [12,13]. Other operation-related limitations are input side is never to be short-circuited and the output side is never to be open-circuited. It has a complex commutation process as a result, the poor quality output waveform will be getting from the set-up [14,15].

The voltage transfer capability can be increased by two methods. The first method is the usage of a transformer. Again the disadvantages are size and cost is increases, efficiency goes to decreases [16]. The second method is the usage of a matrix reactance frequency converter (MRFC). It has two classifications named as integrated matrix reactance frequency

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converter (IMRFC) and cascaded matrix reactance frequency converter (CMRFC). Both methods of MRFC have their disadvantages such as poor voltage gain, very low input side power factor, complex control algorithm, and distorted input and output current waveforms [17].

All these disadvantages are overcome by introducing an impedance source-based direct matrix converter (ZSDMC) [18]. The major advantages of this converter are minimum-sized LC components, performing both buck and boost operations, better reliability and higher efficiency, as well as being free from the dead zone. The disadvantages of ZSDMC are, the voltage transfer ratio is 1.15, waveform phase shifting, inaccurate control, higher voltage, and current switching stresses, higher system losses, discontinuous input current and higher input current harmonics [19,20].

To overcome these disadvantages, many researchers focused on a quasi Z-source direct matrix converter (QZSDMC). It overcomes voltage gain limitations and offers up to four to five times higher voltage gain. It has low impulse current, no phase shift, low voltage and current switching stress [21,22]. With the addition of a quasi Z-source into a direct matrix converter, the electromagnetic interferences ability will be enhanced. It offers high-quality waveforms, continuous input currents and less capacitor voltage stress [23,24].

The conventional structure for variable speed drive has a three-phase power electronics converter with a three-phase motor. The matrix converter or voltage source inverter is coming under a modular power electronics converter [25,26]. When the motor is connected to any one of the modular power electronics converters and increases legs automatically many phases go to increases. The development of modular power electronics converters makes a degree of freedom in the number of possible phases [27]. The multiphase motor drives have their advantages over traditional three-phase motor drives. The notable advantages are high-frequency torque pulsation with minimum amplitude, minimum rotor harmonic current losses, minimum DC-link current harmonics, improved system reliability and redundant structure [28,29].

The five-phase motor drive system has several salient features. It's very attractive to industrial applications. The defense, ship propulsion, traction drive, aircraft and hospital applications required high fault-tolerant property [30,31]. If the number of phases increases automatically volume of the motor drive gets reduced. In naval ships and mining applications, space requirements are very stringent. The five-phase system is more suitable for these applications [32,33]. The British naval ship contains a 15-phase induction motor drive built by Alstom. The machine winding has been reconfigured as 5 three phases or 3 five phases by the application of modular power electronics converters [34,35].

In this paper, the dual space vector PWM-based control strategy is proposed based on the space vector model. The proposed dual SVPWM technique applies for a three-phase to five-phase direct matrix converter cascaded with a quasi-impedance source network. This dual SVPWM is more suitable for digital implementation. In this scheme, the output voltage is enhanced up to four to five times the input voltages. Theoretically, the maximum output magnitude was obtained in the linear modulation region using QZSDMC configurations. This paper presents the simulation result using MATLAB/Simulink environment and the same is validated by experimental prototype set-up. The simulation and experimental results are matched with good feasibility by the suggested QZSDMC topology and its control strategy.

2. QZSDMC: Topology, operation and modelling

Figure 1 shows the main circuit configuration of QZSDMC. It's consisting of a three-phase source, input filter, QZS network, direct matrix converter and five-phase RL load. The QZS network consisting of six inductors named L_{ax}, L_{bx}, L_{cx} (where $x = 1, 2$), six capacitors named as C_{ax}, C_{bx}, C_{cx} (where $x = 1, 2$) and three bidirectional switches S_y (where $y =$ a,b,c) with the same switching states, as a result, the switching signal is represented as S_0. All inductors having equal values as well as all the capacitors are having equal values [36]. The three-phase to five-phase power circuit topology is connected in series with the Z-source network as presented in Figure 1. For five-phase, it consists of five legs and each consisting of bidirectional switches. The bidirectional power flow switches consist of two power diodes and two IGBT switches. The power diode and IGBTs are connected in series and the entire switching configuration should be connected in a common-emitter configured bidirectional power flow switch as available in Figure 2 [37]. The output configuration should be odd in phases. The nature of the load connected to the power circuit should be RL load.

The definition for switching function like

$S_{oi} = 1$ for the switch is in a closed condition
$S_{oi} = 0$ for the switch is in an open condition

where o = A, B, C, D, E represent output phases and $i =$ a, b, c represent input phases. The general switching constrain is

$$S_{Ai} + S_{Bi} + S_{Ci} + S_{Di} + S_{Ei} = 1$$

The QZSDMC working principle consists of two states called shoot-through state and non-shoot-through the state. The switch S_0 is in an OFF state during shoot through the state as a result the output of QZSDMC is shorted for boost operation. The switch S_0 is in an ON state during non-shoot-through the state, and the QZSDMC is working as normal DMC. The equilibrium of the system should be maintained

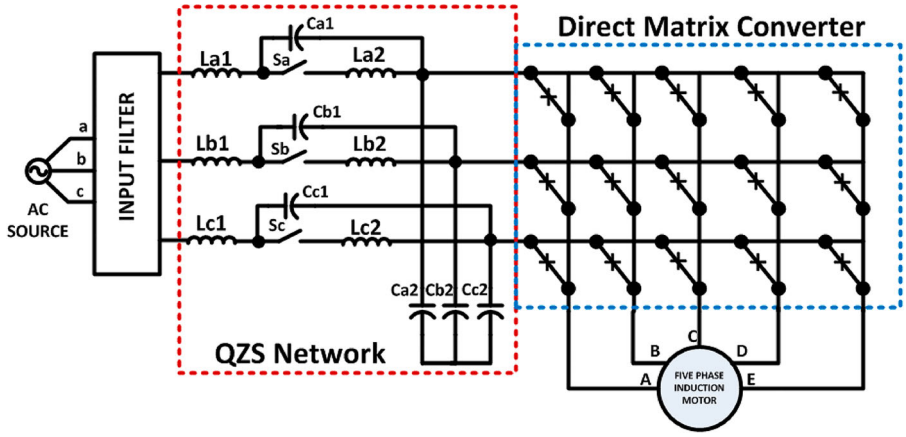


Figure 1. Main circuit configuration for three-phase to five-phase QZSDMC.

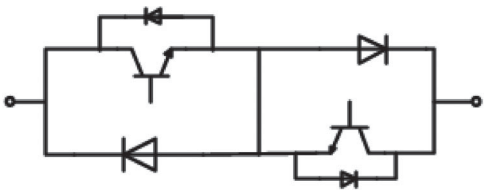


Figure 2. Common-emitter configured bidirectional power flow switch.

by making all capacitors are equal and all inductors are equal [38,39].

Consider T_s as one switching cycle, consisting of T_1 as a shoot-through time interval and T_2 as a non-shoot-through time interval. Hence, $T_s = T_1 + T_2$ and the shoot-through duty ratio $D = T_1/T_s$. The output voltage equation during shoot through the state can be represented as

$$\begin{pmatrix} V_{AB} \\ V_{BC} \\ V_{CD} \\ V_{DE} \\ V_{EA} \end{pmatrix} = \begin{pmatrix} Vla1 \\ Vlb1 \\ Vlc1 \\ Vld1 \\ Vle1 \end{pmatrix} - \begin{pmatrix} Vlb1 \\ Vlc1 \\ Vld1 \\ Vle1 \\ Vla1 \end{pmatrix} + \begin{pmatrix} Vca1 \\ Vcb1 \\ Vcc1 \\ Vcd1 \\ Vce1 \end{pmatrix} - \begin{pmatrix} Vcb1 \\ Vcc1 \\ Vcd1 \\ Vce1 \\ Vca1 \end{pmatrix} \quad (1)$$

The output voltage equation during non-shoot-through the state can be represented as

$$\begin{pmatrix} V_{AB} \\ V_{BC} \\ V_{CD} \\ V_{DE} \\ V_{EA} \end{pmatrix} = \begin{pmatrix} Vla1 \\ Vlb1 \\ Vlc1 \\ Vld1 \\ Vle1 \end{pmatrix} - \begin{pmatrix} Vlb1 \\ Vlc1 \\ Vld1 \\ Vle1 \\ Vla1 \end{pmatrix} + \begin{pmatrix} Vca1 \\ Vcb1 \\ Vcc1 \\ Vcd1 \\ Vce1 \end{pmatrix} - \begin{pmatrix} Vcb1 \\ Vcc1 \\ Vcd1 \\ Vce1 \\ Vca1 \end{pmatrix} + \begin{pmatrix} Va'b' \\ Vb'c' \\ Vc'd' \\ Vd'e' \\ Ve'a' \end{pmatrix} \quad (2)$$

During the steady-state condition over one switching cycle in the inductor, the average voltage is zero [40,41]. The symmetrical voltages across three-phase capacitors are

$$\begin{pmatrix} Va'b' \\ Vb'c' \\ Vc'a' \end{pmatrix} = \frac{1}{1-2D} \begin{pmatrix} Vab \\ Vbc \\ Vca \end{pmatrix} \quad (3)$$

The boost factor B for ZSDMC can be expressed as

$$B_{\text{ZSDMC}} = \frac{V_o}{V_i} = \frac{1}{\sqrt{3D^2 - 3D + 1}} \quad (4)$$

The boost factor B for QZSDMC can be stated as

$$B_{\text{QZSDMC}} = \frac{V_o}{V_i} = \frac{1}{1-2D} \quad (5)$$

where V_o is the amplitude of output voltage and V_i is the amplitude of input voltage.

Thus, the voltage gain "G" for the QZS network using boost factor and modulation index, over one switching cycle is [42]

$$\text{G} = BM \quad (6)$$

3. SVPMW control algorithm

In the space vector plane, the three-phase input current and five-phase output voltages are represented based on the space vector algorithm. In the QZSDMC, there are different switching states are available [43,44]. The switching state represents the connections between the output phases to the input phases. The total numbers of switches including QZS are 18. In that, the main bidirectional switches are 15. The possible combinations of switching states are 2^{15}. The following constraints should be followed by QZSDMC for safe switching operations [45,46]. At any switching time do not short circuit at the input side and do not open-circuited at the output side. There are 3^{15} switching combinations are available to satisfy the above-mentioned switching

combinations. These 243 possible switching combinations can be categorized into five groups. The combination of switches is represented as [A, B, C], where A, B, C represents the combination of output phases are connected to the input phases a, b, c. The first groups of switching states are zero vectors (i.e. A # B # C [A, B, C ∈ 0, 0, 5]). In this switching state, all the output phases are connected to any one of the same input phases. In the zero vectors, the magnitude and frequency of the output parameters are zero. There are three possible switching combinations are available in this group [47,48].

The second groups of switching states are A # B # C [A, B, C ∈ 0, 1, 4]. In this switching state, any four of the output phases are connected to any one of the same input phases and the remaining one of the output phases is connected to the remaining input phase. One input phase is always not connected to the output phase. There are 30 switching combinations are available in this category. In the space vector, it has a variable amplitude and constant frequency, i.e. amplitude of output voltages depending on the selected input line voltages. In this case, 30 combinations of output voltage and input current space vectors phase angle do not depend on the input voltage and output current phase angle, respectively.

The third groups of switching states are A # B # C [A, B, C ∈ 0, 2, 3]. In this switching state, any three of the output phases are connected to any one of the same input phases and two of the output phases are connected to any one of the remaining input phases. One input phase is always not connected to the output phase. There are 60 switching combinations are available in this category. In the space vector, it has a variable amplitude and constant frequency, i.e. amplitude of output voltages depending on the selected input line voltages. In this case, 30 combinations of output voltage and input current space vectors phase angle do not depend on the input voltage and output current phase angle, respectively [49,50].

The fourth groups of switching states are A # B # C [A, B, C ∈ 0, 2, 3]. In this switching state, any three of the output phases are connected to any one of the same input phases and the remaining two output phases are connected to the remaining two input phases. In this case, all the input phases are engaged with any one of the output phases. There are 60 switching combinations are available in this group. In the space vector, it has a variable amplitude and variable frequency. It says that the amplitude of output voltages depends on the selected input line voltages. In this case, the 60 combinations of output voltage and input current space vectors space angle depend on the input voltage and output current space vector space angles. The output voltage and input current space vectors of these 60 combinations do not have prefixed positions. The locus of the space vector forms ellipses at a different orientation. As a result, the phase angle of input and output vectors cannot be controlled, independently. So the space vector modulation for three-phase to five-phase conversion does not consist of this category of switching states.

The fifth groups of switching states are A # B # C [A, B, C ∈ 1, 2, 2]. In this switching state, any two of the output phases are connected to any one of the same input phases, another two of the output phases are connected to any one of the same input phases and the remaining one output phase is connected to the remaining one input phase. In this case, all the input phases are engaged with any one of the output phases. There are 90 switching combinations are available in this group. In the space vector, it has a variable amplitude and variable frequency. It says that the amplitude of output voltages depends on the selected input line voltages. In this case, the 90 combinations of output voltage and input current space vectors space angle depend on the input voltage and output current space vector space angles. The output voltage and input current space vectors of these 90 combinations do not have prefixed positions. The locus of the space vector forms ellipses at a different orientation. As a result, the phase angle of input and output vectors cannot be controlled, independently. So the space vector modulation for three-phase to five-phase conversion does not consist of this category of switching states. As a result, the effective utilization of the active space vectors for the proposed dual SVPWM for three-phase to five-phase QZSDMC is used in only 93 vector combinations [51,52].

4. Dual space vector PWM control strategy

Figure 1 represents the general topology for three-phase to five-phase QZSDMC. The modulation technique effectively used to control the QZSDMC utilizes only 93 active switching vectors instead of 243. Depending on the output contributions, these active switching states can be grouped into four.

Group 1 [A, B, C ∈ 5, 0, 0]. Three vectors come under this category and it's called zero vectors.

Group 2 [A, B, C ∈ 4, 1, 0]. Thirty vectors come under this category and it's called medium vectors.

Group 3 [A, B, C ∈ 3, 2, 0]. Thirty vectors come under this category and it's called large vectors. In this switching state, any two adjacent output phases are connected to the same input phase.

Group 4 [A, B, C ∈ 3, 2, 0]. The remaining 30 vectors come under this category and it's called large vectors. The major difference in these switching states with the previous case is any two alternate output phases are connected to the same input phase (Figure 3).

Figures 4 and 5 represent the input current switching space vectors and output voltage space vectors. Depending on the switching sequences, all the input current space vectors are combined with all the output voltage space vectors. For each combination, the input voltage and current, as well as output voltage and input

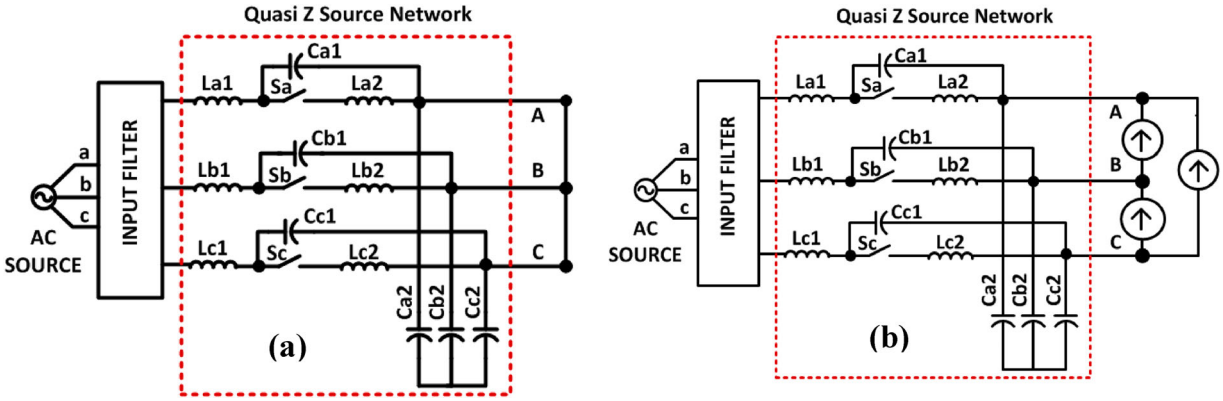


Figure 3. Equivalent circuit of QZSDMC (a) at shoot-through state and (b) at non-shoot-through state.

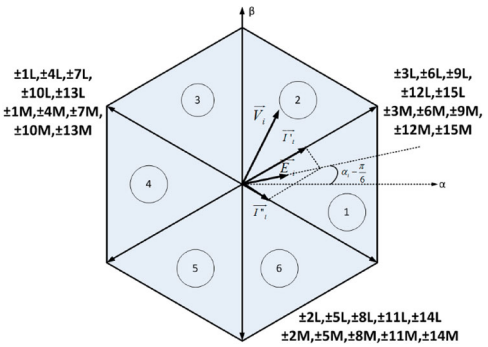


Figure 4. Group 3: Input current switching space vector.

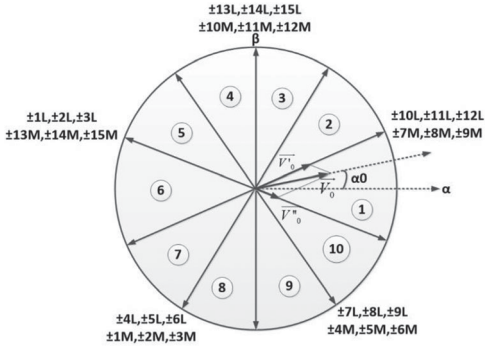


Figure 5. Group 3: Output voltage switching space vector.

current space vectors, are defined as

$$\overrightarrow{V_i} = \frac{2}{3}\left(V_{ab} + V_{bc}e^{j\frac{2\pi}{3}} + V_{ca}e^{j\frac{4\pi}{3}}\right) = V_i \cdot e^{j\alpha_i} \quad (7)$$

$$\overrightarrow{V_0} = \frac{2}{5}\left(V_{AB} + V_{BC}e^{j\frac{2\pi}{5}} + V_{CD}e^{j\frac{4\pi}{5}} + V_{DE}e^{j\frac{6\pi}{5}} + V_{EA}e^{j\frac{8\pi}{5}}\right) = V_0 \cdot e^{j\alpha_0} \quad (8)$$

$$\overrightarrow{I_i} = \frac{2}{3}\left(I_a + I_b e^{j\frac{2\pi}{3}} + I_c e^{j\frac{4\pi}{3}}\right) = I_i \cdot e^{j\beta_i} \quad (9)$$

$$\overrightarrow{I_0} = \frac{2}{5}\left(I_A + I_B e^{j\frac{2\pi}{5}} + I_C e^{j\frac{4\pi}{5}} + I_D e^{j\frac{6\pi}{5}} + I_E e^{j\frac{8\pi}{5}}\right) = I_0 \cdot e^{j\beta_0} \quad (10)$$

where V_{ab}, V_{bc}, V_{ca} are input line voltages; V_{AB}, V_{BC}, V_{CD}, V_{DE}, V_{EA} are output line voltages; I_a, I_b, I_c are input currents; I_A, I_B, I_C, I_D, I_E are output currents; α_i is the input voltage vector space angle; α_0 is the output voltage vector space angle; β_i is the input current vector phase angle; β_0 is the output current vector phase angle.

Let, M is the medium size space vector; L is the large size space vector; $\overrightarrow{V_i}$ is the desired input line voltage space vector; $\overrightarrow{V_0}$ is the desired output line voltage space vector; $\overrightarrow{I_i}$ is the desired input line current space vector; $\overrightarrow{I_0}$ is the desired output line current space vector and $\overrightarrow{E_i}$ is the input line to neutral voltage vector, and it's defined as

$$\overrightarrow{E_i} = \frac{1}{\sqrt{3}}\overrightarrow{V_i} \cdot e^{-j\frac{\pi}{6}} \quad (11)$$

The proposed space vector control strategy must obey the constraint of unity input power factor for the generation of desired output voltage vectors. So the direction of $\overrightarrow{E_i}$ and $\overrightarrow{I_i}$ should be the same for obtaining unity input power factor. From Figures 4 and 5, the identified three-phase input and five-phase output side sectors are 6 and 10, respectively. Consider input and output vectors are in sector-1, the components of $\overrightarrow{V_0}$ are $\overrightarrow{V'_0}$ and $\overrightarrow{V''_0}$ (i.e. two adjacent vector directions). Similarly, the components of $\overrightarrow{I_i}$ are $\overrightarrow{I'_i}$ and $\overrightarrow{I''_i}$. All the output voltage and input current components at sector-1 are given below.

$\overrightarrow{V'_0}$: ± 10L, ±11L, ±12L and ± 7M, ±8M, ±9M

$\overrightarrow{V''_0}$: ± 1L, ±2L, ±3L and ± 13M, ±14M, ±15M

$\overrightarrow{I'_i}$: ± 3L, ±6L, ±9L, ±12L, ±15L and ± 3M, ± 6M, ±9M, ±12M, ±15M

$\overrightarrow{I''_i}$: ± 1L, ±4L, ±7L, ±10L, ±13L and ± 1M, ±4M, ± 7M, ±10M, ±13M

Table 1. Space vector choices in SVPWM for various sectors combinations.

Sector number for V_0	Sector number for I_i		
	1 or 4	2 or 5	3 or 6
1 or 6	±1L,±3L,±10L,±12L±7M,±9M,±13M,±15M	±2L,±3L,±12L,±11L±8M,±9M,±15M,±14M	±1L,±2L,±10L,±11L±7M,±8M,±13M,±14M
2 or 7	±4L,±6L,±10L,±12L±1M,±3M,±7M,±9M	±5L,±6L,±11L,±12L±2M,±3M,±8M,±9M	±4L,±5L,±10L,±11L±1M,±2M,±7M,±8M
3 or 8	±4L,±6L,±13L,±15L±1M,±3M,±10M,±12M	±5L,±6L,±14L,±15L,±2M,±3M,±11M,±12M	±4L,±5L,±13L,±14L±1M,±2M,±10M,±11M
4 or 9	±7L,±9L,±13L,±15L±4M,±6M,±10M,±12M	±8L,±9L,±14L,±15L±5M,±6M,±11M,±12M	±7L,±8L,±13L,±14L±4M,±5M,±10M,±11M
5 or 10	±1L,±3L,±7L,±9L±4M,±6M,±13M,±15M	±2L,±3L,±8L,±9L±5M,±6M,±14M,±15M	±1L,±2L,±7L,±8L±4M,±5M,±13M,±14M

The fundamental SVM algorithm is to select the appropriate switching states and calculate the duty cycle for each switching state during the switching period T_s. To achieve the desired output voltages and input currents, two adjacent switching states should be selected along with zero switching states. This combination will provide maximum output to input voltage transfer ratio. The output voltage and input current vectors can be synthesized by selecting the common switching states. The common switching states are ±10L,±12L,±7M,±9M and ±1L,±3L,±13M,±15M.

The two switching states with the same number with opposite signs, one state should be used based on the duty cycle sign. If the duty cycle is positive, then the positive switching states are used; otherwise, the negative switching states are used if it is negative. From Figures 4 and 5, the input voltage space vector phase angle is $0 \le \alpha_i \le (\pi/3)$ and the output voltage sector phase angle is $0 \le \alpha_0 \le (\pi/5)$. In this case, assume line voltage V_{AB} and $-V_{CA}$ are higher values. The large and medium vector configurations are used to obtain the $\overrightarrow{V'_0}$ is +10L,−12L,+7M and −9M and for $\overrightarrow{V''_0}$ is +1L,−3L,+13M and −15M. These configurations are associated with the vector directions adjacent to the input current vector positions. Table 1 represents the 60 switching combinations of large and medium vectors for different sectors [53].

Apply the SVM technique and solve the system equation at sector-1, the on-time ratio δ can be calculated for each configuration as

$$\begin{aligned}&\delta_{+10\mathrm{L}} \cdot |L| \cdot V_{ab} - \delta_{-12\mathrm{L}} \cdot |L| \cdot V_{ca} \\ &\quad + \delta_{+7\mathrm{M}} \cdot |M| \cdot V_{ab} - \delta_{-9\mathrm{M}} \cdot |M| \cdot V_{ca} = V'_0 \\ &\quad = \frac{5}{3}|\vec{V_0}| \cdot |L+M| \cdot \sin\left(\frac{\pi}{10} + \alpha_0\right)\end{aligned} \tag{12}$$

$$\delta_{+10\mathrm{L}} \frac{2}{\sqrt{3}} i_D = I'_i = |\overrightarrow{I'_i}| \frac{2}{\sqrt{3}} \sin\left(\frac{\pi}{6} - \left(\alpha_i - \frac{\pi}{6}\right)\right) \tag{13}$$

$$\delta_{-12\mathrm{L}} \frac{2}{\sqrt{3}} i_D = I''_i = |\overrightarrow{I'_i}| \frac{2}{\sqrt{3}} \sin\left(\frac{\pi}{6} + \left(\alpha_i - \frac{\pi}{6}\right)\right) \tag{14}$$

Table 2. Space vector switching sequence execution with commutation representation.

VECTOR NUMBER	SPACE VECTORS	OUTPUT PHASES				
		A	B	C	D	E
0	0/2	b	b	b	b	b
1	+7M/2	b	b	a	b	b
2	+13M/2	b	b	b	b	a
3	-10L/2	a	b	b	b	a
4	+1L/2	a	b	b	a	a
5	-3L/2	a	c	c	a	a
6	+12L/2	a	c	c	c	a
7	-15M/2	c	c	c	c	a
8	-9M/2	c	c	a	c	c
9	0	c	c	c	c	c
8	-9M/2	c	c	a	c	c
7	-15M/2	c	c	c	c	a
6	+12L/2	a	c	c	c	a
5	-3L/2	a	c	c	a	a
4	+1L/2	a	b	b	a	a
3	-10L/2	a	b	b	b	a
2	+13M/2	b	b	b	b	a
1	+7M/2	b	b	a	b	b
0	0/2	b	b	b	b	b

$$\delta_{+7\mathrm{M}}\frac{2}{\sqrt{3}}i_C = I_i' = |\overrightarrow{I'}_i|\frac{2}{\sqrt{3}}\sin\left(\frac{\pi}{6} - \left(\alpha_i - \frac{\pi}{6}\right)\right) \tag{15}$$

$$\delta_{-9\mathrm{M}}\frac{2}{\sqrt{3}}i_C = I_i'' = |\overrightarrow{I'}_i|\frac{2}{\sqrt{3}}\sin\left(\frac{\pi}{6} + \left(\alpha_i - \frac{\pi}{6}\right)\right) \tag{16}$$

Consider a balanced three-phase system. The sinusoidal nature supply voltage can be expressed as

$$\begin{aligned} V_{ab} &= |\overrightarrow{V_i}|\cos\alpha_i \\ V_{bc} &= |\overrightarrow{V_i}|\cos\left(\alpha_i - \tfrac{2\pi}{3}\right) \\ V_{ca} &= |\overrightarrow{V_i}|\cos\left(\alpha_i - \tfrac{4\pi}{3}\right) \end{aligned} \tag{17}$$

Now, generate $\overrightarrow{V'_0}$ and set the input current vector direction using configurations +10L,−12L and +7M,−9M.

$$\begin{aligned} \delta_{+10\mathrm{L}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|L|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}+\alpha_0\right)\cdot\sin\left(\frac{\pi}{3}-\alpha_i\right) \\ \delta_{-12\mathrm{L}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|L|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}+\alpha_0\right)\cdot\sin(\alpha_i) \\ \delta_{+7\mathrm{M}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|M|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}+\alpha_0\right)\cdot\sin\left(\frac{\pi}{3}-\alpha_i\right) \\ \delta_{-9\mathrm{M}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|M|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}+\alpha_0\right)\cdot\sin(\alpha_i) \end{aligned} \tag{18}$$

Now, generate $\overrightarrow{V''_0}$ and set the input current vector direction using configurations +1L,−3L and +13M,−15M.

$$\begin{aligned} \delta_{+1\mathrm{L}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|L|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}-\alpha_0\right)\cdot\sin\left(\frac{\pi}{3}-\alpha_i\right) \\ \delta_{-3\mathrm{L}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|L|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}-\alpha_0\right)\cdot\sin(\alpha_i) \\ \delta_{+13\mathrm{M}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|M|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}-\alpha_0\right)\cdot\sin\left(\frac{\pi}{3}-\alpha_i\right) \\ \delta_{-15\mathrm{M}} &= \frac{|\overrightarrow{V_0}|}{|\overrightarrow{V_i}|}\cdot|M|\cdot\frac{10}{3\sqrt{3}}\sin\left(\frac{\pi}{10}-\alpha_0\right)\cdot\sin(\alpha_i) \end{aligned} \tag{19}$$

The obtained results are valid only when $-(\pi/10) \le \alpha_0 \le (\pi/10)$ and for $0 \le \alpha_i \le (\pi/3)$. The on-time duty cycle ratios should be positive and the sum of duty cycle ratios must be lower than or equal to unity.

$$\begin{aligned} &\delta_{+10\mathrm{L}} + \delta_{-12\mathrm{L}} + \delta_{+1\mathrm{L}} + \delta_{-3\mathrm{L}} + \delta_{+7\mathrm{M}} \\ &\quad + \delta_{-9\mathrm{M}} + \delta_{+13\mathrm{M}} + \delta_{-15\mathrm{M}} \le 1 \end{aligned} \tag{20}$$

Some key points in this dual SVPWM control techniques are on-time duty ratio should be positive, some of the duty ratios must be lower than or equal to unity and a similar procedure should be followed for all sectors. In the case of three-phase to five-phase DMC, the maximum value of voltage transfer value can be determined as $q = 0.7886$.

5. Shoot-through insertion strategy

The conventional dual space vector modulation for QZSDMC was analysed and getting improved by distributing the shoot-through states. The shoot-through state analysis is based on the present 90 active states and 3 zero states. The DMC constrain is, the input side is never to be short-circuited. It will be overcome by connecting the QZS network at the input side of DMC. Now the input sides of DMC can safely short circuit and its acting in the shoot-through state with zero vectors. During non-shoot-through the state, the QZSDMC is working under normal mode or active vectors state. The importance of this technique is the sustainability of active vector states, zero vector states and shoots

V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_8	V_7	V_6	V_5	V_4	V_3	V_2	V_1	V_0
$T_0/4$	$T_1/2$	$T_2/2$	$T_3/2$	$T_4/2$	$T_5/2$	$T_6/2$	$T_7/2$	$T_8/2$	$T_0/2$	$T_8/2$	$T_7/2$	$T_6/2$	$T_5/2$	$T_4/2$	$T_3/2$	$T_2/2$	$T_1/2$	$T_0/4$
bbbbb	bbabb	bbbba	abbba	abbaa	accaa	accca	cccca	ccacc	ccccc	ccacc	cccca	accca	accaa	abbaa	abbba	bbbba	bbabb	bbbbb
STba	STab,STba	STab,STba	STba	STba	STbc	STac	STac	STca,STac	STac	STca	STac,STca	STca	STca	STcb	STab	STab	STba,STab	STab

Figure 6. Switching sequences for QZSDMC including shoot-through states with a dual space vector modulation scheme.

through states by efficiently reducing the switching time of bidirectional switches [54]. The duty ratio can be calculated as

$$\begin{aligned} T_1 &= d_{\alpha\mu} T_s = m \sin(36^\circ - \theta_{mi}) \sin(36^\circ - \theta_{mv}) T_s = T_5 \\ T_2 &= d_{\alpha\gamma} T_s = m \sin(\theta_{mv}) \sin(36^\circ - \theta_{mi}) T_s = T_6 \\ T_3 &= d_{\beta\mu} T_s = m \sin(36^\circ - \theta_{mv}) \sin(\theta_{mi}) T_s = T_7 \\ T_4 &= d_{\beta\gamma} T_s = m \sin(\theta_{mv}) \sin(\theta_{mi}) T_s = T_8 \\ T_{st} &= d_{st} T_s, \quad m = m_c m_v \\ T_0 &= 1 - T_1 - T_2 - T_3 - T_4 - T_5 - T_6 - T_7 - T_8 - T_{st} \end{aligned} \tag{21}$$

Table 2 represents the shoot-through vectors of a single output phase. Figure 6 shows the switching sequences for QZSDMC with a dual space vector modulation scheme. The dual SVPWM for QZSDMC can be implemented using eight space vectors for the particular vector. For the specific angular sector, the α_i and α_0 are calculated using phase angle, input line current and output line voltages. For getting the symmetrical switching waveform, the zero space vectors are effectively utilized in each switching cycle. To minimize the number of switching commutations, the switching sequences should be carefully utilized. The eight active switching states and one zero switching state should be ordered to reduce the number of switching commutations. Initially, the switching time T_s get equally halved. For symmetrical switching, zero vector is applied first and followed by active vectors to each half cycle. The mirror images of the switching sequences should be employed for each half cycle of the sampling period. The performance of QZSDMC was improved by adjusting the switching time using

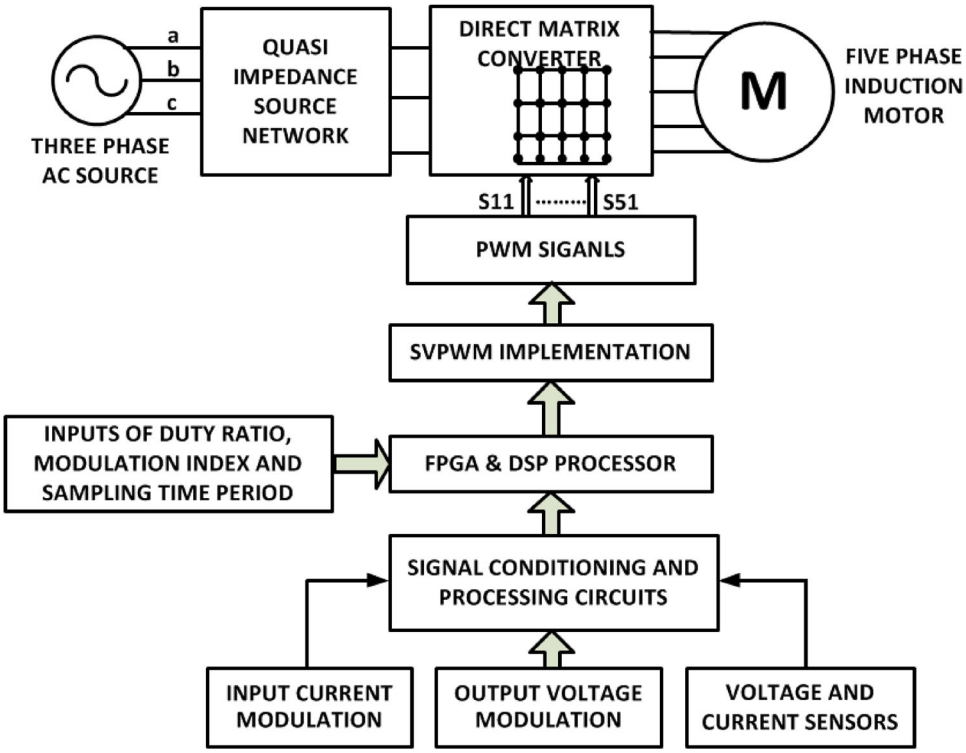


Figure 7. Schematic representation of simulation set-up.

Table 3. Maximum modulation index and voltage gain formulation.

Matrix converter configuration (N × K)	Maximum output to input formula	Maximum modulation index (%)	Maximum gain (G)
3 × 3	$\frac{1/(2\cos(\frac{\pi}{6}))}{\frac{2}{3}V_{dc}}$	86.66	$\frac{1/(2\cos(\frac{\pi}{6}))}{\frac{2}{3}V_{dc}} \times B$
3 × 5	$\frac{1/(2\cos(\frac{\pi}{10}))}{\frac{2}{3}V_{dc}}$	78.86	$\frac{1/(2\cos(\frac{\pi}{10}))}{\frac{2}{3}V_{dc}} \times B$
3 × 6	$\frac{1/(2\cos(\frac{\pi}{12}))}{\frac{2}{3}V_{dc}}$	77.65	$\frac{1/(2\cos(\frac{\pi}{12}))}{\frac{2}{3}V_{dc}} \times B$
3 × 7	$\frac{1/(2\cos(\frac{\pi}{14}))}{\frac{2}{3}V_{dc}}$	76.93	$\frac{1/(2\cos(\frac{\pi}{14}))}{\frac{2}{3}V_{dc}} \times B$
3 × 9	$\frac{1/(2\cos(\frac{\pi}{18}))}{\frac{2}{3}V_{dc}}$	76.15	$\frac{1/(2\cos(\frac{\pi}{18}))}{\frac{2}{3}V_{dc}} \times B$
5 × 3	$\frac{1/(2\cos(\frac{\pi}{6}))}{0.6472V_{dc}}$	89.21	$\frac{1/(2\cos(\frac{\pi}{6}))}{0.6472V_{dc}} \times B$
5 × 5	$\frac{1/(2\cos(\frac{\pi}{10}))}{0.6472V_{dc}}$	81.23	$\frac{1/(2\cos(\frac{\pi}{10}))}{0.6472V_{dc}} \times B$

shoot-through zero vectors. The switching time of active space vectors remains unchanged. It is observed that in each portion of the sampling period either one or two switching commutations are taking place and a total of 24 commutations are required for each sampling period.

6. Maximum modulation index and voltage gain formulation in N to K phase QZSDMC

The voltage gain of the QZSDMC is given by G = *BM*, where G is the voltage gain of QZSDMC, *B* is the boost factor for QZSDMC and *M* is the modulation index for QZSDMC. Table 3 shows the maximum modulation index formulation for N to K phase QZSDMC. The maximum output in the linear range can be getting for N to K phase QZSDMC as

$$\text{Maximum possible output in N to K QZSDMC matrix converter(G)} = \frac{\text{Maximum output in K phase QZS inverter in the linear range}}{\text{Length of the largest space vector of } n-\text{phase QZS inverter}} \times B \tag{22}$$

$$G = \frac{1/2\cos\left(\frac{pi}{2M}\right)}{\frac{2}{3}V_{dc}} \times B \tag{23}$$

7. Simulation results and discussions

The simulation work is supported to study the operation and performance of this converter in the whole range of operations. The suggested modulation scheme for QZSDMC provides excellent performance in all the operating regions. The MATLAB/Simulink platform is used to develop the simulation model by using the library block of the simpowersystem.

The block diagram representation of the suggested PWM is presented in Figure 7. The MatLab/Simulink

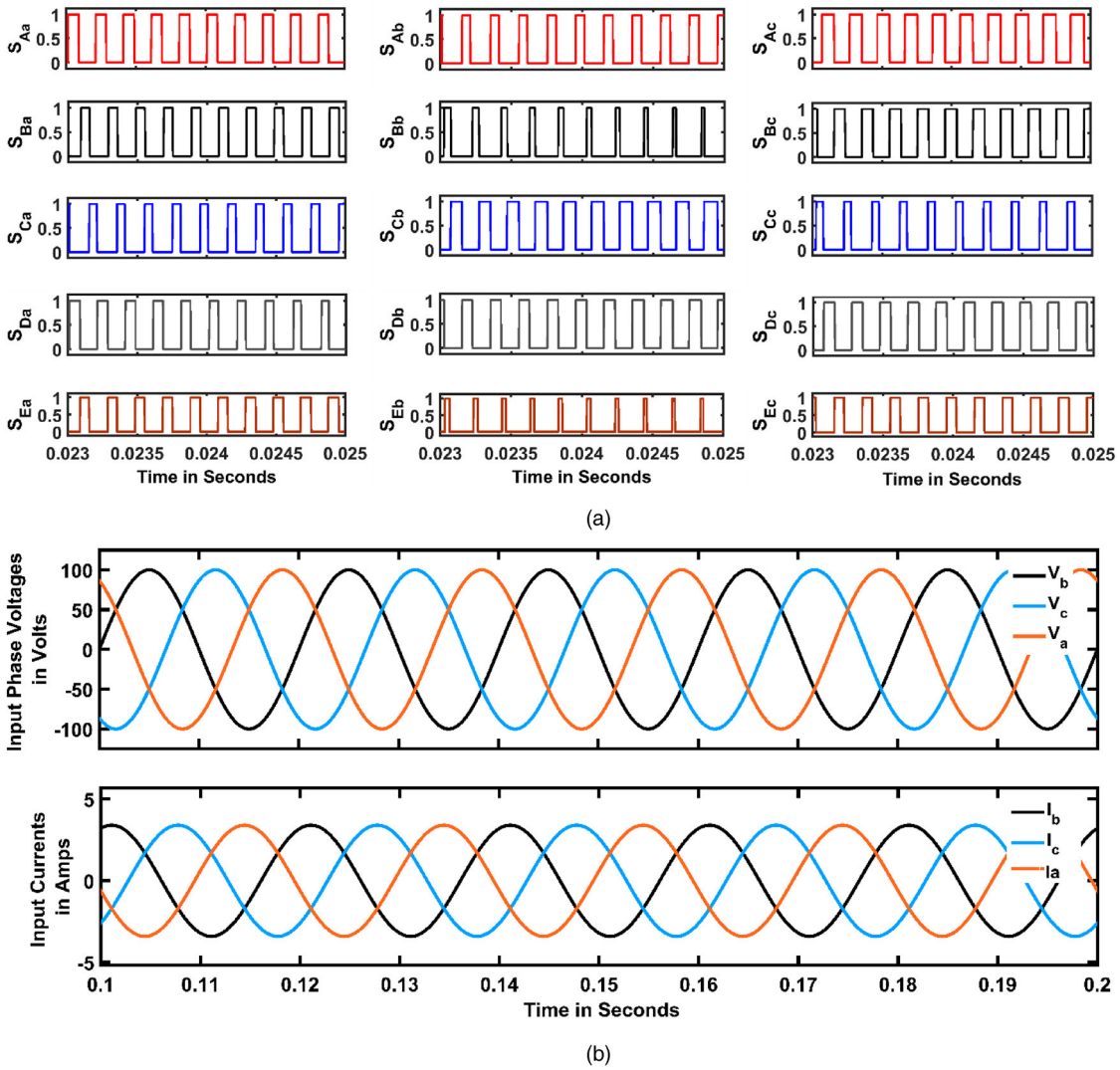
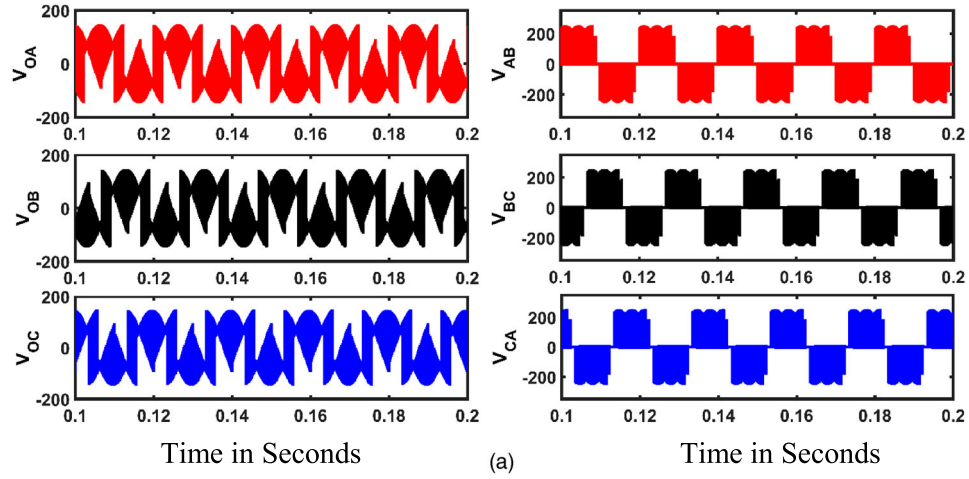
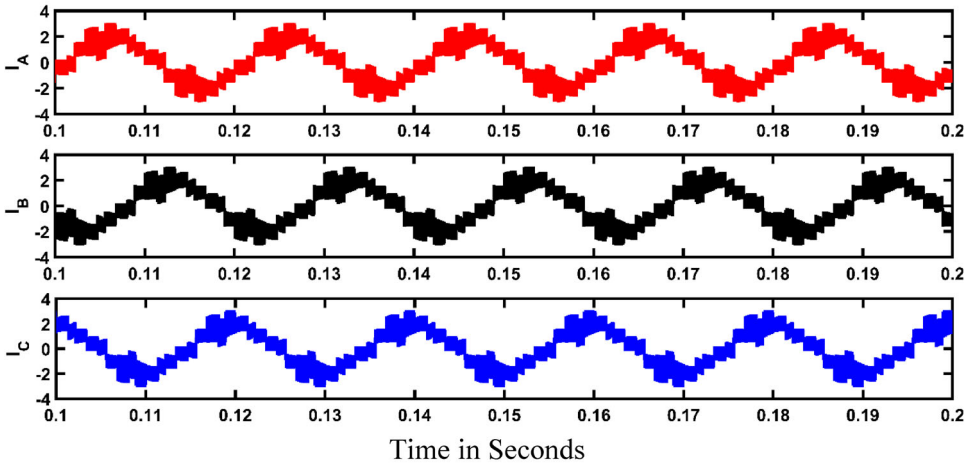


Figure 8. (a) Controlled switching signals generated by a dual SVPWM control technique for each leg. (b) Three-phase input voltages and current for 3φ to 5φ QZSDMC with frequency 50 Hz.



(a)



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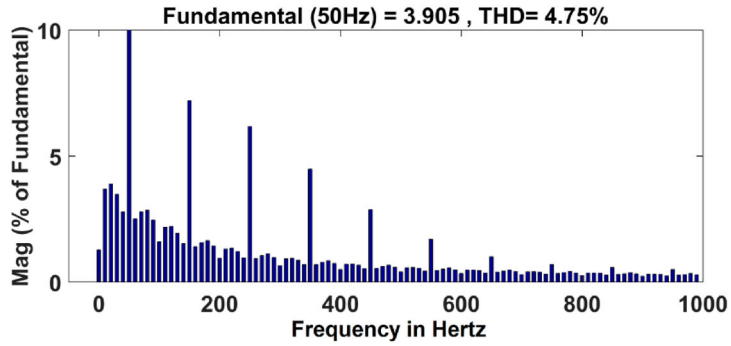

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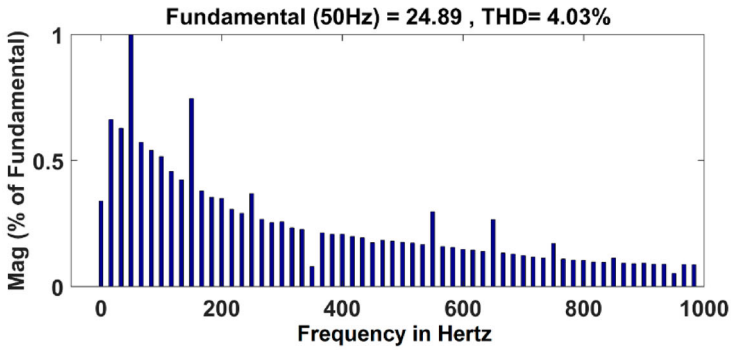


(d)

Figure 9. (a) Three-phase output phase voltages and line voltages at frequency 50 Hz. (b) Three-phase output load currents at frequency 50 Hz. (c) Output voltages THD of three-phase to three-phase QZSDMC. (d) Output current THD of three-phase to three-phase QZSDMC.

Table 4. MatLab simulation and experimental parameters consideration.

Parameters	Values
AC input line-to-ground RMS voltage, V_i	100 V
AC input current, I_i	3.3 A
AC input voltage frequency, f_i	50 Hz
QZS network inductance, L	1.5 mH
QZS network capacitance, C	330 µF
QZSDMC switching frequency, f_s	5000 Hz
AC output line-to-ground RMS voltage, V_o	147 V
AC output line current, I_o	2.2 A
AC output voltage frequency, f_o	50 Hz
Modulation index, M	0.66
Shoot-through duty ratio, D_0	0.34
Power factor, cosφ	0.955
Simulation step size	10 µs
R-Load connected to the QZSDMC	100 Ω
L-Load connected to the QZSDMC	10 mH

environment is used to validate the proposed dual space vector PWM for QZSDMC. Also, the viability of the design is checked by constructing the experimental prototype. Table 4 represents the parameters chosen for various elements used in simulation and real-time hardware equipment. In the simulation part, the QZSDMC waveforms are validated by comparing them with normal DMC waveforms. Figure 8(b) shows the input phase voltages with a magnitude of 100 V, 50 Hz frequency. Assume 0.66 as modulation index M_0 and 0.34 as shoot-through duty ratio D_0. Figure 9(a,b) shows the output five-phase voltages of 145 V (RMS) and 2.45 A load current. The calculated gain of QZSDMC is 2.05. This gain value represents the relationship between output voltages concerning input voltages, i.e. the output voltage is 2.05 times of input voltages with a cut-off frequency of 5 kHz.

Theoretically, the boost factor B is calculated as 3.125 with a maximum voltage gain of 2.06. Using these parameters, the period for shoot-through duty ratio can be calculated as 0.34 which is the same as the theoretical value. The simulation results for the conventional DMC show the output phase voltages of 86.65 V (RMS). It represents the voltage transfer ratio of conventional DMC is only 0.866 which is less than the voltage transfer capability of QZSDMC. Also, the sinusoidal nature with continuous input current waveforms can be getting from QZSDMC. On the other side, the input current flows through the conventional DMC has pulsating current with higher harmonics voltage and current as shown in Figure 9(c,d).

Figure 10 shows the five-phase output voltage and current waveforms with harmonics representations getting from the 3φ to 5φ QZSDMC with the input voltages of 100 V peak at frequency 50 Hz. The 3φ to 5φ QZSDMC has the capability of producing various output voltages and frequencies like 25, 75 and 100 Hz. From Figures 11–16, the researcher can observe the inbuild wide range voltage gain capability of QZSDMCS with more than three phases. From the proposed converter, the following points are proven clearly. A wide range

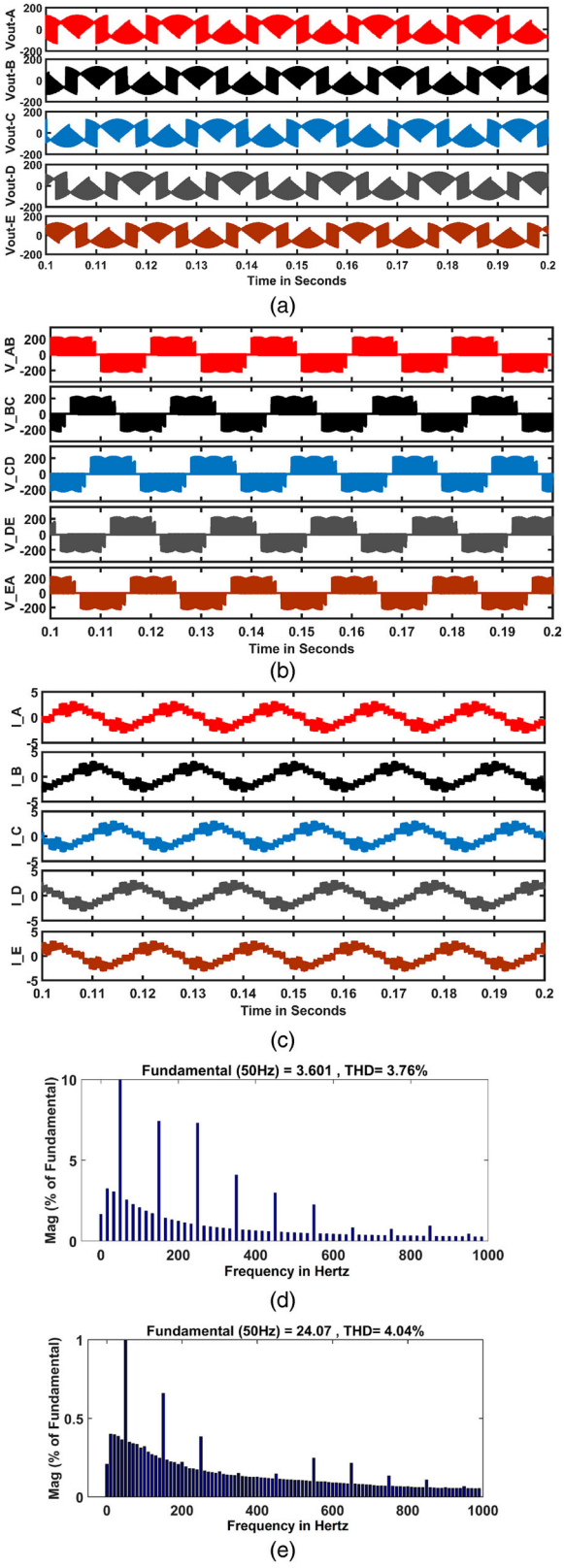
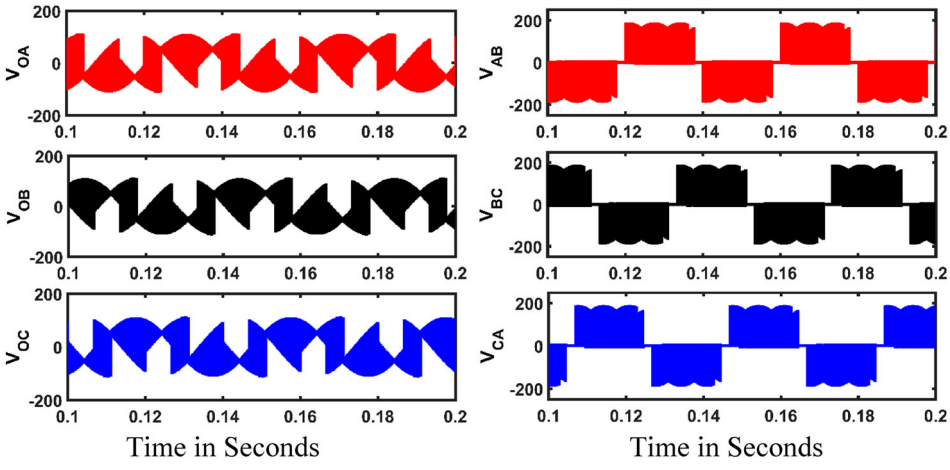
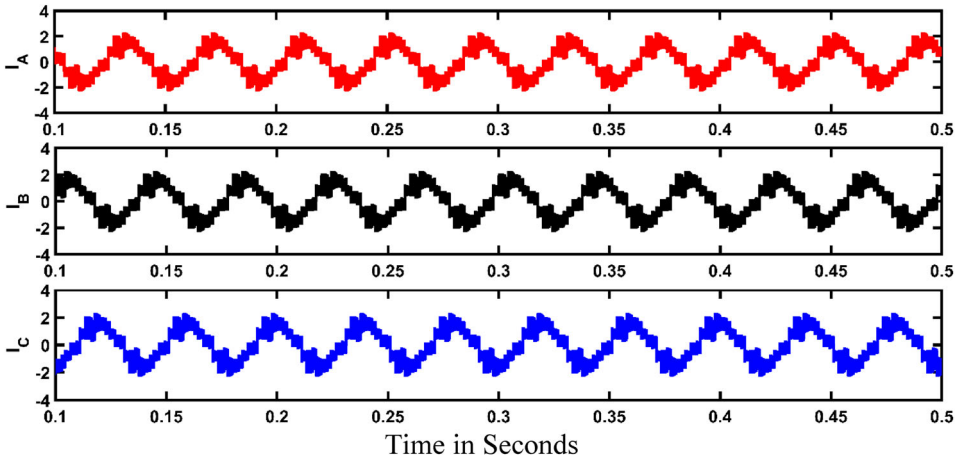


Figure 10. (a) Five-phase output phase voltages at frequency 50 Hz. (b) Five-phase output line voltages at frequency 50 Hz. (c) Five-phase load currents at frequency 50 Hz. (d) Output voltages THD of three-phase to five-phase QZSDMC. (e) Output current THD of three-phase to five-phase QZSDMC.

of voltage gain, sinusoidal nature of input current with less THD, minimum usage of power switches compared with back-to-back connected multiphase voltage source



(a)



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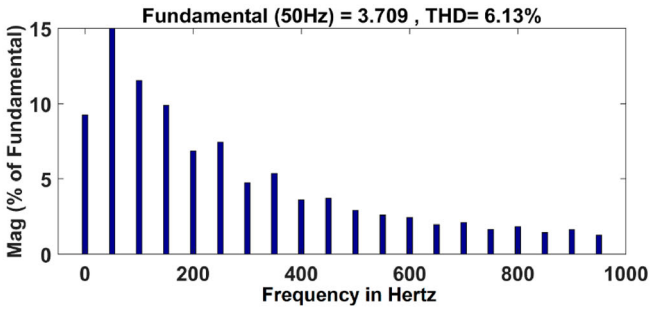

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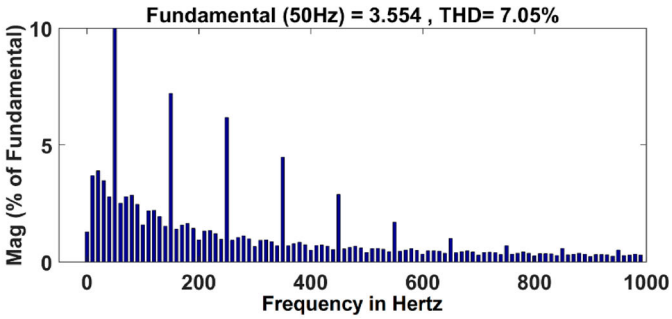


(d)

Figure 11. (a) Three-phase output phase voltages and line voltages at frequency 25 Hz. (b) Three-phase output load currents at frequency 25 Hz. (c) Output voltages THD of three-phase to three-phase QZSDMC. (d) Output current THD of three-phase to three-phase QZSDMC.

inverter and the input filter elimination. As per the control law, the output pattern for controlling the output voltage is directly derived and these control signals are given to the switches as shown in Figure 8(a).

Figures 10–16 show the voltage THD and current THD of conventional DMC and 3φ to 5φ QZSDMC. From that Figures 10–16, the observation taken as THD of 3φ to 5φ QZSDMC is less than the THD of conventional DMC by the percentage of 2.5. The voltage THD and current THD of 3φ to 5φ QZSDMC are 3.76 and 4.04%, respectively, and the voltage THD and current THD of conventional DMC are 4.76 and 4.03%, respectively, with a frequency 50 Hz. These THD tolerance limits are specified within the IEEE19-1999 standards. Table 5 shows the consolidated observation getting from Figures 9–16 like input voltage, output phase voltages, output line voltages, load currents, voltage harmonics and current harmonics of both three-phase output, and five-phase output of dual SVPWM-based QZSDMC with 25, 50, 75 and 100 Hz.

The proposed experimental prototype set-up structure is shown in Figure 17. The experimental results are used to validate the proposed concepts of the dual space vector PWM technique for 3φ to 5φ QZSDMC. These experimental results are helpful to analyse and justify the theoretical concepts, reliability, and ease of digital implementation. Hence, the proposed direct ac–ac converter can be used for the wide range of speed control for multiphase drive systems. The schematic blocks for the experimental set-up are as shown in Figure 17. Figure 18 represents the experimental set-up of a three-phase to five-phase quasi Z-source direct matrix converter. The IXYS-based FIO50-12BD bidirectional switches-based power modules are used to compose the required experimental prototype set-up. It's an ISOPLUS i4-PAC consisting of fast diode bridges and diagonally connected IGBTs. The IGBTs and diode bridges have the voltage blocking capability of 1200 V and the current-carrying capability of each device are 50 A.

This module is available in the market as a single chip with five output pins. Among the five output pins, four pins are used to diode bridges, and one pin is used to IGBT gate drive circuit. Using the single control signal, the bidirectional current flow can be controlled by a single chip module. The QZSDMC consists of 27 bidirectional power switches among that 18 switches are effectively utilized. The spartan 3-A DSP controller and Xilinx XC3SD1800A FPGA are used to generate the control signals for bidirectional switching devices. The FPGA board consists of logic gates, A/D and D/A conversion processors, gate drive signal generator and modulation code processor. The FPGA board has the capability of handling the PWM signals up to 50. The entire power module circuit is protected using damping diode circuits.

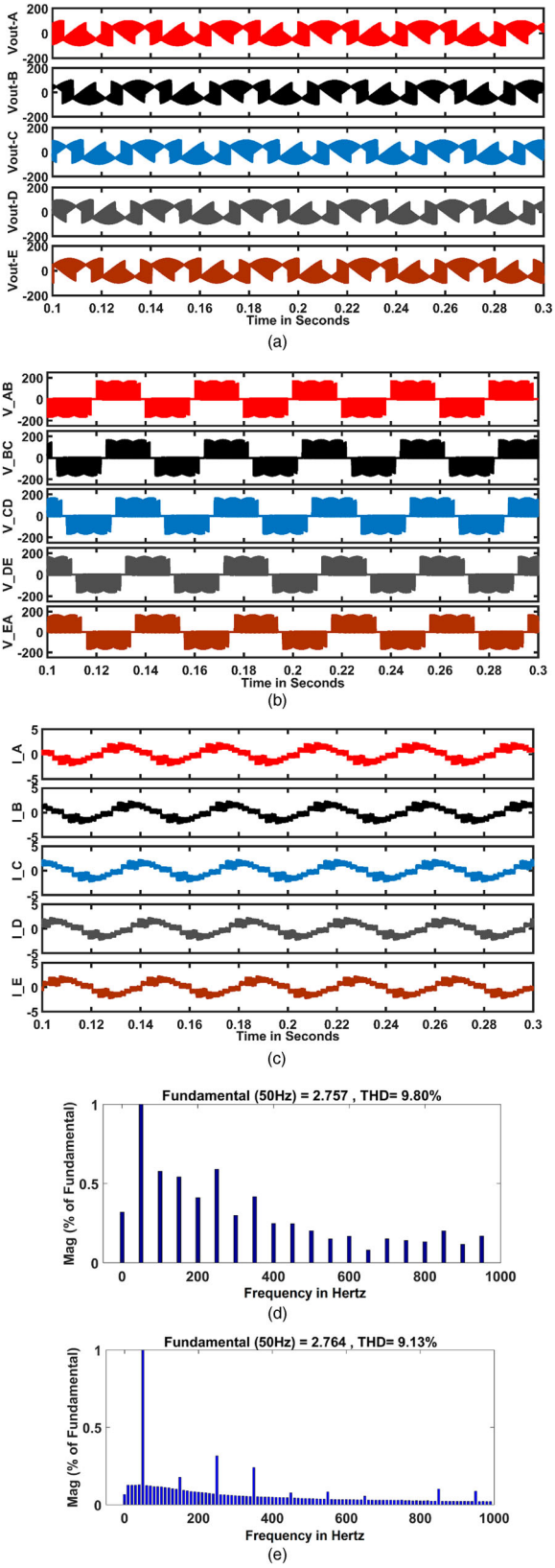
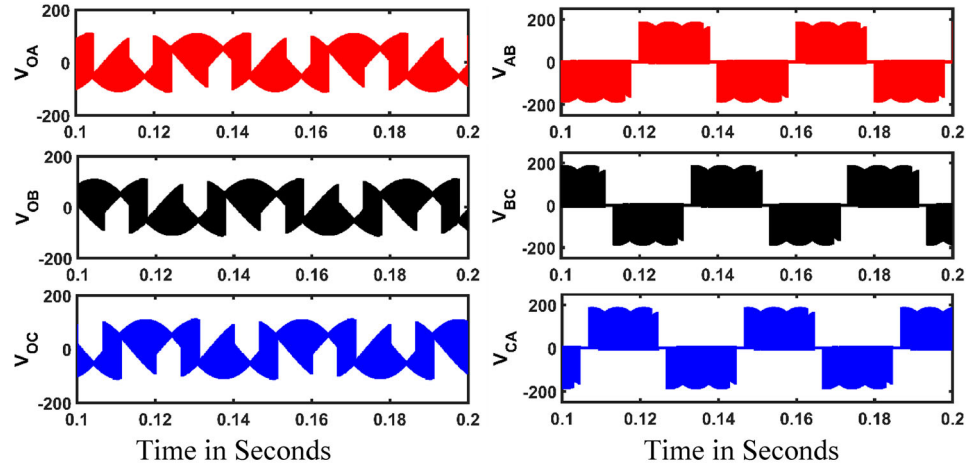
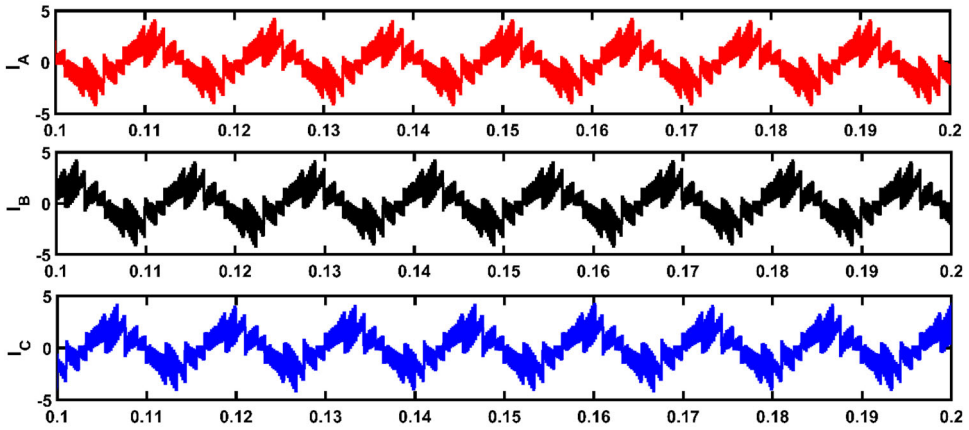


Figure 12. (a) Five-phase output phase voltages at frequency 25 Hz. (b) Five-phase output line voltages at frequency 25 Hz. (c) Five-phase output load currents at frequency 25 Hz. (d) Output voltages THD of three-phase to five-phase QZSDMC. (e) Output current THD of three-phase to five-phase QZSDMC.

The autotransformer is used to provide the input power supply of 100 V, 50 Hz, 3phase AC power. The QZSDMC is made of bidirectional switches with a



(a)



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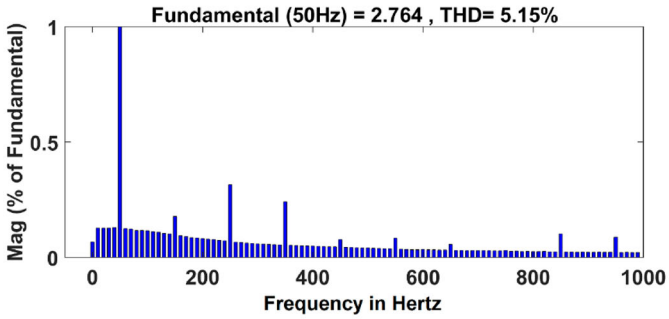

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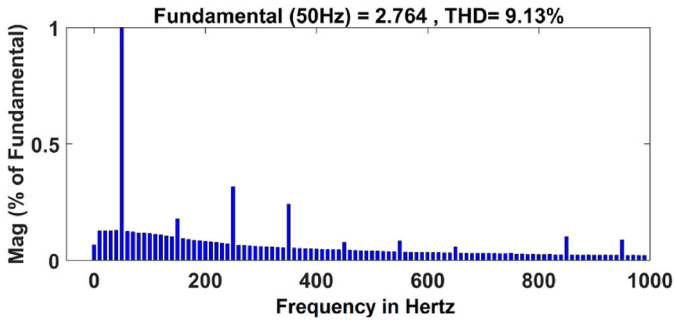


(d)

Figure 13. (a) Three-phase output phase voltages and line voltages at frequency 75 Hz. (b) Three-phase output load currents at frequency 75 Hz. (c) Output voltages THD of three-phase to three-phase QZSDMC.(d) Output current THD of three-phase to three-phase QZSDMC.

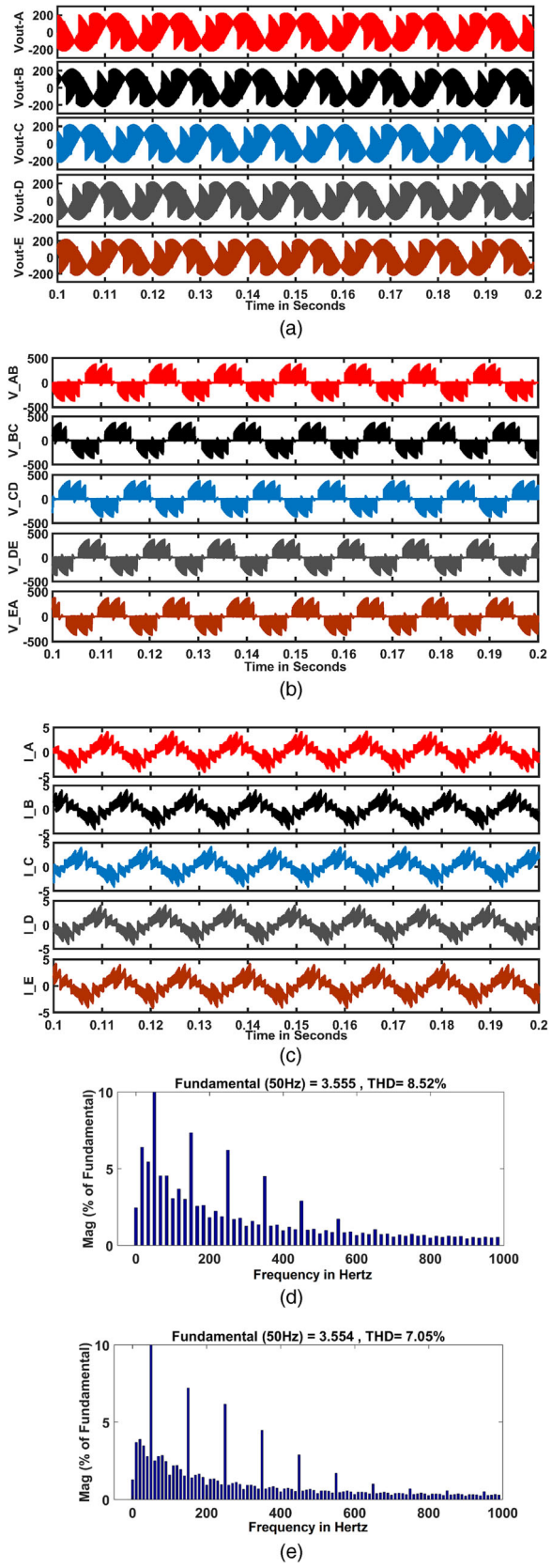


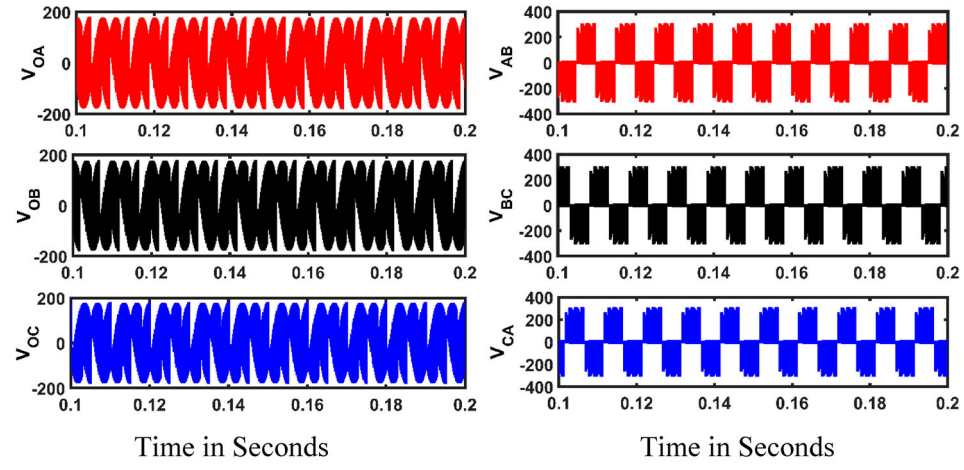
Figure 14. (a) Five-phase output phase voltages at frequency 75 Hz. (b) Five-phase output line voltages at frequency 75 Hz. (c) Five-phase output load currents at frequency 75 Hz. (d) Output voltages THD of three-phase to five-phase QZSDMC. (e) Output current THD of three-phase to five-phase QZSDMC.

switching frequency of 5 kHz. Table 4 represents various input side parameters, filter parameters and output side load parameters. Figure 19(a) shows 3φ to 5φ QZSDMC resulting output per phase voltage waveforms with the fundamental frequency of 25, 50, 75 and 100 Hz. Figure 19(b) shows 3φ to 5φ QZSDMC resulting output per line voltage waveforms with the fundamental frequency of 25, 50, 75 and 100 Hz. Figure 19(c) shows the resulting output per phase current waveforms with the fundamental frequency of 25, 50, 75 and 100 Hz. Figure 19(d) shows 3φ to 5φ QZSDMC experimental output voltage of 145 V (RMS) with the operating frequency of 25, 50, 75 and 100 Hz. In general, Figure 19 shows 3φ to 5φ QZSDMC experimental sample output phase voltage, line voltage, load current of 3.3 A with the operating frequency of 25, 50, 75 and 100 Hz. Referring to Figure 9, the output voltage and output current of conventional DMC are limited to 86.667 V (RMS) and 2.8 A. From the experimental results, the observation is taken as voltage gain of 3φ to 5φ QZSDMC is superior to the conventional DMC. The reason behind the increased voltage gain of 3φ to 5φ QZSDMC is the distribution of shoot-through states evenly without changing the active states. Figure 19 shows the output phase voltage waveforms are adjusted in-phase with the output load currents. It means the unity power factor is maintained at the load side.

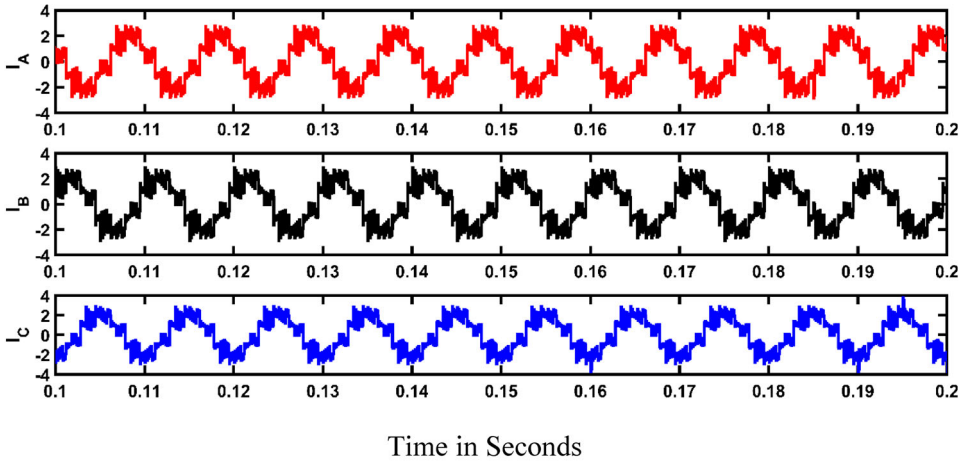
Thus, the dual space vector control and modulation algorithm-based QZSDMC hardware results validate its performance better than the conventional DMC. Figure 20 represents the step-by-step procedure of experimental validation in a flowchart form. The implementation of a dual SVPWM control scheme for 3φ to 5φ QZSDMC was represented clearly. Table 6 shows the comparative evaluation of simulated results with the experimental prototype results. Most of the measured results are equating to the theoretical results via simulation. The main constraints followed in the experimental set-up are non-ideal parameters of inductors and capacitors. As a result, unpredicted voltage drops arise across the power devices and inductors. So the expected voltages of the QZS network are less than the simulated output voltages.

The experimental results mostly coincide with the simulation results to a good extent. Figures 21–24 show an input voltage and current THDs with output voltage and current THDs. The output voltage and current THDs of 3φ to 5φ QZSDMC are 3.76 and 4.04%, respectively. The three-phase input voltage and current THDs are 4.76 and 4.03%, respectively. This result shows the superior performance of 3φ to 5φ QZSDMC with the proposed dual space vector PWM technique. Further at the input side, the current is in phase with the voltage waveforms. The beauty of the proposed converter is prooved by maintaining the unity power factor at the input side.

The prototype module uses bidirectional switches. The major advantage is the utilization of a minimum number of IGBT switches for multiphase operation.



(a)



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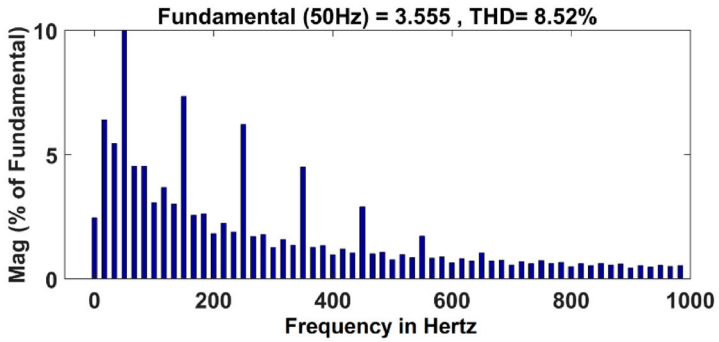

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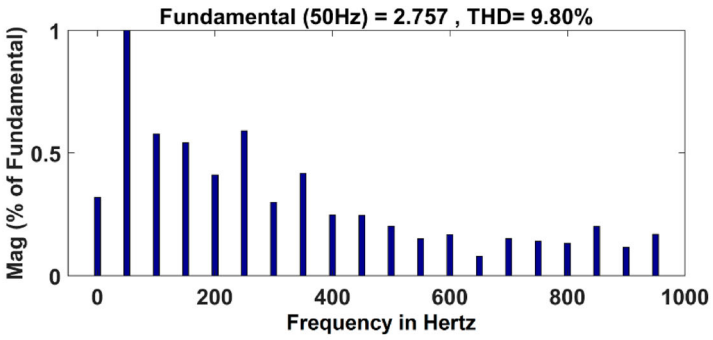

(d)

Figure 15. (a) Three-phase output phase voltages and line voltages at frequency 100 Hz. (b) Three-phase output load currents at frequency 100 Hz. (c) Output voltages THD of three-phase to three-phase QZSDMC. (d) Output current THD of three-phase to three-phase QZSDMC.

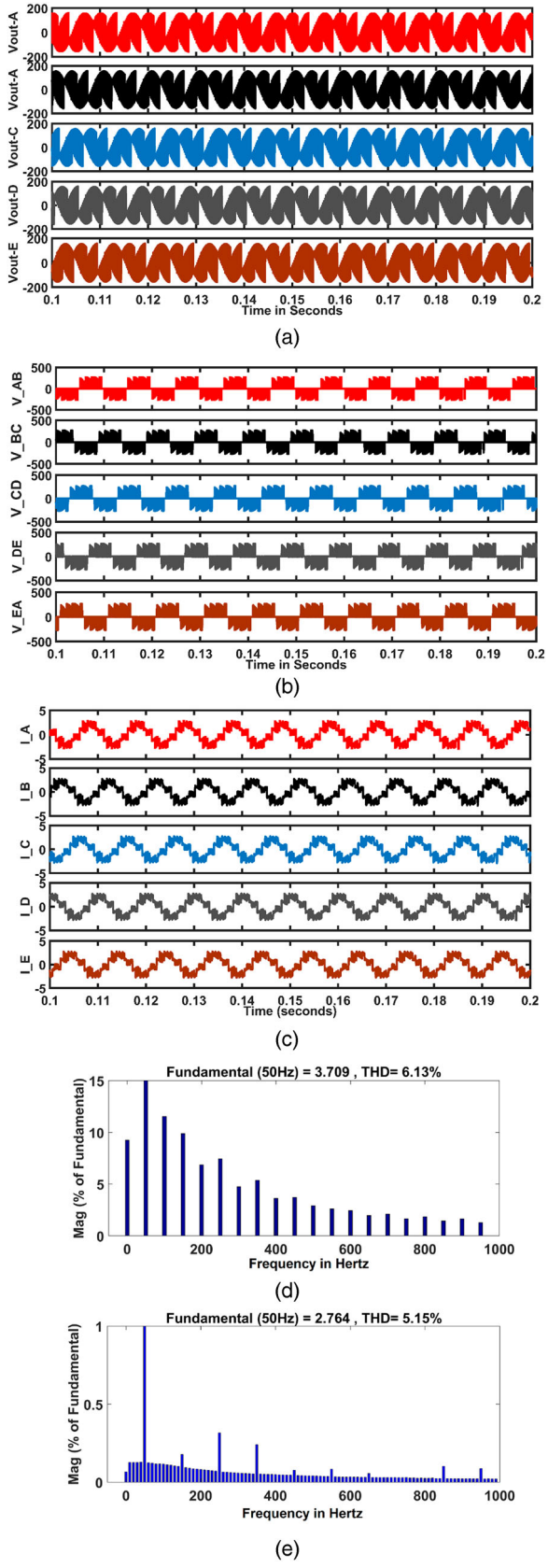

Figure 16. (a) Five-phase output phase voltages at frequency 100 Hz. (b) Five-phase output line voltages at frequency 100 Hz. (c) Five-phase output load currents at frequency 100 Hz. (d) Output voltages THD of three-phase to five-phase QZSDMC. (e) Output current THD of three-phase to five-phase QZSDMC.

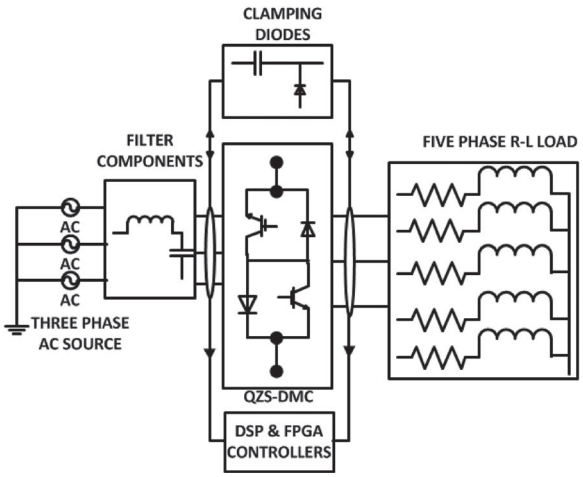

Figure 17. Structure of experimental prototype set-up experimental results and discussions.

The considerable disadvantages are higher conduction losses, two-step commutation, usage of extra line inductance for safe operation, overlapping of current during commutation, and the requirement of clipping circuits and snubbers for dead time compensations. The testing of developed QZSDMC is done over a wide range of fundamental frequencies.

Table 7 shows the comparison of ZSDMC, discontinuous and continuous QZSDMC AC–AC converter topologies. From the comparison, it is ensured that the QZSDMC offers a high voltage boost ratio, good waveform quality, lesser capacitor voltage stress and continuous input current. The simulation and the investigational results of the prototype verify the feasibility of the suggested QZSDMC topology and its control strategy. Comparing the hardware results with the simulation results, that show the proposed modulation scheme for QZSDMC provides better results at all the fundamental frequencies.

Table 8 shows the comparison of direct duty ratio PWM technique with various classic modulation techniques like Alesina-Venturini modulation technique, Carrier PWM Technique, SVPWM Technique, Simple Boost Modulation Method, Constant Boost Modulation Method and Maximum Constant Boost Modulation Method. This comparison is based on the current and voltage THD getting from each method at different operating frequencies of the QZSDMC. At the operating frequency = 25 Hz, the SVPWM technique-based QZSDMC generated the voltage and current harmonic distortion of 6.9 and 7.3%, respectively. Whereas the DDR-based PWM technique generates the voltage and current harmonic distortion of 9.52 and 10.62%, respectively. The remaining modulation techniques are producing more THD in the mentioned operating frequency. At the operating frequency = 50 Hz,

Table 5. Output parameters of dual SVPWM-based QZSDMC with different frequencies.

	3φ to 3φ QZSDMC				3φ to 5φ QZSDMC			
Parameters	25 Hz	50 Hz	75 Hz	100 Hz	25 Hz	50 Hz	75 Hz	100 Hz
Input voltage (V)	100	100	100	100	100	100	100	100
Input current (A)	3.3	3.3	3.3	3.3	3.3	3.3	3.3	3.3
Output phase voltage (V)	143	145	146	148	140	144	145	143
Output line voltage (V)	243	245	244	246	240	244	243	241
Load current (A)	2.75	2.8	2.6	2.5	2.1	2.2	2.3	2.15
Voltage THD (%)	6.13	4.75	5.15	8.52	9.8	3.76	8.52	6.13
Current THD (%)	7.05	4.03	9.13	9.8	9.13	4.04	7.05	5.15

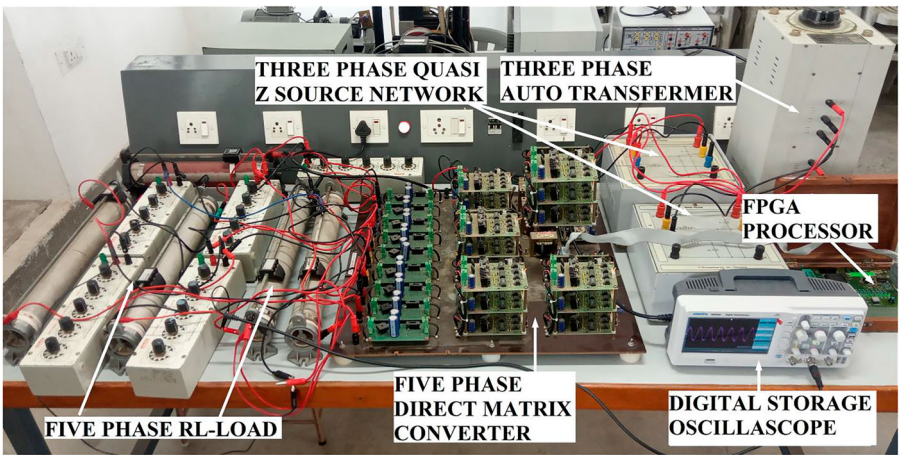

Figure 18. Experimental set-up of a three-phase to five-phase quasi Z-source direct matrix converter.

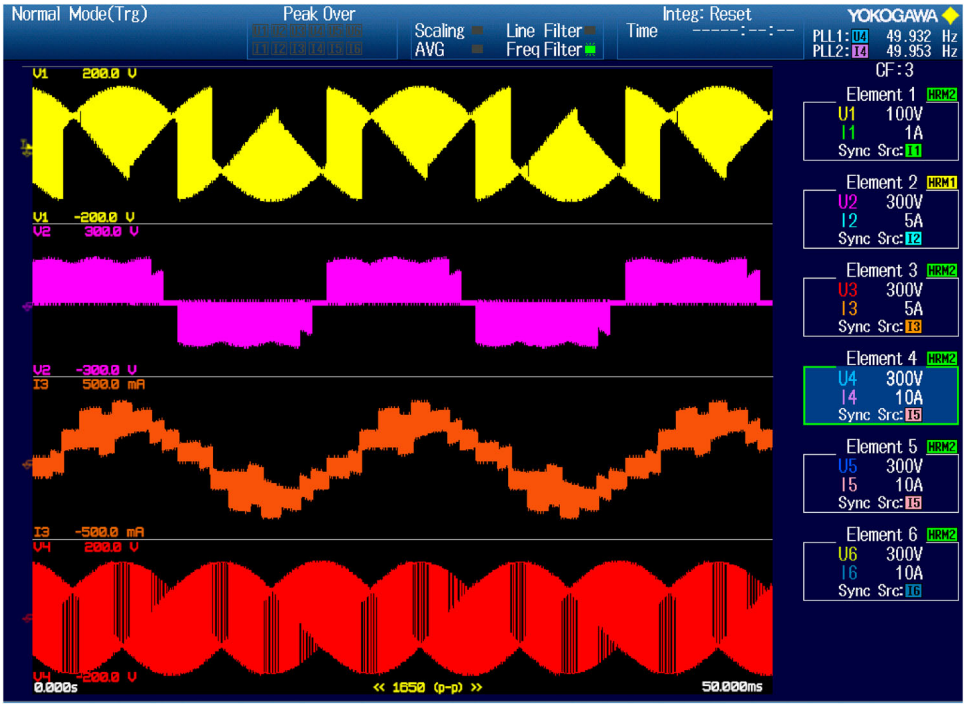

Figure 19. Experimental per phase result of a three-phase to five-phase quasi Z-source direct matrix converter.

the SVPWM technique-based QZSDMC generating the voltage and current harmonic distortion of 3.5 and 4.2%, respectively. Whereas the DDR-based PWM technique generates the voltage and current harmonic distortion of 4.7 and 6.7%, respectively. The remaining modulation techniques are producing more THD in the mentioned operating frequency [55].

At the operating frequency = 75 Hz, the SVPWM technique-based QZSDMC generated the voltage and current harmonic distortion of 5.8 and 6.3%, respectively. Whereas the DDR-based PWM technique generates the voltage and current harmonic distortion of 7.3 and 7.5%, respectively. The remaining modulation techniques are producing more THD in the

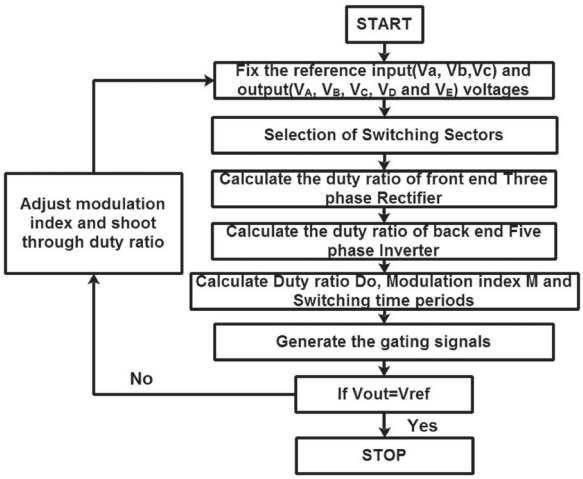

Figure 20. Flowchart for experimental validation of control scheme employed in QZSDMC.

Table 6. Comparison between simulation and experiment results of QZSDMC.

Parameters of QZSDMC	Simulated results	Experimental results
Input phase voltage (V) (RMS voltage)	100	100
Output phase voltage (V) (RMS voltage)	145	141
Output line voltage (V) (RMS voltage)	245	241
Output current (A)	2.8	2.2
Boost factor	3.125	2.95
Shoot-through duty ratio	0.34	0.33
Voltage gain	2.05	1.97

Figure 21. Experimental input current THD of 4.03%.

Figure 22. Experimental input voltage THD of 4.76%.

Figure 23. Experimental output voltage THD of 3.76%.

Figure 24. Experimental output current THD of 4.04%.

mentioned operating frequency. At the operating frequency = 100 Hz, the SVPWM technique-based QZSDMC generates the voltage and current harmonic distortion of 3.9 and 4.5%, respectively. Whereas the DDR-based PWM technique generates the voltage and current harmonic distortion of 4.7 and 6.7%, respectively. The remaining modulation techniques are producing more THD in the mentioned operating frequency.

The comparison represented in Figure 25 represents the performance of each technique implemented in ZSDMC concerning its voltage and current THD values. The comparison figure shows that the proposed modulation technique is better than the classic modulation techniques which are prosed to the various Z-source matrix converter [55].

8. Conclusion

In this paper, the dual space vector pulse width modulation control technique was proposed to three-phase to five-phase QZSDMC. Here, the input is three-phase, while the output is five-phase. A five-phase motor drive

Table 7. Quantitative comparison of direct and indirect QZSDMC with discontinuous and continuous mode operations.

Parameters	ZSDMC	Discontinuous QZSDMC	Continuous QZSDMC	Discontinuous QZSIDMC	Continuous QZSIDMC
Total number of inductors and capacitors required	09	15	12	27	27
Additional input LC	Yes	Yes	No	Yes	No
Ripples in Current	High	Low	Low	Low	Low
Ripples in Voltage	Low	High	Medium	High	Medium
Stresses in Inductor current	Low	High	Medium	High	Medium
Stresses in Capacitor voltage	Medium	Low	High	Low	High
Gain	Low	High	High	High	High
THD of input current	Medium	High	Low	High	Low
THD of output voltage	High	Medium	Low	Medium	Low
Required current rating of element	Low	High	Medium	High	Medium
Required voltage rating of the element used	Medium	Low	High	Low	High
Losses	Medium	High	Low	High	Low
Efficiency	High	Low	High	Low	High

application can effectively utilize this type of converter. In the proposed dual SVPWM technique, 93 active space vectors are utilized from the possible 243 switching space vectors. For one sampling period, utilization of active vectors, zero vectors, 24 commutations and symmetrical switching of each half period is obtained. The proposed QZSDMC topology was consisting of a three-phase QZS network with five-phase DMC. The restrictions of voltage transfer ratio in the conventional DMC were overcome by 3φ to 5φ QZSDMC. In this paper, the proposed dual SVPWM technique was discussed in detail. The limitation associated with the conventional DMC at linear modulation is voltage gain. The attained voltage boost capability of the proposed QZSDMC is 1.97. In the absence of extra input filters, the voltage gain attainment is greater than unity. The experimental prototype set-up was fabricated to verify the simulation results. Both results are investigated and justified in detail. The simulation and hardware results show the maximum boost output voltage of 145 V (RMS) with a voltage gain of 1.97 and a shoot-through duty ratio of 0.33. By doing a comparison between 3φ to 5φ QZSDMC with conventional DMC, the voltage transfer capability was observed as 1.97 and 0.8667, respectively. The major advantages of the proposed converter are continuous input and output currents during any phase fault, nearly unity power factor at both sides, absence of bulky input LC filters and low input current THD as well as low output voltage THD. In the motor drive applications and the renewable energy applications, the occupation of conventional DMC can be replaced by the proposed 3φ to 5φ QZSDMC with its promising dual space vector PWM control technology. In the future, the performance of the proposed converter under the over modulation region in the SVPWM technique can investigate, the effects of fault tolerance, stability and performance variation during any one phase fault condition can analyse, the performance of proposed modulation schemes for multiphase to three-phase energy conversion systems applied for wind energy systems can investigate, a quasi-impedance source-based multiphase multilevel matrix converter for changing the energy capture and improve the performance of wind energy conversion systems can develop, this converter topology in wind energy conversion system to maintain constant voltages and frequency at load side from continuous variations in the wind speeds can apply, different topologies with improved impedance source network such as T-network could be used to multiphase QZSDMC and the

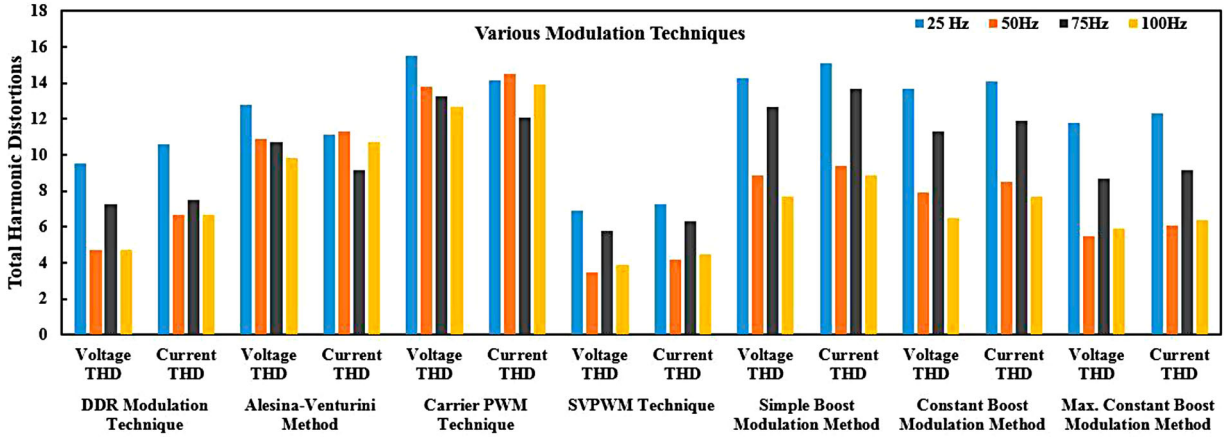

Figure 25. Comparison of voltage THD and current THD generation by QZSDMC for various classic PWM techniques.

Table 8. Comparison of THD generation by various modulation techniques.

Converter operating frequencies	DDR modulation technique		Alesina-Venturini method		Carrier PWM technique		SVPWM technique		Simple boost modulation method		Constant boost modulation method		Max. constant boost modulation method	
	Voltage THD %	Current THD %	Voltage THD %	Current THD %	Voltage THD %	Current THD %	Voltage THD %	Current THD %	Voltage THD %	Current THD %	Voltage THD %	Current THD %	Voltage THD %	Current THD %
25 Hz	9.52	10.62	12.8	11.15	15.5	14.19	6.13	7.05	14.29	15.1	13.67	14.1	11.8	12.3
50 Hz	4.7	6.7	10.9	11.3	13.8	14.5	4.75	4.03	8.9	9.4	7.9	8.5	5.5	6.1
75 Hz	7.3	7.5	10.7	9.2	13.3	12.1	5.15	9.13	12.7	13.7	11.3	11.9	8.7	9.2
100 Hz	4.7	6.7	9.8	10.7	12.7	13.9	8.52	9.8	7.7	8.9	6.5	7.7	5.9	6.4

performance evaluation of multiphase motor drive fed by multiphase matrix converter with the proposed control algorithm can evaluate. These are all wide range of areas for the proposed matrix converter can work for better future extraction.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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