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Encapsulated 3Ø converter for power loss minimization in a grid-connected system

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ABSTRACT

A newly designed DC–AC three phase bidirectional converter (DATBC) with an encapsulated DC–DC converter (EDC) for the energy storage system (ESD) is analysed and investigated in this research paper. By using encapsulated or embedded or hidden DC–DC converter a stable and constant DC bus is developed between the encapsulated DC–DC converter and DC–AC three phase bidirectional converter. The proposed converter is entirely different from the traditional dual-stage DC–AC converter, because it takes less than 20% of power used for the DC–AC conversion process. So, this reduced power consumption increases efficiency to a considerable value. A new control technique for zero sequence has been adopted components are inserted in the modulating signal based on carrier pulse width modulation (CPWM). Working principle, implementation and characteristics of the DC–AC three phase bidirectional converter are analysed. Effectiveness and feasibility of the developed converter are examined with a proto-type model.

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KEYWORDS
DC–AC three phase bidirectional converter; energy storage system; encapsulated DC–DC converter; carrier pulse width modulation

1. Introduction

Renewable energy source connected grid, energy storage system and electric vehicles are based on DC–AC three phase bidirectional converters [1,2]. Uninterrupted power supply and microgrid are the other applications which are using these types of converters [3,4]. Dual-stage conversion of the DC–AC converter consists of the DC–AC converter with a DC–DC converter which are the two stage conversion which can perform the inverter/rectifier operation, the block diagram of which is shown in Figure 1.

Level of voltage in ESD is less and varies in a wide range with state of charge variation [5]. The dual stage DC–AC converter maintains the DC bus voltage as stable and constant for the inversion stage. Whatever may be ESD voltage, the converter voltage is maintained to be constant. Due to dual stage operation, overall power is utilized and due to more power consumption, conversion efficiency is low [6,7]. On the other side both stages are completely based on full power, overall size, cost, and consumption of power which are the major drawbacks of the conventional DSDA converter [8,9]. Several researchers tried to improve the overall efficiency by changing the topology design [10,11]. Modulation is made with different control strategies for this DC–AC conversion [12,13]. Lot of techniques have been adopted to improve power management in the dual-stage DC–AC converter [14,15]. The encapsulated DC–DC converter is modelled from the parallel-connected buck–boost converter with FLC for hybrid energy system, pv powered, hybrid energy storage system control using bidirectional and boost converters [16,17]. Moreover dual-stage DC–AC converter conversion problems remain unchanged. This proposed research work proposes a new DC–AC three phase bidirectional converter with an encapsulated DC–DC converter block diagram as shown in Figure 2 and modulating signal based on carrier pulse width modulation is analysed, effectiveness and feasibility of the developed converter are examined. Main advantages of the proposed work are single stage conversion, reduced power consumption and DC–DC converter

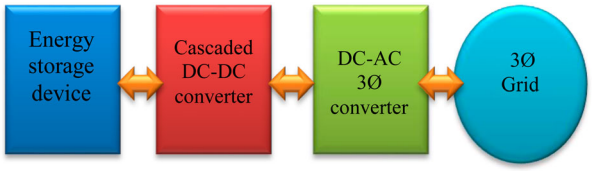

Figure 1. Existing converter.

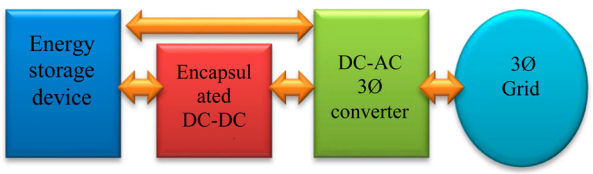

Figure 2. Proposed converter.

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power rating and DC–AC converter with three level output.

2. Modes of operation

The traditional converter is as shown in Figure 3. The DC–AC three phase bidirectional converter with an encapsulated DC–DC converter circuit is shown in Figure 4. The proposed converter is designed with dual parts DC–AC three phase bidirectional conversion stage and encapsulated DC–DC converter stage. High voltage (V_{HIGH}) is the centre part voltage from the sources like super capacitor, ultra capacitor and ESD. This V_{HIGH} is from the encapsulated DC–DC converter stage. The diagram of the power flow DC–AC three phase bidirectional converter with an inverter/rectifier performance is shown in Figures 5 and 6, respectively.

Compared with the traditional converter DC–AC three phase bidirectional converter source voltages

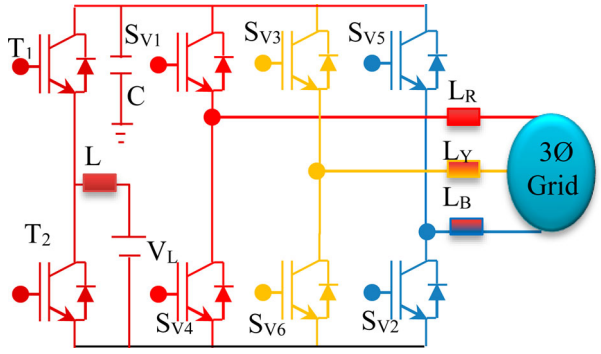


Figure 3. Existing converter circuit.

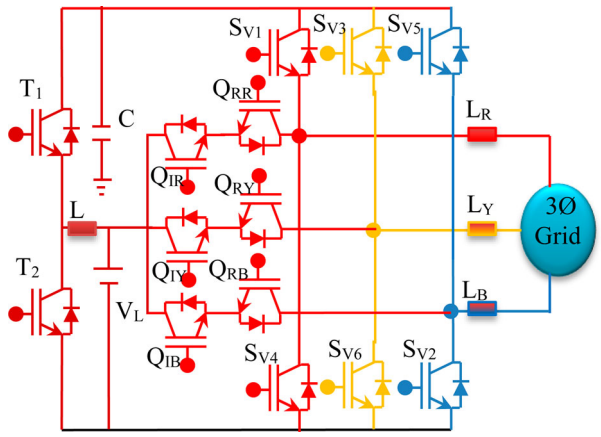


Figure 4. Proposed converter circuit.

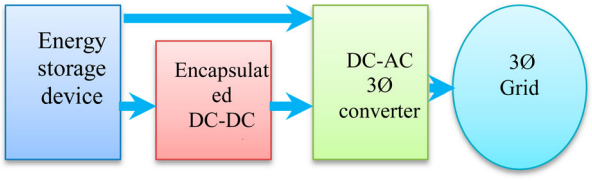


Figure 5. Power flow DC–AC mode.

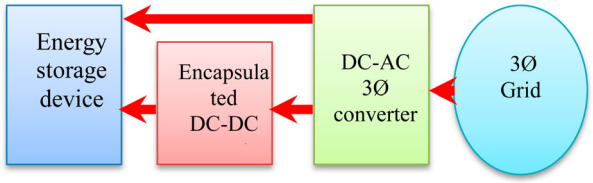


Figure 6. Power flow AC–DC mode.

V_{HIGH} of both DC–AC three phase bidirectional converter or encapsulated DC–DC converter circuit stages. So V_{HIGH} is source or power consumed from inverter stage straightly and sharing power with the grid in a single stage conversion so the encapsulated DC–DC converter circuit processed power and loss in any stages are reduced considerably. Voltage directly extracted from the DC source can change in a wide range. From the grid-side AC voltage, the inverter output voltage has a constant peak amplitude. So, the voltage being high/low voltage (V_{LOW}) is directly calculated from DC supply and can change with a wide range. Apart from this, two voltage levels three phase DC–AC converter can produce three level three phase DC–AC as the output. So, multi-level output with less switching losses from the converter can be obtained from the inverter stage.

3. Control CPWM

The block diagram of control CPWM is as given in Figure 7. A (sg) sign function is helped to get loop-control to find the direction of power flow. Voltage control of V_{HIGH} is obtained by the DC–DC operation stage and whole true power and unused power are controlled by the inverter stage. From the inverter stage current loop-control is created in proportional–integral control direct-quadrature coordinates. The current loop-control direct axis is shown in Figure 8. The open loop-control transfer function is written in Equation (1)

$$G_{io}(s) = G_i(s) * G_d(s) * K_{PWM} * \frac{1}{sL_x} * H_i \quad (1)$$

Current from the proportional–integral controller is expressed in Equation (2)

$$G_i(s) = K_P * \frac{K_i}{s} * H_i \quad (2)$$

The PWM unit and coefficient feedback of inductor are denoted by K_{PWM} and H_i. Phase margin and cut-off frequency of the proportional–Integral controller can be found easily.

Figure 8 shows the inverter control stage is the same to the three phase traditional inverter. Moreover, the control strategy is the main thing to decrease power consumption by the DC–DC stage and increase source power supply from V_{LOW} to the inverter stage straightly (DC–AC mode) is entirely different from the existing control strategy to the three phase converter.

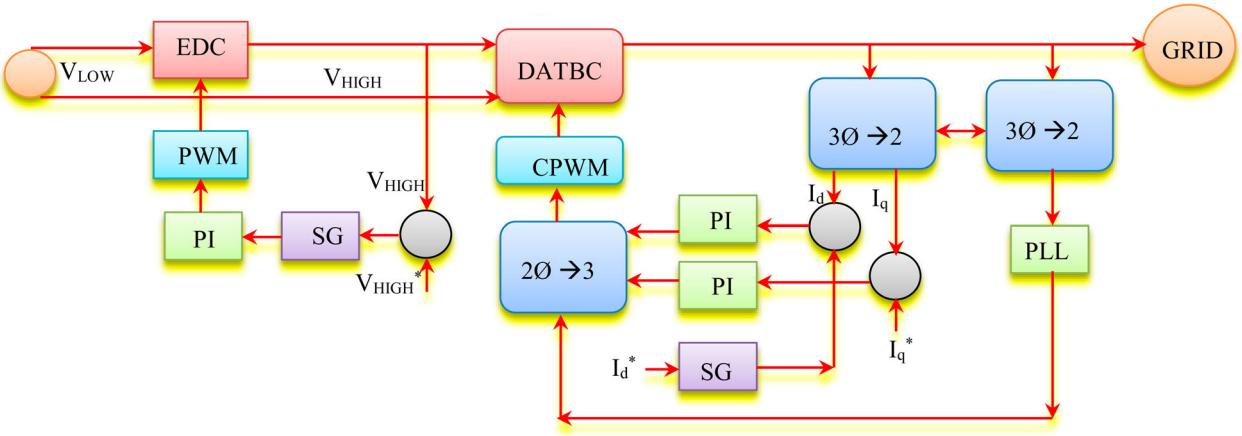


Figure 7. Block diagram of CPWM [7].

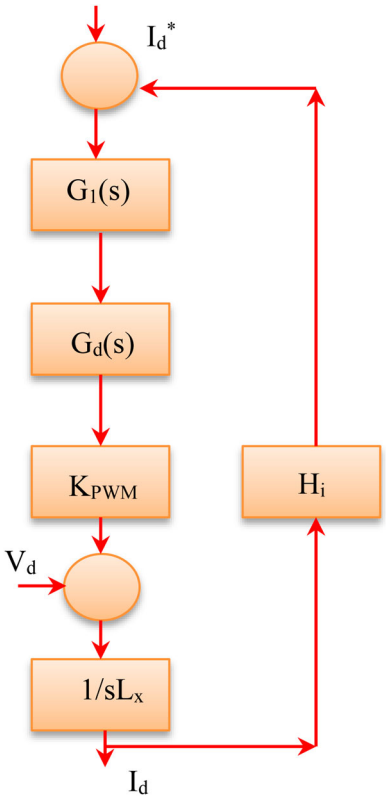


Figure 8. Control loop.

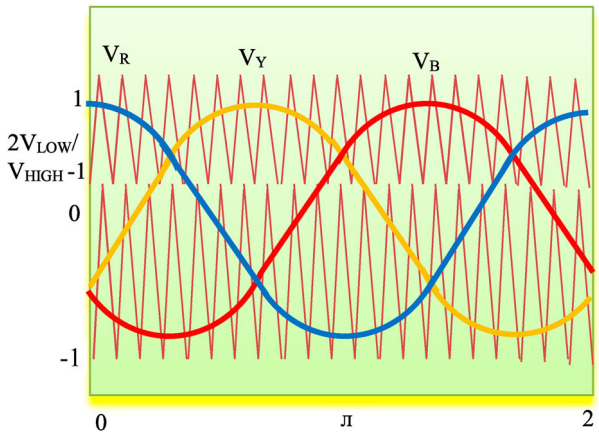


Figure 9. Modulation strategy.

To create single stage power sharing between V_{LOW} and grid, the processed power by the encapsulated DC–DC converter stage can be decreased by the changed CPWM technique that is adopted. The inverter topology is similar to the existing three level converter. Moreover, the main difference is the V_{LOW} is changed and not equal to 50% of V_{HIGH}. Aside from control, the power shared DC-DC converter is as small as possible. During DC–AC mode power straightly supplied by V_{LOW} with the single stage power conversion stage is increased. The variable voltage V_{LOW} and V_{HIGH} double carriers are displaced with zero-axis. Peak-peak voltages are changed, V_{LOW} and V_{HIGH}, as shown in Figure 9. The magnitudes of double carrier are in voltage proportion ($V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}$) and V_{LOW} and normalized by the Equation (3)

$$V_{pT} = \frac{V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}}{V_{\mathrm{HIGH}}/2} = \frac{2(V_{\mathrm{HIGH}} - V_{\mathrm{LOW}})}{V_{\mathrm{HIGH}}} \tag{3}$$

$$V_{pB} = \frac{V_{\mathrm{LOW}}}{V_{\mathrm{HIGH}}/2} = \frac{2V_{\mathrm{LOW}}}{V_{\mathrm{HIGH}}} \tag{4}$$

Especially when $V_{\mathrm{LOW}} = V_{\mathrm{HIGH}}/2$, it is satisfied that $V_{\mathrm{PT}} = V_{\mathrm{PB}}$. From this case magnitude of dual carriers is the same which is similar like the existing three-level converter with carriers. On another side three phase control signal can be written in Equation (5) where the Modulation index is denoted by the letter M, and phase angle is denoted as θ.

$$\begin{cases} V_R = m\cos\theta \\ V_Y = m\cos\theta - 120 \\ V_B = m\cos\theta + 120 \end{cases}. \tag{5}$$

In the DC–AC mode V_{LOW} can source in the inverter stage and phase leg connected with V_{LOW}. For example, when SHA1and SHA2 switches are turned ON, V_{LOW} is connected to phase leg and charging/discharging of V_{LOW} is from current IR. A similar operation is valid for the remaining two phases. If active power is increased from V_{LOW}, the mean value of load current

is enhanced as more as possible. Accordingly, the duty ratio of phase leg V_{LOW} is given in Equation (6)

$$d_x = \begin{cases} \dfrac{1 - V_X}{2 - 2V_{LOW}/V_{HIGH}} & if\ V_X \geq \dfrac{2V_{LOW}}{V_{HIGH}} - 1 \\ \dfrac{1 - V_X}{2V_{LOW}/V_{HIGH}} & if\ V_X < \dfrac{2V_{LOW}}{V_{HIGH}} - 1 \end{cases} \tag{6}$$

$$d_x = \sum_{x=R,Y,B} d_x.i_x \tag{7}$$

Where the current in the R-phase is high when voltage is low.

If mean current values are increased, direct method stops current flowing in the opposite direction into V_{LOW}. Switches with V_{LOW} connected will be OFF and phase current is opposite. To obtain the aim injected zero sequence current into sine waveform, . the three phase output is given, I_m is the maximum current and power factor angle Ø. For unity power factor, Ø = 0. Analysis is performed in section six, Q_1 – Q_6, shown in Figure 7. If Q1 30 < = Θ < = 90, it satisfies that $i_R > = 0$, $i_y > = 0$ and $i_B < 0$. Phase current is the opposite direction in these cases should be blocked. The duty ratio is made zero, zero sequence injected derived as follows:

$$\begin{cases} I_R = I_m \cos(\theta - \varphi) \\ I_Y = I_m \cos(\theta - 120 - \varphi\ ) \\ I_B = I_m \cos(\theta + 120 - \varphi) \end{cases} \tag{8}$$

A similar analysis can be used to other sections. Finally, zero sequence signal output voltage can be expressed in Equation (9). Where the minimum value of voltage of V_R, V_Y, V_B. zero sequence output voltage and zero sequence with changed modulation signal V_X^I is given in Figures 9 and 10.

A zero sequence signal is injected into the sine waveform, changed modulation signal is clamped at −1 during the interval of 120°. During the interval 0 < = Θ < = 120, controlled signal is shifted to −1means opposite direction of phase current is stopped.

$$V_{out} = -V_{min} - 1 \tag{9}$$

The CPWM technique block diagram is as shown in Figure 9. Two important parts asymmetrical carrier and

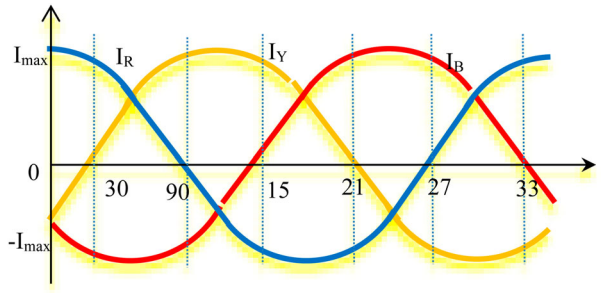


Figure 10. Modulation strategy.

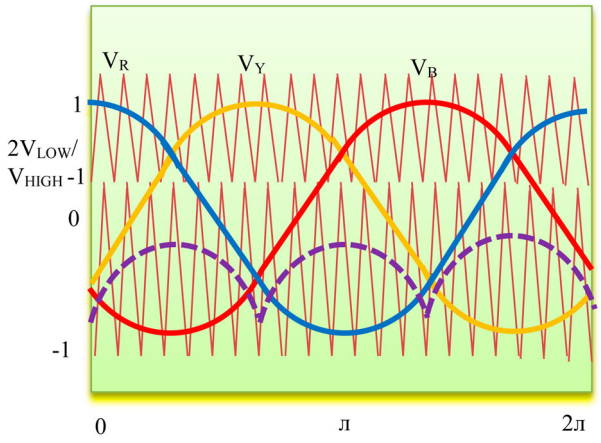


Figure 11. Original sinusoidal modulation ZSI.

changed modulation signals are highlighted. Changed modulation signal is compared with asymmetrical carrier waveform to produce the triggering signal. Real time implementation in a processor asymmetric carrier is simple with the pulse width modulation is shown in Figure 11.

Control signal bisected with top carrier switches operates more frequency. Same duty ratio of two switches varied from 0 to 1. Control signal is changed as

$$V_{x1} = \frac{V_{x1} + 1 - 2V_{LOW}/V_{HIGH}}{2V_{LOW}/V_{HIGH}} \tag{10}$$

Other sets of switches are triggered using changed control signal as given in (11)

$$V_{x1} = \frac{V_{x1} + 1}{2V_{LOW}/V_{HIGH}} \tag{11}$$

Block diagram is as shown in Figure 13. The implementation of CPWM is illustrated in Figure 14. Elaborated equivalent flow of the control strategy is given in Figure 12. Using the CPWM technique the power from source V_{HIGH} to inverter stage power shared in one stage is given in Equation (12). Total power is calculated from zero losses consideration

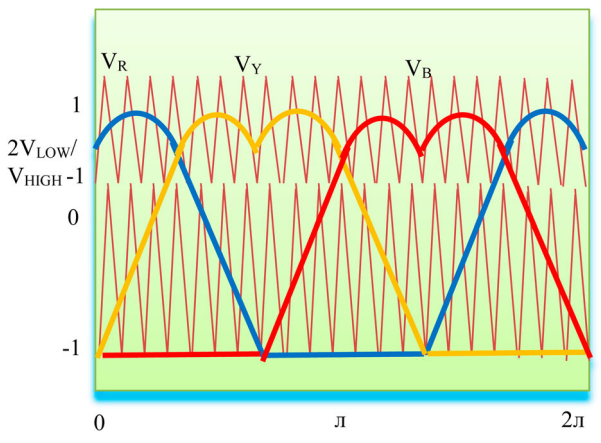


Figure 12. Changed modulation ZSI.

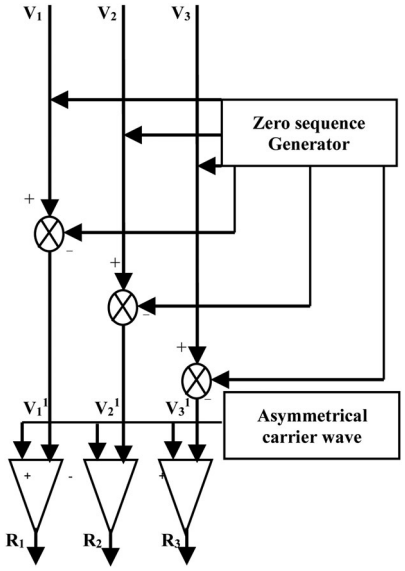


Figure 13. Block diagram CPWM.

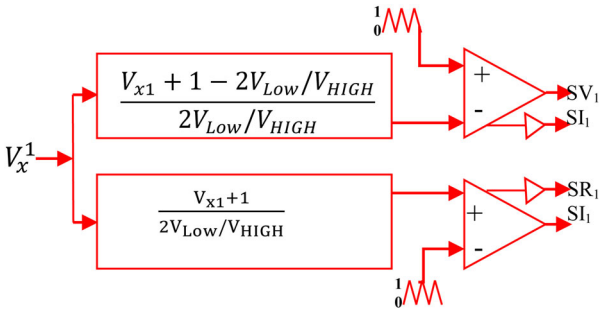


Figure 14. Implementation of CPWM.

which is given in Equation (13). The modulation strategy of process is as depicted in Figure 15(a–c).

$$P_{LOW} = V_{LOW}\frac{1}{2\pi}\int_0^{2\pi} i_{LOW(\theta)}d\theta \tag{12}$$

$$P_{OUT} = \sqrt{3}V_{RB}\frac{I_{max}}{\sqrt{2}}cos\theta \tag{13}$$

$$P_{Lownormal} = \frac{P_{Low}}{P_{out}} \tag{14}$$

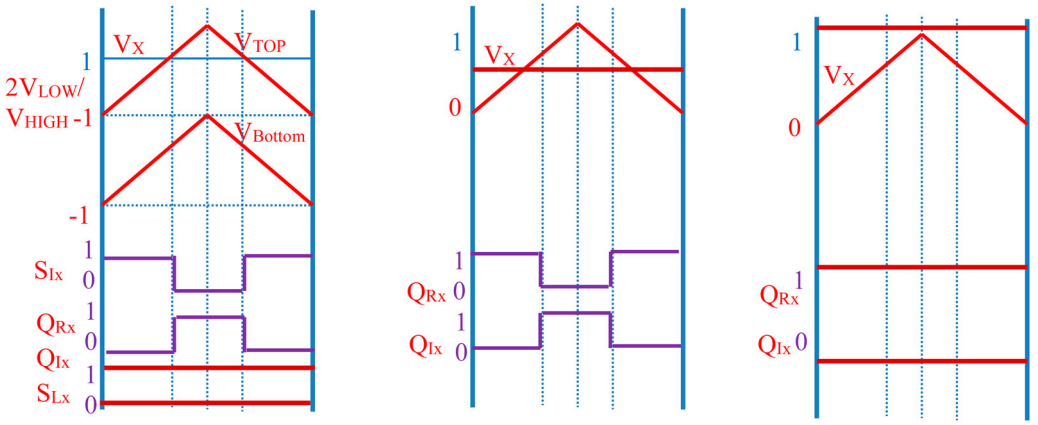
4. Simulation using MATLAB-simulink

MATLAB-Simulink of the proposed system is as shown in Figure 16. To verify the performance of the designed proposed system specifications are given in Table 1. Variable voltages of 250, 50 and 500 V performance and stability are ensured by means of a cutoff frequency of loop-current being set as 2 kHz with 45° phase margin. Gain values of proportional and integral are 0.057 and 20.7 respectively. Specific three values of voltage are taken. Results of the dynamic process by changing reference current from load 2 kW to full load 3 kW and its line voltage of three phase results with filter are shown in Figure 17 and without filter is as shown in Figure 17. Current total harmonic distortion (THD) is obtained as 0.95% with R-L load being given in Figure 18.

The prototype test bench model of the proposed system is as shown in Figure 19. To verify the performance of the designed proposed system specifications are given in Table 1. Variable performance and stability are ensured by means of a cut-off frequency of loop-current being set as 2 kHz with 45° phase margin. Gain values of proportional and integral as 0.057 and 20.7, respectively. Specific three values of voltage are taken. Results of dynamic process by changing reference current from load 2 kW to full load 3 kW and

Table 1. Circuit parameters.

Parameters	Values
V_{LOW}	250–500 V
V_{HIGH}	700 V
Capacitance C_1	500 µF
Inductance L_1	2.2 mH
Inductance 3Ø	1.6 mH
F_s EDC	50 kHz
F_s DATBC	20 kHz
Switches T_1 T_2	CF10110D
Switches 3Ø	HFTF20N10N



(a) Case 1: 2VLow/Vhigh >1 (b) Case 1: 2VLow/Vhigh =1 (C) Case 1: 2VLow/Vhigh <1

Figure 15. Modulation strategy of CPWM process A.

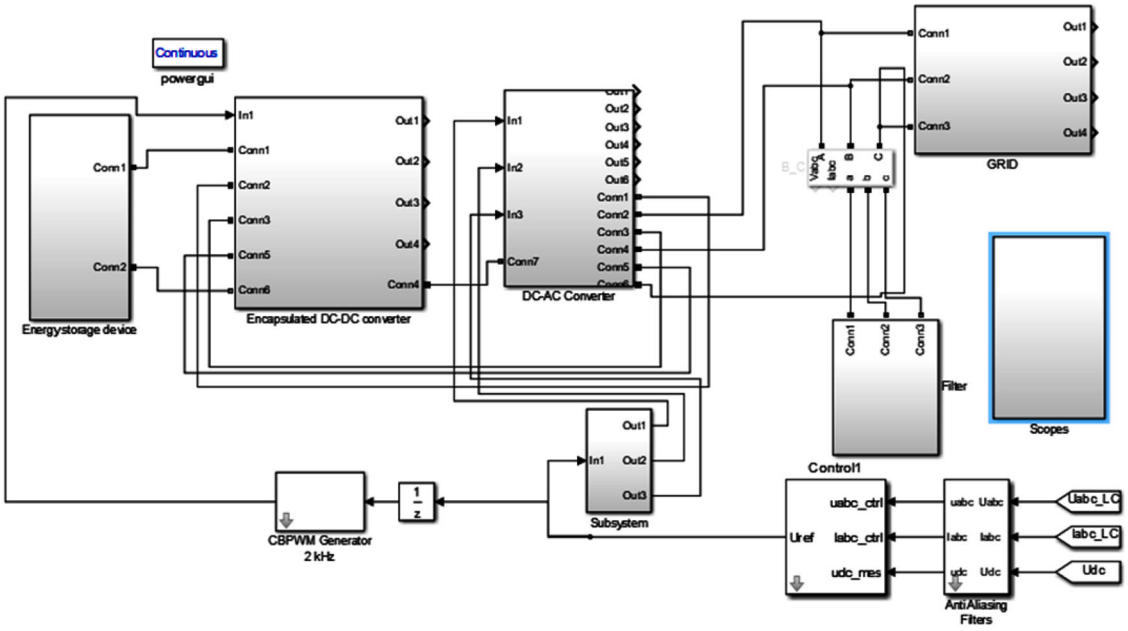


Figure 16. Simulation model.

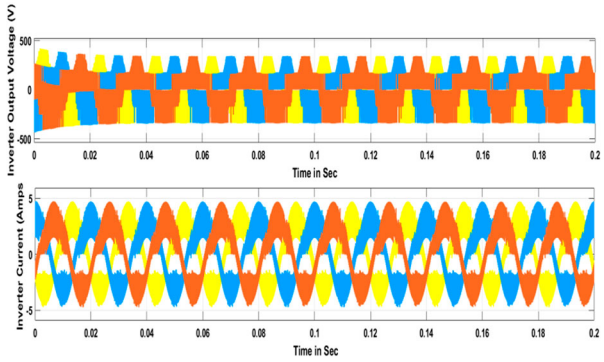


Figure 17. DC–AC converter output without filter (500 V).

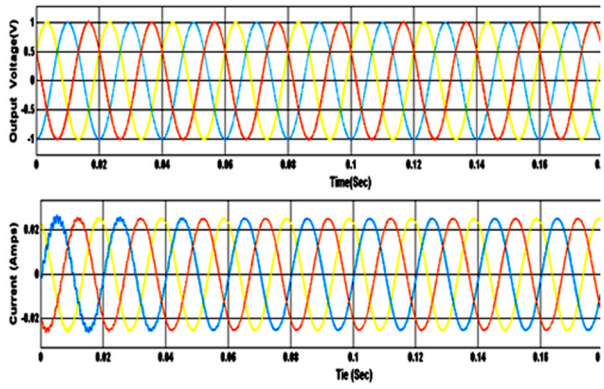


Figure 18. DC–AC converter output with filter (500 V).

its phase current and voltage R phase results are given in Figure 20. Phase voltage and DC voltage (V_{LOW}) are given in Figure 21.

Phase voltage and DC voltage (V_{LOW}) are illustrated in Figure 22, Phase voltage and current are depicted in Figure 23 and line voltage and phase current are shown in Figure 24. Experiment result of dynamic operation bidirectional energy flow is possible, its R & B phase

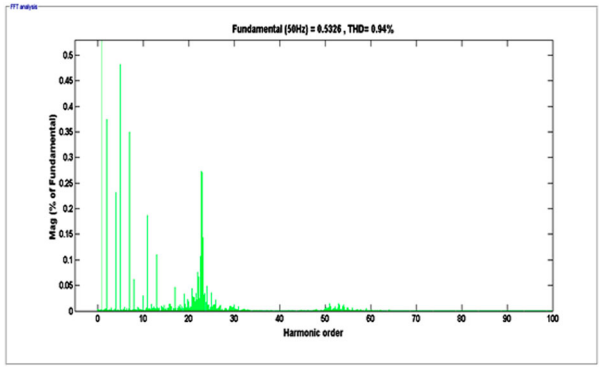


Figure 19. Current THD with filter THD = 0.95%.

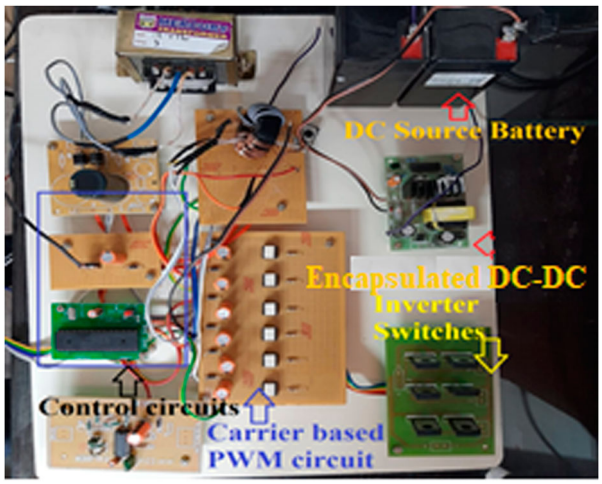


Figure 20. Prototype set-up.

voltages are given in Figure 25 and boost and buck DC voltages are shown in Figure 26. From this it can be observed that phase current is in phase with phase voltage in the DC–AC mode and 180° out of phase

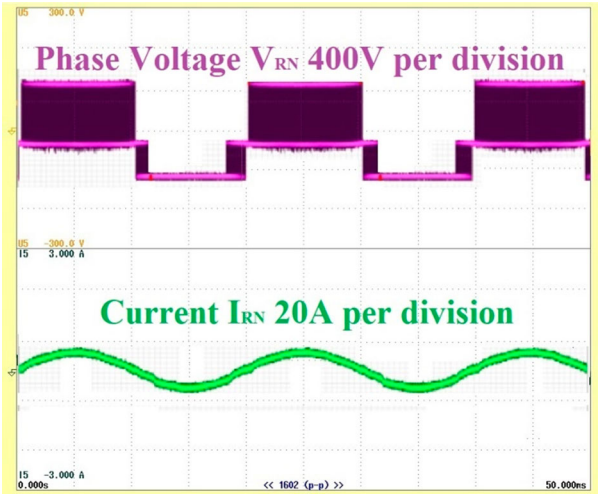


Figure 21. Phase current and voltage R phase.

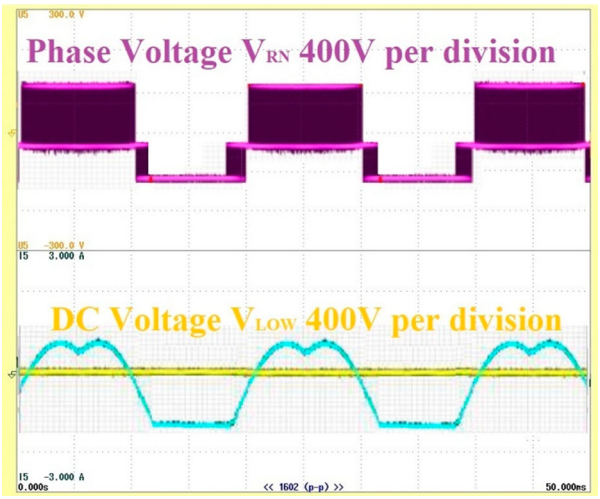


Figure 22. Phase voltage and DC voltage (V_{LOW}).

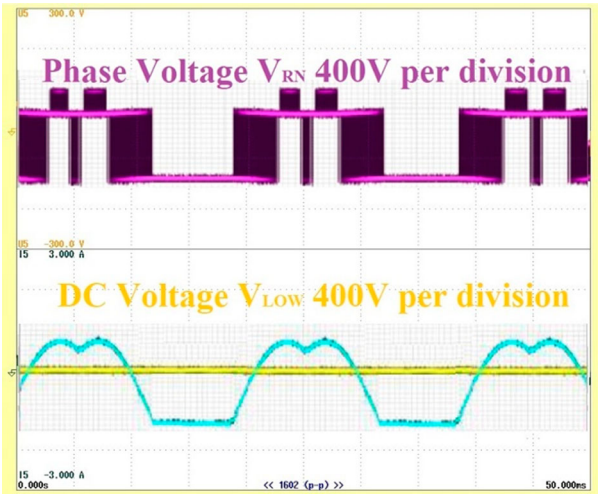


Figure 23. Phase voltage and DC voltage (V_{LOW}).

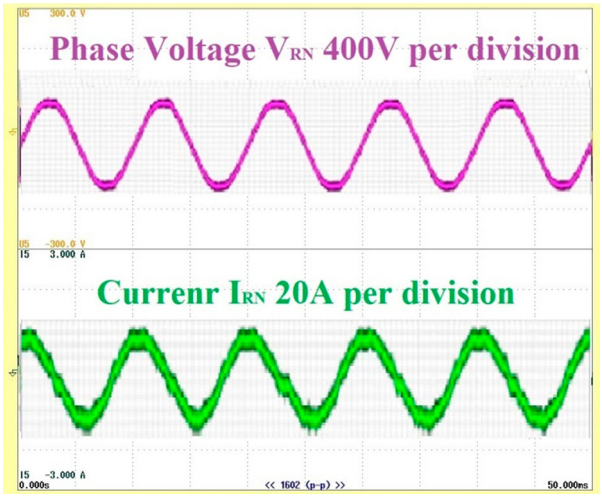


Figure 24. Phase voltage and current.

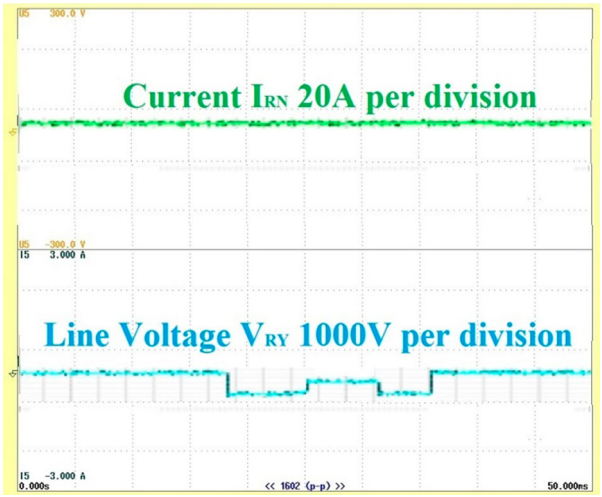


Figure 25. Line voltage and phase current.

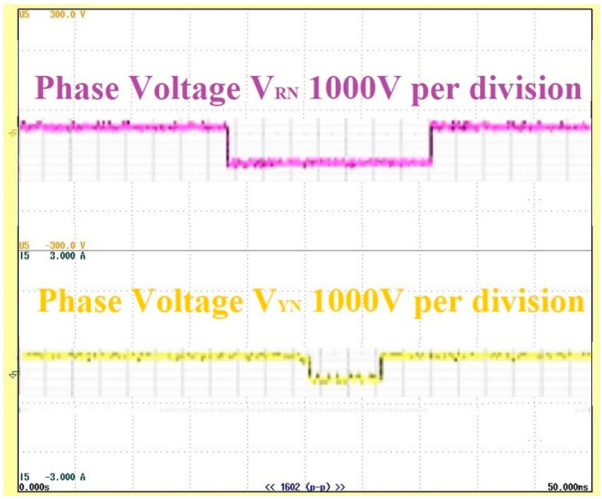


Figure 26. R and B phase voltages.

during AC–DC mode. The command signal is in action. All experimental results show a quick and changing response for bidirectional operation.

Efficiency of the overall system of the proposed converter is identified and compared with the traditional converter. Traditional dual stage DC–AC converter is exactly implemented as that of the proposed converter. Efficiency curves are examined with different values of the load ratio under different conditions. Figure 27(a)

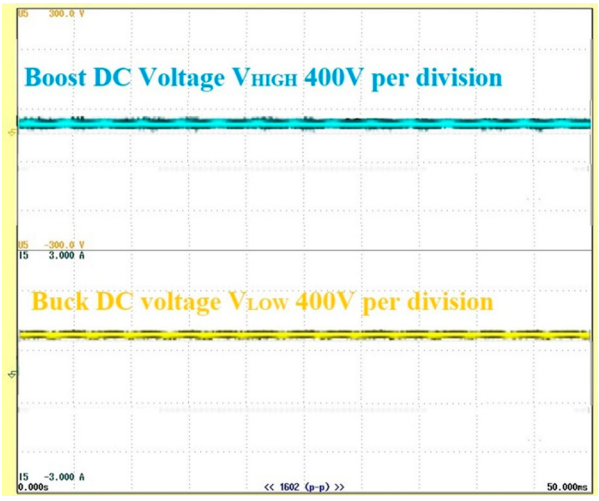


Figure 27. Boost and buck DC voltages.

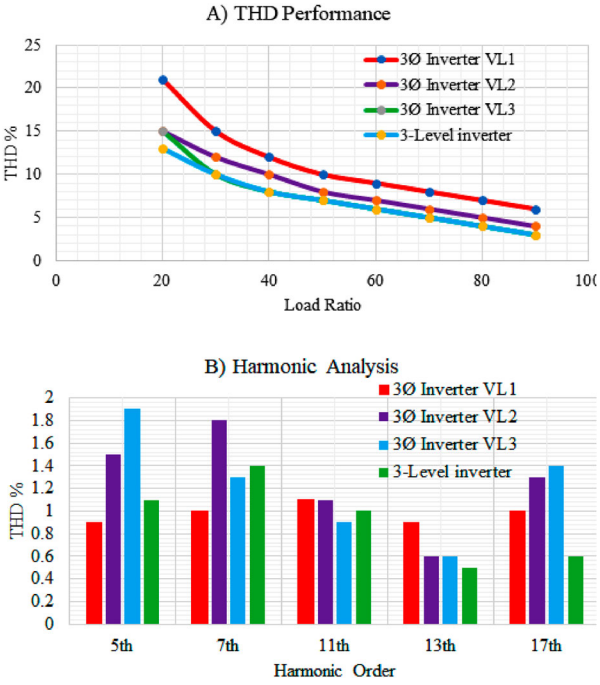


Figure 28. THD vs harmonic order.

shows THD performance and Figure 27(b) shows the different load values of different voltages and harmonic order. From the fair comparisons, proposed solution efficiency is much better than dual stage conversion.

5. Conclusion

The DC–AC three phase bidirectional converter (DATBC) with an encapsulated DC–DC converter (EDC) for the energy storage system (ESD) is analysed and investigated. Working principle, implementation and characteristics of the DATBC are analysed. EDC is stable and constant DC bus is developed between EDC and DATBC. A control technique is adopted for zero sequence components to be inserted in the modulating signal based on carrier pulse width modulation (CPWM). Effectiveness and feasibility of the developed converter are examined with a proto-type model. The proposed converter is entirely different from traditional DSDAC, because it take less than 20% of power used for the DC–AC conversion process. So small power consumption increases efficiency to 96.5%.

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