Selection of PID controller design plane for time-delay systems using genetic algorithm

Original Scientific Paper

Aye Taiwo Ajiboye
University of Ilorin,
Faculty of Engineering and Technology,
Department of Computer Engineering,
Ilorin, Kwara State, Nigeria.
ajiboye.at@unilorin.edu.ng

Olusogo Joshua Popoola
University of Ilorin,
Faculty of Engineering and Technology,
Department of Computer Engineering,
Ilorin, Kwara State, Nigeria.
olusogo@unilorin.edu.ng

Jayeola Femi Opadiji
University of Ilorin,
Faculty of Engineering and Technology,
Department of Computer Engineering,
Ilorin, Kwara State, Nigeria.
jopadiji@unilorin.edu.ng

Olalekan Femi Adebayo
University of Ilorin,
Faculty of Engineering and Technology,
Department of Computer Engineering,
Ilorin, Kwara State, Nigeria.
adebayo.of@unilorin.edu.ng

Abstract *– The design of a Proportional-Integral-Derivative (PID) controller with proportional, integral, and derivative, gain, k_p, k_i, and k_d, respectively, for a time-delay system, is quite common, particularly in the k_i- k_d plane, for a fixed k_p or in the k_p - k_i plane, for a fixed k_d. These design methods have been widely reported in the literature, however, the process of investigating the effects of using any of these design planes on system performance has not been given serious attention hence the need for this study. The stability region in the k_i- k_d and k_p - k_i design plane for a fixed value of k_p and k_d respectively were determined. For every determined stability region, the optimum value of controller gains in the plane was determined using a genetic algorithm (GA) with the integral of time multiplied by absolute error (ITAE) used as the objective function. The optimum value of the fixed gains was graphically determined by plotting the minimum of ITAE (Min-ITAE) for each stability region against the fixed gains. The overall optimum controller gains are the fixed gain that gives minimum of Min-ITAE (Min (Min-ITAE)) and the gains that resulted in Min-ITAE that yielded the Min (Min-ITAE). Using the determined overall optimum controller gains, the system closed-loop step response was plotted for the two design planes and the time domain performance measures (TDPMs) were determined. Based on TDPMs obtained for examples 1, 2, and 3, the k_i-k_d design plane yielded a faster response while the k_p- k_i design plane yielded a response that closely tracks the input irrespective of the system type and order. The study will enable control system designers to select the design plane that will give the best system performance right from the start of controller design without involving trial and error once the system transfer function and design specifications are known.*

Keywords*: Genetic algorithm, ITAE, PID controller, Stability region, Time-delay system, Time domain performance measures*

1. INTRODUCTION

All practical control systems have associated time delays [1-3] resulting from the processing and transmission of signals in the control loop [4, 5]. Therefore, the designing of a controller for such a system requires a full understanding of the effects of this delay on the system's performance. Time delay can degrade the system's quality of performance or destabilise the system in the worst case [6]. To control this class of systems, a PID controller is normally employed due to its popularity [7], simplicity, robustness, and ease of use [8-10]. To design a PID controller for a time-delay system the first step is to establish the stability boundary in the space of the controller parameter [11]. This is because of the lots of work that have been done in this area to the most recent, designs of PID controller for time-delay systems are normally carried out using the stability locus method [12].

One of the proven steps for the design of a PID controller for time-delay systems using the stability locus method involves plotting the stability boundaries in the k_i-k_d plane for a fixed k_p or in the k_p-k_i plane for a fixed k_d and then computing all the stabilizing values of k_p, k_i, and k_d in the stability region by sweeping over k_p and k_d for k_i-k_d, and k_p-k_i design planes respectively [16, 17].

The method for computation of all the stabilizing PID controller gains for a linear arbitrary order system with time delay in the k_i-k_d plane with fixed k_p was re-

ported in [7], while the procedure for computing the entire stability gains in the k_p-k_i plane with fixed k_d was explained in [13]. The stabilization of controller parameters in the k_p-k_i plane for a given k_d, for a time-delay integral fractional-order system, under the control of a fractional-order PID controller, was earlier determined and reported in [14]. It was observed that the controller gains in the k_p-k_i plane for a given k_d and other controller parameters yielded a general stability region, while the global stability region was obtained after the griding of k_d. PID parameters for a second-order plant with time delay were obtained in the k_p-k_i plane with a fixed k_d for specified GM and PM using the dominant poles method, as reported in [13]. PID controller tuning method for integrating system with time delay was developed in the k_p-k_i plane for a fixed k_d by [15]. After determining the stability region, weighted geometrical center approach was used to determine the required PID controller gains. The results obtained via simulation are good, but the fixed k_d was not optimized. In [16, 17], parametric methods were used to establish the stability region in the k_i-k_d plane for a fixed k_p and k_p-k_i plane for a fixed k_d, and GA was used to determine the optimum controller gains in the established region of the plane.

Despite the huge amount of published works in the literature on PID controller designs for time-delay systems in either k_i-k_d or k_p-k_i design planes, the effects of using either of the two design planes on the performance of the designed system have not been given serious attention in the research community, hence the need for this study. The aim of this study, therefore, is to investigate the effects of PID controller design plane selection on the performance of the designed system.

To achieve the aim of this study, the equations that relate the controller gains, the system parameters, and the time delay together were derived. Using these equations and the frequency obtained from the graph of k_p and k_d against the frequency (ω), the stability boundaries in k_i-k_d and k_p-k_i planes for fixed k_p and k_d respectively was plotted. After the determination of the stability boundaries, the optimum controller gains within the stability region can now be determined. Several optimization methods have been used in the literature but in this study, GA was used because of its heuristic characteristics, powerful searching capabilities [18], and amenability of the method of stability boundary locus (used in this study) to GA. For each of these regions, the optimum controller gains were determined via GA using ITAE as the objective function. Since GA was used as a minimization process in this study, the obtained minimum value of ITAE (Min-ITAE) was plotted against the fixed k_p and k_d for k_i-k_d and k_p-k_i design planes respectively. Based on these graphs, the overall optimum gains were determined. These gains were used together with the system and time-delay transfer functions to generate the system closed-loop unit step response, which yielded the system TDPMs. The TDPMs considered in this study are T_r (rise time), %OS (percentage overshoot), %US (percentage undershoot), T_p (peak time), T_s (settling time), and ess (steady-state error). These performance measures were used for system analysis and characterisation in the plane under consideration. The results show that the k_i-k_d design plane produced a faster response while the k_p-k_i design plane gives a response that closely tracks the input irrespective of the system's type and order. Therefore, the major contribution of the study is to aid the control system designers in the selection of the design plane that will give the best system performance at the beginning of controller design without involving trial and error, given that the system transfer function and design specifications are known.

2. METHODOLOGY

2.1. DETERMINATION OF STABILITY BOUNDARY FOR PID-CONTROLLED SYSTEM

The derivation of system forward and closed-loop transfer functions used in this study is based on the block diagram of the unity feedback control system shown in Fig.1, where *R(s)*, *E(s)*, and *Y(s)* are the reference input, error, and output respectively. Equations (1), (2), and (3) are the adopted expression for the plant, time delay, and controller transfer function respectively.

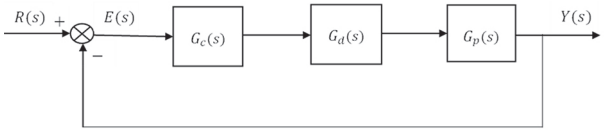

Fig. 1. Block diagram of unity feedback time-delay control system

$$G_p(s) = \frac{N(s)}{D(s)} \tag{1}$$

where *N(s)* and *D(s)* are the plant transfer function numerator and denominator respectively.

$$G_d(s) = e^{-\tau s} \tag{2}$$

where τ is the time delay in sec.

$$G_c(s) = \frac{k_d s^2 + k_p s + k_i}{s} \tag{3}$$

For easy application of D-decomposition method, the numerator and denominator of Equation (1) were broken into their even and odd parts after substituting jω for s as shown in Equation (4). It should be noted that for compactness purpose, the ($-\omega^2$) term has been removed from N_e ($-\omega^2$), N_o ($-\omega^2$), D_e ($-\omega^2$) and D_o ($-\omega^2$) in Equation (4) [19].

$$G_p(j\omega) = \frac{N_e + j\omega N_o}{D_e + j\omega D_o} \tag{4}$$

Finding the stability boundary in k_p, k_i, and k_d space is a three-dimensional problem. For easy controller de-

sign and analysis, it can be reduced to a two-dimensional problem by fixing one of the parameters and finding the stability region in the plane of the remaining two parameters. The overall stability region can be determined using the stability regions in the plane of the two parameters by sweeping over the fixed parameter values. For this study, k_p and k_d were fixed and the stability boundaries in the k_i-k_d and k_p-k_i planes were determined respectively.

The equations and conditions required for determining the stability region in the k_i-k_d plane for a fixed k_p and the stability region in the k_p-k_i plane for a fixed k_d are presented as follows [16, 17, 19, 20]:

2.1.1. Stability region in the k_i-k_d plane for a fixed k_p

For ω=0

$$k_i=0 \tag{5}$$

For ω>0

$$k_p = \frac{\left(\omega^2 N_o D_o + N_e D_e\right)\cos(\omega T)+\omega(N_o D_e - N_e D_o)\sin(\omega T)}{-\left(N_e{}^2+\omega^2 N_o{}^2\right)} \tag{6}$$

$$k_d=\frac{\omega^2(N_o D_e - N_e D_o)\cos(\omega T)-\omega(N_e D_e+\omega^2 N_o D_o)\sin(\omega T)+k_i\left(N_e{}^2+\omega^2 N_o{}^2\right)}{\omega^2\left(N_e{}^2+\omega^2 N_o{}^2\right)} \tag{7}$$

where $\omega = \omega_n$, (n=1,2,……) are the frequencies at which the line of a given value of k_p intercepts the graph of k_p of Equation (6) versus ω, and n is the number of points of intersection or the number of lines obtainable from Equation (7).

The stability boundary in the k_i-k_d plane is formed by the line obtained from Equation (5) and the lines generated from Equation (7) when ω_n is substituted for ω.

2.1.2. Stability region in the k_p-k_i plane for a fixed k_d

For ω=0

$$k_i=0 \tag{8}$$

For $\omega\geq 0$

$$k_p = \frac{\left(\omega^2 N_o D_o + N_e D_e\right)\cos(\omega T)+\omega(N_o D_e - N_e D_o)\sin(\omega T)}{-\left(N_e{}^2+\omega^2 N_o{}^2\right)} \tag{9}$$

$$k_i=\frac{\omega^2(N_o D_e - N_e D_o)\cos(\omega T)-\omega(N_e D_e+\omega^2 N_o D_o)\sin(\omega T)-K_d\omega^2\left(N_e{}^2+\omega^2 N_o{}^2\right)}{-\left(N_e{}^2+\omega^2 N_o{}^2\right)} \tag{10}$$

where ω=[0,ω_c] and ω_c is the frequency at which the line of a given value of k_d in Equation (10) intercepts the graph of k_d in Equation (11) against ω. Equation (11) was obtained from equation (7) when it is assumed that k_i=0.

$$k_d = \frac{\omega^2(N_o D_e - N_e D_o)\cos(\omega T)-\omega\left(N_e D_e+\omega^2 N_o D_o\right)\sin(\omega T)}{\omega^2\left(N_e{}^2+\omega^2 N_o{}^2\right)} \tag{11}$$

The stability boundary in the k_p-k_i plane is formed by the line obtained from Equation (8) and the locus generated by Equations (9) and (10) when ω=[0,ω_c].

2.2. OPTIMIZATION OF PID CONTROLLER PARAMETERS

After the determination of the system convex stability region, the next step is to determine the value of the controller parameters that give the best system performance. The success of the determination and selection of optimum PID controller parameters using GA as an optimization tool is strongly dependent on the selection of appropriate objective function. To optimize the PID controller parameters, different system performance indices have been used as the objective function. ITAE, ISE, MSE, and IAE were used by [21], ISE, ITAE, and IAE were used in [22, 23], while in [24] work, ISE, ITAE, IAE, and their combination were used. The ITAE (see equation (12)) was adopted in this study due to its best selectivity, a good criterion for PID controllers design [25]; and its minimum value can be easily defined as the system parameters are varied [26],

$$ITAE = \int_0^\infty t|e(t)|\,dt \tag{12}$$

where $T_1 \geq T_s$,(T_s is the system settling time in sec.), e(t) is the error and t is the time in sec.

2.3. GA-BASED PID CONTROLLER PARAMETERS OPTIMIZATION

The PID controller gains were optimised using GA by following the steps shown in the flowchart of Fig. 2.

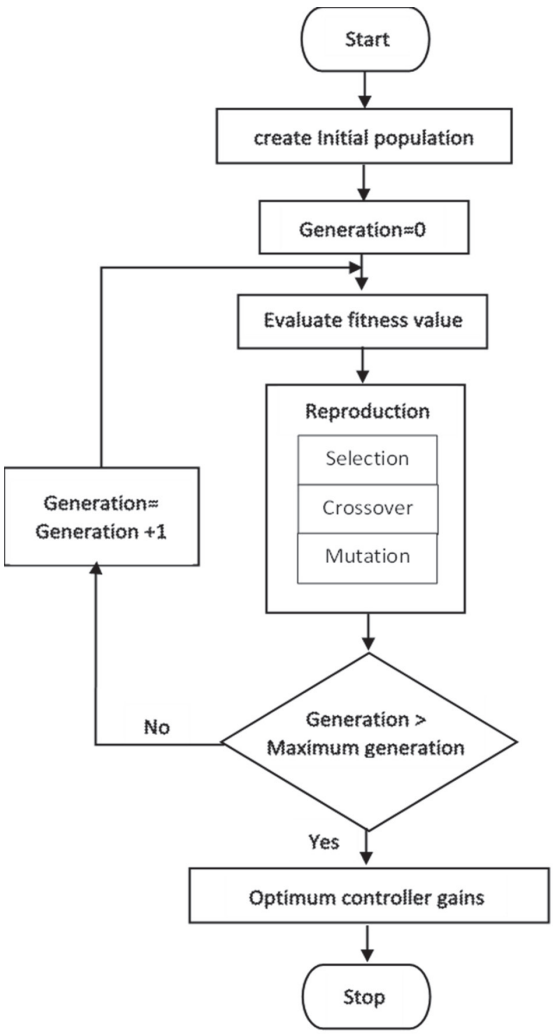

Fig. 2. Flowchart of GA process for optimising PID controller gains [27, 28]

The initial population was created inside the stability region because the stability boundary serves as the constraint for the optimisation problem. To determine the fitness of the generated PID controller gains, the objective function, ITAE in this case was calculated for these gains in parallel. Based on the ranking value of the fitness function for the PID controller gains, half of the population was selected for reproduction. To get the next generation, the crossover was carried out on the already selected feasible solutions (gains). Also, to guide against the production of false optimum controller gains, a few individual solutions in the generation were mutated. The process continues in a loop until when there are no significant changes in the generations which is the condition for termination of the optimisation process. Details on the design of PID controllers for delay-free and time-delay systems using GA can be found in [16, 17] and [29] respectively.

3. SIMULATION EXAMPLES

Three different examples were used to demonstrate the selection of the PID controller design plane. For each of these examples, GA was used in searching for the: (i) optimum k_i and k_d in the k_i - k_d plane for different values of k_p (ii) optimum k_p and k_i in the k_p - k_i plane for different values of k_d. Associated with each set of the optimum gains is a unique Min-ITAE since GA was used as a minimisation process. The optimum fixed k_p gain $k_{p,f,opt}$ for the k_i-k_d plane and $k_{d,f,opt}$ for the k_p - k_i plane is the one that gives Min(Min-ITAE) and can be graphically determined from the graphs of Min-ITAE versus fixed k_p and Min-ITAE versus fixed k_d for k_i-k_d plane and k_p - k_i plane respectively. The overall optimum gains for the k_i-k_d plane are the $k_{p,f,opt}$ and the optimum k_i and k_d denoted by $k_{i,opt}$ and $k_{d,opt}$ respectively, that yielded the Min-ITAE that gives Min(Min-ITAE). Also, the overall optimum gains for the k_p-k_i plane are the $k_{d,f,opt}$ and the optimum k_p and k_i also denoted by $k_{p,opt}$ and $k_{i,opt}$ respectively, that yielded the Min-ITAE that gives Min(Min-ITAE).To provide room for system performance analysis and characterisation in each of these design planes using TDPMs, the system step response was plotted based on the overall optimum controller gains.

3.1. EXAMPLE 1

The design of the PID controller for an integrating second-order time-delay system with the system transfer function given by equation (13) [30] was considered in this example. For this system N_e=1, N_o=0, D_e=-ω^2, and D_o=1.

$$G(s) = \frac{1}{s(s+1)} e^{-s} \tag{13}$$

The ranges of k_d and k_p were first determined by plotting k_d against k_p as shown in Fig. 3 using equations (6) and (11). Also based on these equations, the plots of k_p against ω and k_d against ω are shown in Fig. 4 and 5 for the determination of the relevant frequencies for any given value of k_p and k_d respectively. It can be seen from Fig. 3 that the ranges of k_p and k_d are 0 – 1.717 and -1 – 2.261 respectively.

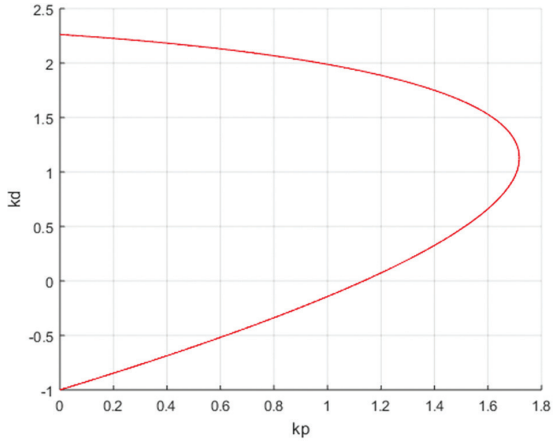

Fig. 3. Plot of k_d against k_p

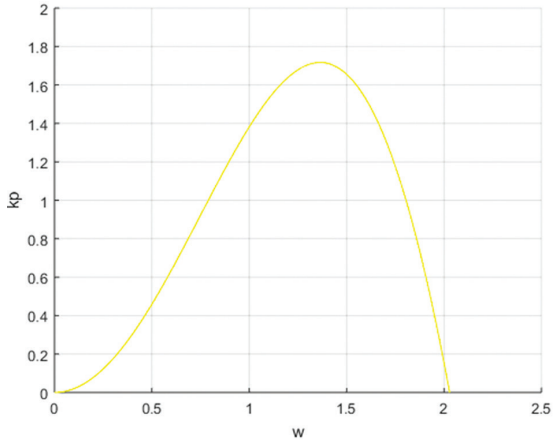

Fig. 4. Plot of k_p against ω

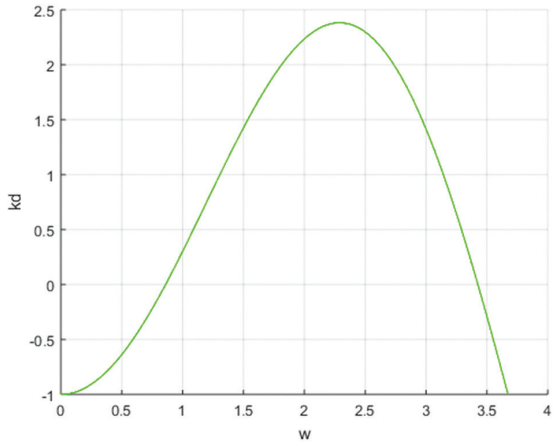

Fig. 5. Plot of k_d against ω

For the case of PID controller design in the k_i-k_d plane, the fixed gains considered based on the range of k_p as presented in Fig. 4 are k_p = 0.2, 0.4, 0.6, 0.8, 1.0, 1.2, 1.4, and 1.6. The detailed design for k_p = 0.2 is presented as follows:

As explained in Subsection 2.1.1., when ω = 0, the stability boundary equation that can be used for generating one of the boundary lines was derived using Equation (5). To generate the equations that can be used to form the

remaining boundary lines, the frequency at the point of intersection of the line of k_p = 0.2 with the plot of k_p versus ω in Fig. 4 was determined. From Fig. 4, the points of intersection are two and their corresponding frequencies are ω_1=0.322 rad and ω_2= 1.991 rad. Substituting ω_1 and ω_2 in Equation (7) yielded the remaining two equations required for generating the stability boundary's lines. The resulting stability boundary equations are:

$$k_i=0 \quad (14)$$

$$k_{d1}=9.6447k_i-0.8467 \quad (15)$$

$$k_{d2}=0.2523k_i+2.2257 \quad (16)$$

Based on Equations (14) – (16), and the similar equations obtained for values of remaining fixed k_p following, the steps used for k_p = 0.2, the system stability boundary in the k_i-k_d plane shown in Fig. 6 and 7 were obtained for when k_p = 0.2 and for the complete set of fixed k_p, respectively.

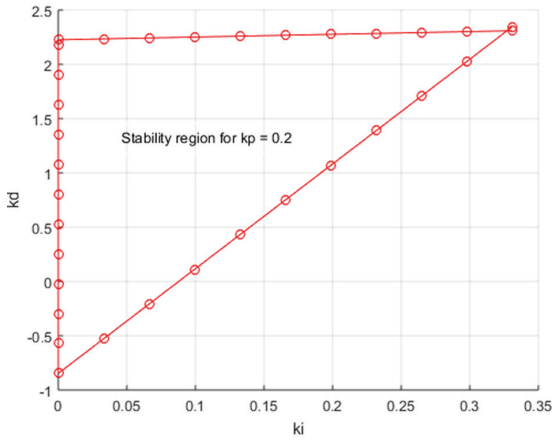

Fig. 6. The stability boundary in the k_i-k_d plane for k_p = 0.2

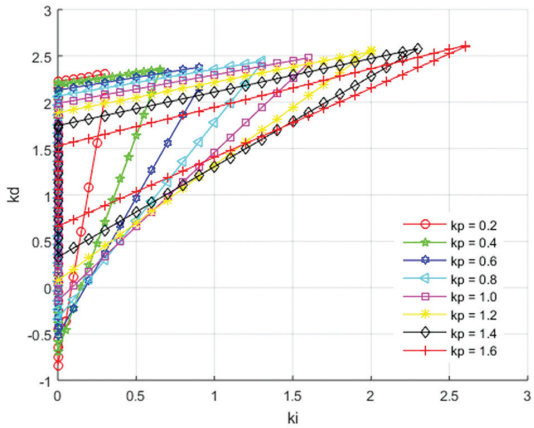

Fig. 7. The stability boundary in the k_i-k_d plane for the set of fixed k_p

The constraints needed for the GA were formed using Equations (14) – (16) and the stability boundary equations for other fixed k_p considered following the same steps. After the formation of the constraints, the GA MATLAB code was written according to the flowchart in Fig. 2. The code was run for each scenario to determine the optimum k_i and k_d, and the corresponding Min-ITAE for each of the fixed k_p. The $k_{p,f,opt}$ and Min (Min-ITAE) were obtained from the plot of Min-ITAE versus fixed k_p. The required TDPMs were obtained from the unit step response plotted using the determined overall optimum controller gains.

Taking the case of PID controller design in the k_p-k_i plane the fixed gains considered based on the range of k_d as shown in Fig. 5 are k_d = -0.5, 0, 0.5, 1.0, and 1.5. The design analysis for k_d = -0.5 is presented as follows:

As discussed in Subsection 2.1.2., when ω = 0, the stability boundary equation that was used for generating one of the boundaries was derived using Equation (8). The frequency at the first point of intersection of the line of k_d = -0.5 with the plot of k_d versus ω in Fig. 5 was determined to generate the equation that can be used to form the remaining boundary locus. From Fig. 5, the frequency at the said points of intersection, ω_c=0.5917 rad. By generating the straight line defined by Equation (8) and plotting k_i against k_p using Equations (9) and (10) with ω=[0, ω_c] the stability boundary of Fig. 8 was obtained for k_d = -0.5.

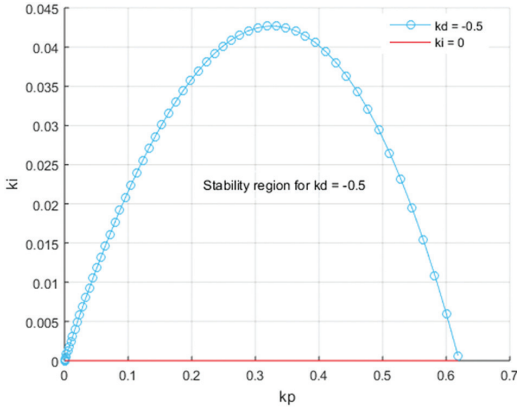

Fig. 8. The stability boundary in the k_p-k_i plane for k_d = -0.5

The same steps used for k_d = -0.5 was adopted for other fixed k_d scenarios and the stability boundaries of Fig. 9 were obtained. The stability boundary equations for k_d = -0.5 case were obtained from Equation (8) and by curve fitting the stability locus of Fig. 8 and are presented in Equations (17) and (18) respectively.

$$k_i=0 \quad (17)$$

$$k_i= -0.061k_p^4-0.069k_p^3-0.34k_p^2+0.25k_p-3.6\times10^{-6} \quad (18)$$

For other fixed k_d values, the stability boundary equations like (17) and (18) were also generated following the steps used for k_d = -0.5 case.

The constraints needed for the GA were formed using Equations (17) and (18) and the stability boundary equations for other fixed k_d were considered. After the formation of constraints, the GA MATLAB code was written according to the flowchart in Fig. 2. The code was run for each scenario to determine the optimum k_p and k_i,

and the corresponding Min-ITAE for each of the fixed k_d. $k_{d,f,opt}$ and Min (Min-ITAE) were obtained from the plot of Min-ITAE versus fixed k_d. Also, the required TDPMs were obtained from the unit step response plotted using the determined overall optimum controller gains.

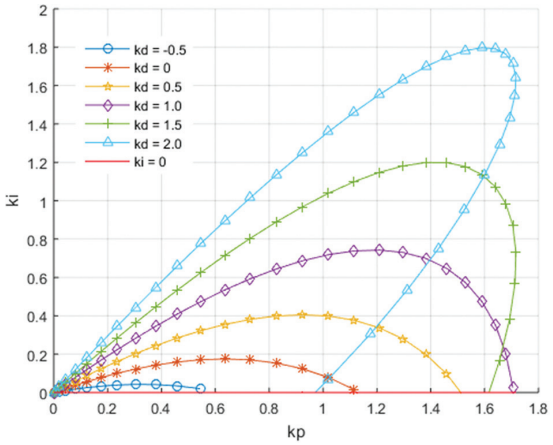

Fig. 9. The stability boundary in the k_p-k_i plane for the set of fixed k_d

3.2. EXAMPLE 2

The design of a PID controller for an integrating second-order time-delay system with left-hand side zero whose transfer function is shown in Equation (19) [15] was considered in this example. For this system N_e=0.6, N_o=-0.18, D_e= -w^2, and D_o=1

$$G(s) = \frac{0.6(-0.3s+1)e^{-0.2s}}{s(s+1)} \tag{19}$$

The method employed for the design of the PID controller in Example 1 was adopted in this example. As a result, the PID controller design in the k_i-k_d plane in this example was considered for the following fixed k_p values:1, 2, 3, 4, 5, and 6. The stability boundary for the considered values of fixed k_p is shown in Fig. 10. The required TDPMs were obtained from the unit step response plotted using the determined overall optimum controller gains.

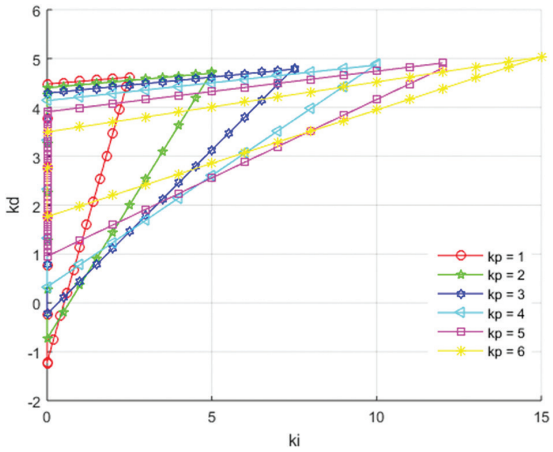

Fig. 10. The stability boundary in the k_i-k_d plane for the set of fixed k_p

To design the PID controller in the k_p-k_i plane for this example the considered range of fixed k_d are k_d = -1, 0, 1, 2, 3, and 4, and the stability boundaries of Fig. 11 were obtained for these fixed values of k_d. The required TDPMs were obtained from the unit step response plotted using the determined overall optimum controller gains.

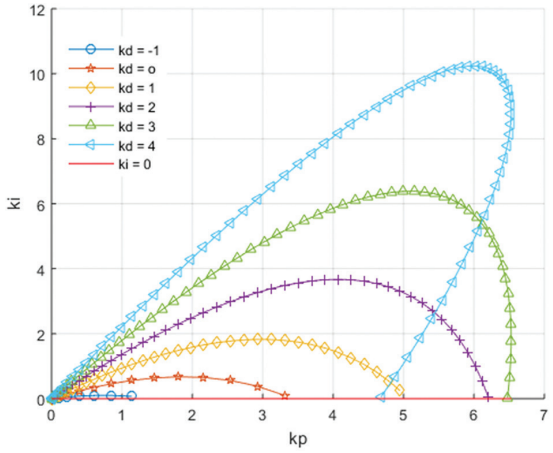

Fig. 11. The stability boundary in the k_p-k_i plane for the set of fixed k_d

3.3. EXAMPLE 3

The design of a PID controller for a second-order time-delay system with left-hand side zero whose transfer function is shown in Equation (20) [19] was considered in this example. For this system N_e=1, N_o=-0.5, D_e=1-2w^2, and D_o=3.

$$G(s) = \frac{(-0.5s+1)e^{-0.6s}}{(s+1)(2s+1)} \tag{20}$$

In this example, the method of PID controller design used in Example 1 was adopted. Therefore, for the k_i-k_d plane the considered fixed k_p values are: k_p = -0.5, 0, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, and 3.5. For these k_p values, the obtained stability boundary is shown in Fig. 12. The required TDPMs were obtained from the unit step response plotted using the determined overall optimum controller gains.

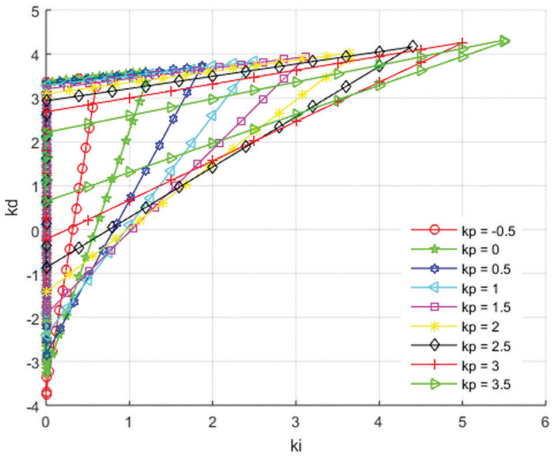

Fig. 12. The stability boundary in the k_i-k_d plane for the set of fixed k_p

For the design of PID controller in the k_p-k_i plane the fixed values of k_d considered are: k_d = -3, -2, -1, 0, 1, 2 and 3. Based on these values of k_d the stability boundaries plot of Fig. 13 was obtained. The required TDPMs were obtained from the unit step response obtained using the determined overall optimum controller gains.

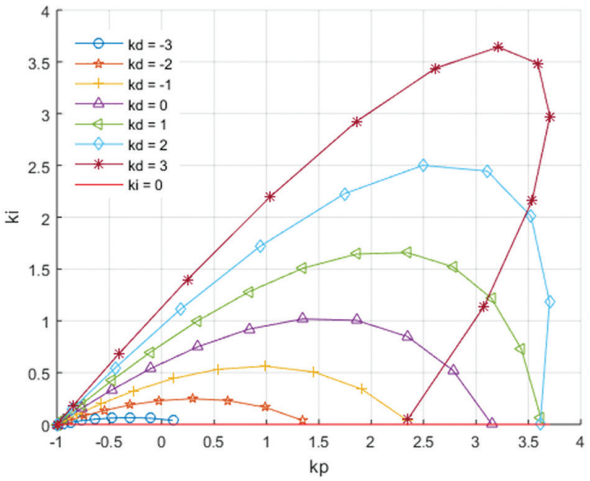

Fig. 13. The stability boundary in the k_p-k_i plane for the set of fixed k_d

4. RESULTS AND DISCUSSIONS

The graphs of Min-ITAE versus the fixed k_p and fixed k_d for the k_i-k_d design plane and k_p-k_i design plane for Examples 1, 2, and 3 are shown in Fig. 14, 15, and 16 respectively. It can be seen from these Figures that Min-ITAE decreases from the initial value to the minimum value and then increases to a final value. Based on the minimum of Min-ITAE and the corresponding fixed k_p and fixed k_d obtained, $k_{p,f,opt}$, $k_{d,f,opt}$ and Min (Min-ITAE) were determined and presented in Table 1. Using the value of $k_{p,f,opt}$, $k_{d,f,opt}$ and the corresponding value of Min (Min-ITAE) the value of $k_{p,opt}$, $k_{i,opt}$ and $k_{d,opt}$ were obtained from the GA optimisation results and presented in Table 1.

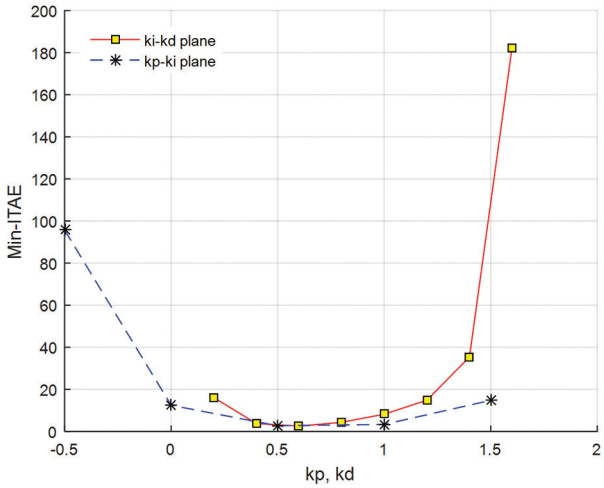

Fig. 14. Plot of Min-ITAE versus the values of fixed k_p, k_d for Example 1

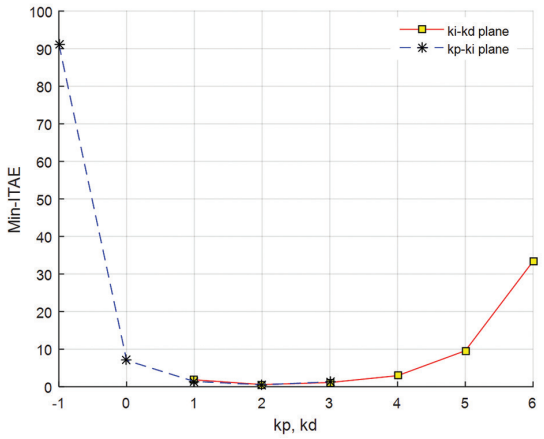

Fig. 15. Plot of Min-ITAE versus the values of fixed k_p, k_d for Example 2

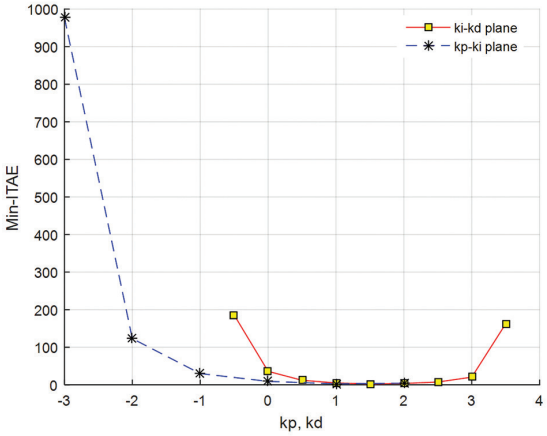

Fig. 16. Plot of Min-ITAE versus the values of fixed k_p, k_d for Example 3

Using the open-loop transfer functions of Equations (13), (19), and (20) and the overall optimum gains of Table 1, the system closed-loop unit step responses of Fig. 17, 18, and 19 were plotted for Examples 1, 2, and 3 respectively. From Fig. 17, 18, and 19, it is obvious that the systems' response never tracks the unit step input instead, 0.5, 0.375, and 0 were tracked respectively, therefore, the need for a controller for these systems.

The TDPMs values obtained from the step response of Fig. 17 to 19 for the controlled systems under the two design planes are presented in Table 2. It is obvious from Table 2 that the resulting system from the two design planes for the 3 examples is of good steady state because *ess*=0. Considering the transient state status, the response of the k_i-k_d design plane has higher swiftness for all the examples because of low T_r and T_p compared to the k_p-k_i design plane. On the other hand, the degree of similarity between the response of the system designed in the k_p-k_i plane with the unit step input for all examples is high compared with that of the k_i-k_d plane because of the lower value of %***OS*** and T_s associated with the former. It can also be seen from Table 2, for Examples 2 and 3, there is an associated %*US* because of the right-hand side zero. But the %*US* for the k_i-k_d plane is higher than that of the k_p-k_i plane.

Table 1. Optimum controller gains for different scenarios

Example	Plane	$k_{p,f,opt}$	$k_{d,f,opt}$	$k_{p,opt}$	$k_{i,opt}$	$k_{d,opt}$	Min (Min-ITAE)
1	k_i-k_d	0.6			-1.133×10^{-11}	0.712	2.538
	k_p-k_i		0.5	0.470	3.338×10^{-07}		2.703
2	k_i-k_d	2.000			-1.808×10^{-09}	2.278	0.5762
	k_p-k_i		2.000	1.935	2.013×10^{-12}		0.5184
3	k_i-k_d	1.5			0.485	1.113	2.398
	k_p-k_i		1.000	1.410	0.460		2.564

Table 2. TDPMs for different examples and planes

Example	Plane	T_r (sec.)	*%OS*	*%US*	T_p (sec.)	T_s (sec.)	*ess*
1	k_i-k_d	1.293	10.222	0	3.522	6.720	0.000
	k_p-k_i	2.067	1.092	0	5.083	3.935	0.000
2	k_i-k_d	0.437	14.048	41.009	1.421	2.940	0.000
	k_p-k_i	0.549	7.926	36.000	1.618	2.136	0.000
3	k_i-k_d	1.485	1.874	27.812	3.985	3.202	0.000
	k_p-k_i	1.736	0.948	25.000	4.570	3.066	0.000

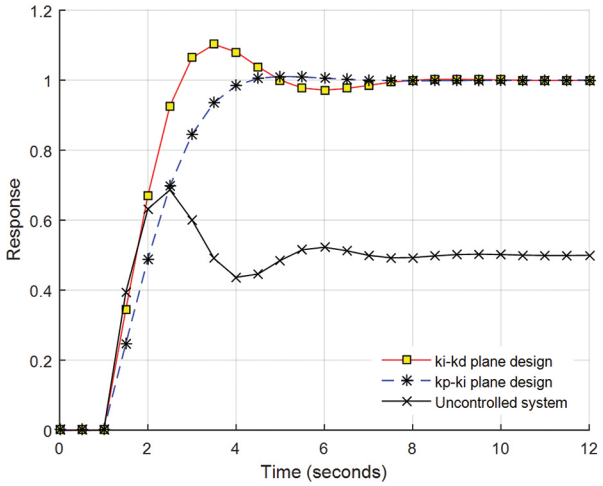

Fig. 17. The unit step response using overall optimum gains for Example 1

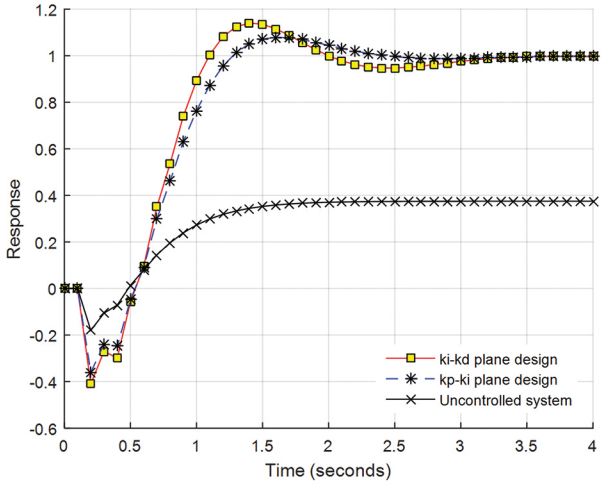

Fig. 18. The unit step response using overall optimum gains for Example 2

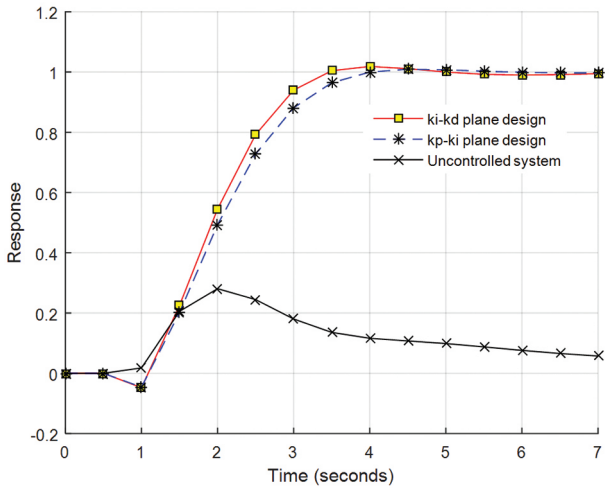

Fig. 19. The unit step response using overall optimum gains for Example 3.

It was observed that irrespective of the type and order of the system to be controlled, the k_i-k_d design plane yielded a faster response while the k_p-k_i design plane yielded a response that closely tracks the input. From these results, the system design plane can be decided by control system designers since system design specifications depend on its applications.

5. CONCLUSIONS

The parametric effects of design plane selection on the performance of PID-controlled time-delay systems were presented in this study. System stability region in the k_i-k_d and k_p-k_i planes were determined for a fixed value of k_p and k_d respectively. The study concluded that systems required controllers because their closed-loop response can never track the reference input. The controllers were designed by optimising the controller

gains using a combination of GA and graphical methods to get the overall optimum gains.

It was also concluded, that irrespective of the type and order of the system, the k_i-k_d design plane yielded a system with a faster response while the k_p-k_i design plane yielded a system response that closely track the input. Also, for a system with right-hand-side zero the k_i-k_d design plane results in a system response with a higher $\%US$ compared to the k_p-k_i design plane.

The study contributes to aiding the control system designers to select the design plane which gives the best performance right from the start of controller design without using a trial and error approach, once the system transfer function and design specifications are known.

6. REFERENCES

[1] S. Testouri, K. Saadaoui, M. Benrejeb, "Robust stabilization of a class of uncertain systems with time delay", IFAC Proceedings Volumes, Vol. 43, No. 8, 2010, pp. 553-557.

[2] L. Barhoumi, I. Saidi, D. Soudani, "Graphical method for obtaining PID parameters for systems with time delay", International Journal of Computer Science and Network Security, Vol. 19, No. 7, 2019, pp. 31-37.

[3] A. Yüce, N. Tan, D. P. Atherton, "Fractional order pi controller design for time delay systems", IFAC-PapersOnLine, Vol. 49, No. 10, 2016, pp. 94-99.

[4] J. P. Richard, "Time-delay systems: an overview of some recent advances and open problems", Automatica, Vol. 39, No. 10, 2003, pp. 1667-1694.

[5] L. M. Eriksson, M. Johansson, "PID controller tuning rules for varying time-delay systems", Proceedings of the American Control Conference, New York, NY, USA, 11-13 July 2007, pp. 619-625.

[6] A. Gupta, S. Goindi, G. Singh, H. Saini, R. Kumar, "Optimal design of PID controllers for time delay systems using genetic algorithm and simulated annealing", Proceedings of International Conference on Innovative Mechanisms for Industry Applications, Bengaluru, India, 21-23 February 2017, pp. 66 -69.

[7] N. Hohenbichler, "All stabilizing PID controllers for time delay systems", Automatica, Vol. 45, No. 11, 2009, pp. 2678-2684.

[8] F. A. Salem, "New Efficient Model-Based PID Design Method", European scientific journal, Vol. 9, No. 15, 2013, pp. 181-199.

[9] L. Ou, W. Zhang, D. Gu, "Sets of stabilising PID controllers for second-order integrating processes with time delay", IEE Proceedings-Control Theory and Applications, Vol. 153, No. 5, 2006, pp. 607-614.

[10] H. Efheij, A. Albagul, "Comparison of PID and artificial neural network controller in online of real-time industrial temperature process control system", Proceedings of the IEEE 1st International Maghreb Meeting of the Conference on Sciences and Techniques of Automatic Control and Computer Engineering MI-STA, Tripoli, Libya, 25-27 May 2021, pp. 110-115.

[11] N. B. Hassen, K. Saadaoui, M. Benrejeb, "Stabilizing lead lag controllers for time delay systems", Recent Advances on Electroscience and Computers, Vol. 1, No. 2, 2015, pp. 106-109.

[12] C. Onat, "A new design method for PI–PD control of unstable processes with dead time", ISA Transactions, Vol. 84, 2019, pp. 69-81.

[13] S. Srivastava, V. S. Pandit, "A PI/PID controller for time delay systems with desired closed loop time response and guaranteed gain and phase margins", Journal of Process Control, Vol. 37, 2016, pp. 70-77.

[14] S. E. Hamamci, "An algorithm for stabilization of fractional-order time delay systems using fractional-order PID controllers", IEEE Transactions on Automatic Control, Vol. 52, No. 10, 2007, pp. 1964-1969.

[15] M. M. Ozyetkin, C. Onat, N. Tan, "PID tuning method for integrating processes having time delay and inverse response", IFAC PapersOnLine, Vol. 51, No. 4, 2018, pp. 274-279.

[16] K. Saadaoui, S. Elmadssia, M. Benrejeb, "Stabilizing PID controllers for a class of time delay systems", PID Controller Design Approaches-Theory, Tuning and Application to Frontier Areas, IntechOpen, 2012, pp. 141-158.

[17] K. Saadaoui, A. Moussa, M. Benrejeb, "PID controller design for time delay systems using genetic algorithms", The Mediterranean Journal of Measurement and Control, Vol. 5, No. 1, 2009, pp. 31-36.

[18] A.Y. Jaen-Cuellar, R. de J. Romero-Troncoso, L. Morales-Velazquez, R.A. Osornio-Rios, "PID-controller tuning optimization with genetic algorithms in servo systems", International Journal of Advanced Robotic Systems, Vol. 10, No. 9, 2013 pp. 324-337.

[19] N. Tan, "Computation of stabilizing PI and PID controllers for processes with time delay", ISA Transactions, Vol. 44, No. 2, 2005, pp. 213-223.

[20] S. Sujoldzic, J. M. Watkins, "Stabilization of an arbitrary order transfer function with time delay using PI and PD controllers", Proceedings of the American Control Conference, Minneapolis, MN, USA, 14-16 June 2006, pp. 2427-2432.

[21] J. Zhao, M. Xi, "Self-Tuning of PID parameters based on adaptive genetic algorithm", in IOP Conference Series: Materials Science and Engineering, Vol. 782, No. 4, 2020, pp. 1-8.

[22] M. Angelova, T. Pencheva, "Tuning genetic algorithm parameters to improve convergence time", International Journal of Chemical Engineering, 2011, pp. 1-7.

[23] A. A. Chlaihawi, "Genetic algorithm error criteria as applied to PID controller DC-DC buck converter parameters: an investigation", IOP Conference Series: Materials Science and Engineering, Vol. 671, No. 1, 2020, pp. 1-10.

[24] S. Mahfoud, A. Derouich, N. EL Ouanjli, M. EL Mahfoud, M. Taoussi, "A New Strategy-based PID controller optimized by genetic algorithm for DTC of the doubly fed induction motor", Systems, Vol. 9, No. 2, 2021, pp. 1-18.

[25] O. Guenounou, B. Dahhou, B. Athmani, "Optimal design of PID controller by Multi-objective genetic algorithms", Proceedings of the International Conference on Computer Related Knowledge, Sousse, Tunisia, July 2012, pp. 1-6.

[26] K. M. Hussain, R. A. R. Zepherin, M. S. Kumar, S. M. Giriraj Kumar, "Comparison of PID controller tuning methods with genetic algorithm for FOPTD system", International Journal of Engineering Research and Applications, Vol. 4, No. 2, 2014, pp. 308-314.

[27] E. Gouthami, M. A. Rani, "Modeling of an adaptive controller for an aircraft roll control system using PID, fuzzy-PID and genetic algorithm", Journal of Electronics and Communication Engineering, Vol. 11, No. 1, 2016, pp. 15-24.

[28] S. Pareek, M. Kishnani, R. Gupta, "Comparative Analysis of GA-PID Controller for different performance indices", Proceedings of STEER 2014: ICIEEC, 2014, pp. 48-53.

[29] A. A. M. Zahir, S. S. N. Alhady, W.A.F.W. Othman, A. A. A. Wahab, M. F. Ahmad, "Objective functions modification of GA optimized PID controller for brushed DC motor", International Journal of Electrical and Computer Engineering, Vol. 10, No. 3, 2020, pp. 2426-2433.

[30] S. Atiç, E. Cokmez, F. Peker, I. Kaya, "PID controller design for controlling integrating processes with dead time using generalized stability boundary locus", IFAC-Papers Online, Vol. 51, No. 4, 2018, pp. 924-929.