SINGLE EX-CCCII BASED ELECTRONICALLY TUNABLE CURRENT MODE INSTRUMENTATION AMPLIFIER

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Abstract:

The purpose of this study is to present a new design for an electronically tunable instrumentation amplifier. The current-mode design approach is used for the proposed circuit. The proposed current-mode instrumentation amplifier employs a single Extra-X Current Controlled Current Conveyor (EX-CCCII) and a grounded resistor. This circuit design is very simple and suitable for IC integration. Because of the circuit's high output impedance, it can be cascaded with other current-mode circuits without the need for a buffer. In addition, this circuit is electronically tunable with the bias current from EX-CCCII. The proposed instrumentation amplifier provides good frequency performance with a wide bandwidth for differential gain and CMRR. The effects of non-idealities of EX-CCCII and its parasitic elements are also analysed. To validate the proposed instrumentation amplifier, various simulations are performed with the CADENCE VIRTUOSO SPECTRE simulator using 0.18 µm CMOS technology parameters.

1 Introduction

Instrumentation amplifiers (IAs) are widely used in a large number of signal processing circuits. Several applications, such as clinical instrumentation, biosensor read-out circuits, electrocardiography and signal processing, etc., have been reported that pronounce the importance of IA [1-4]. In many implementations, the IA is used as an input stage to distinguish low-magnitude differential signals from unwanted high-value common-mode signals, noise, and disturbance.

The circuit design using the current mode (CM) approach gained significant attention due to its inherent advantages such as large bandwidth, higher linearity, simple circuitry, low power consumption, etc. According to the literature, instrumentation amplifiers using the CM approach perform better than the traditional voltage mode approach, which uses three operational amplifiers (Op-amps) and seven resistors [5-6]. Conventional voltage mode IA using Op-amps requires precise resistor matching to produce a high common mode rejection ratio (*CMRR*). Current-mode instrumentation amplifiers (CMIAs) can overcome the resistance matching problem to achieve high *CMRR* and differential gain. In addition, they have better frequency response compared to conventional voltage-controlled IAs.

With the advancement in the current mode design approach, many current mode active building blocks are introduced in the literature [6-30]. Some of the mostly used active blocks are Second Generation Current Conveyor (CCII) [7, 23, 29], Current Controlled Current Conveyor (CCCII) [8, 13, 14], Differential Voltage Current Conveyor (DVCC) [9, 24], Differential Difference Current Conveyor (DDCC) [10, 30], Operational Floating Current Conveyor (OFCC) [11, 15, 16, 28], Operational Trans-resistance Amplifier (OTRA) [12], Flipped Voltage Follower (FVF) [17], Current Operational Amplifier (COA) [18, 19], Current Mirror [20], Current Differencing Trans-resistance Amplifier (CDTRA) [21], Current Follower Differential Input Trans-conductance Amplifier (CFDITA) [22], Extra-X Current Controlled Current Conveyor (EX-CCCII) [25],

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Current Differencing Current Controlled Current Conveyor (CDCCC) [26], dual z copy current differencing trans-conductance amplifier (DZC-CDTA) [27], and many more.

A review on instrumentation amplifiers shows that a number of topologies are proposed in the literature [5-30], and references cited therein. The available IAs using current mode active blocks may be further categorized based on the type of input and output signals. The IAs with voltage input are termed as Voltage-Mode (VM) [7, 9-11] or Trans-Admittance-Mode (TAM) [8, 16] if the output is available in the form of voltage or current, respectively. In contrast, the IAs with current input are termed as Current-Mode (CM) [14, 16, 18, 19] and Trans-Impedance-Mode (TIM) [12, 16] if the provided output is current and voltage, respectively. In modern integration technologies, low voltage headroom is available since supply voltages have been impressively diminished. Therefore, IA that has input and/or output as a voltage signal suffers from the limitation of low dynamic range and less output swing. Hence, the current mode IAs are preferred over voltage mode IAs. A number of CMIAs are reported in the literature however, the previously available circuits suffer from some major weaknesses:

(1) More active blocks are employed to implement the instrumentation amplifier reported in [7, 8, 11-16, 23, 25, 27-29]. This increases the chip area and power consumption of the circuit. The circuit complexity also increases due to increased active elements.

(2) The IAs reported in [11, 12, 15-18, 23, 24, 27-29] require a large number of passive elements. The passive elements used in some circuits are floating, which is not preferable for IC implementation.

(3) The instrumentation amplifiers presented in [7, 9-11, 15-17, 20, 28-30] are not electronically tunable.

(4) Some circuits mentioned in [7, 9-11, 13, 24, 28-30] do not have appropriate output impedance levels.

(5) The IAs reported in [8, 11, 12, 15-19, 23-25, 26, 28, 30] have less -3 dB frequency for *CMRR*.

(6) Some circuits have less -3 dB frequencies for differential gain [7, 11, 17, 27, 29].

This paper reports a new circuit design of the current mode IA employing a single EX-CCCII and a grounded resistor. The suggested circuit has a very simple structure and is suitable for IC integration. The proposed circuit is cascadable due to its high output impedance terminal. In addition, the circuit exhibits electronic tunability characteristics due to the internal bias current of EX-CCCII. The proposed CMIA offers wide bandwidth of differential gain and *CMRR*.

This paper is structured as: In section 1, the introduction is given. In section 2, the proposed CMIA is presented with its mathematical analysis. The impact of non-ideal EX-CCCII on the proposed CMIA is also discussed in this section. The comparative study of the proposed circuit with previously available instrumentation amplifiers is given in section 3. The performance of the proposed CMIA is verified through simulation results given in section 4. Section 5 concluded the paper.

2 Proposed circuit

2.1 Basics of EX-CCCII

The symbolic representation of EX-CCCII is depicted in Figure 1 and its internal CMOS implementation is shown in Figure 2. The relationship between input and output terminals is shown in a matrix given as,

$$\begin{bmatrix} I_{Y1} \\ V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & R_{X1} & 0 & 0 & 0 \\ 1 & 0 & R_{X2} & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}. \tag{1}$$

Where, R_{X1} and R_{X2} are internal resistances at input terminals X1 and X2, respectively. The values of these internal resistances can be expressed as,

$$R_{X1} = R_{X2} = R_X = \frac{1}{\sqrt{8\mu C_{0X}(\frac{W}{L})I_o}}. \tag{2}$$

Here μ is the mobility, C_{ox} is oxide capacitance, W/L is the aspect ratio and I_0 is the bias current of the active block. The internal resistances R_{X1} and R_{X2} can be used in place of external resistance, so the overall circuit implementation will become simple and favourable for IC implementation.

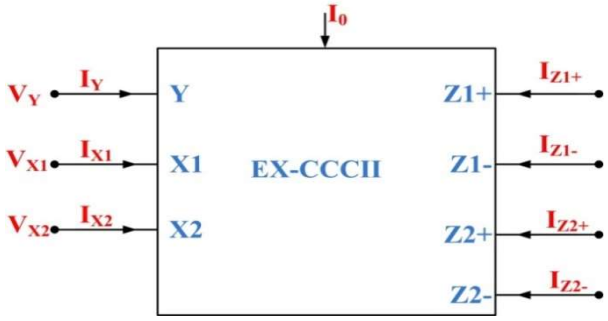


Figure 1. Symbolic representation of EX-CCCII.

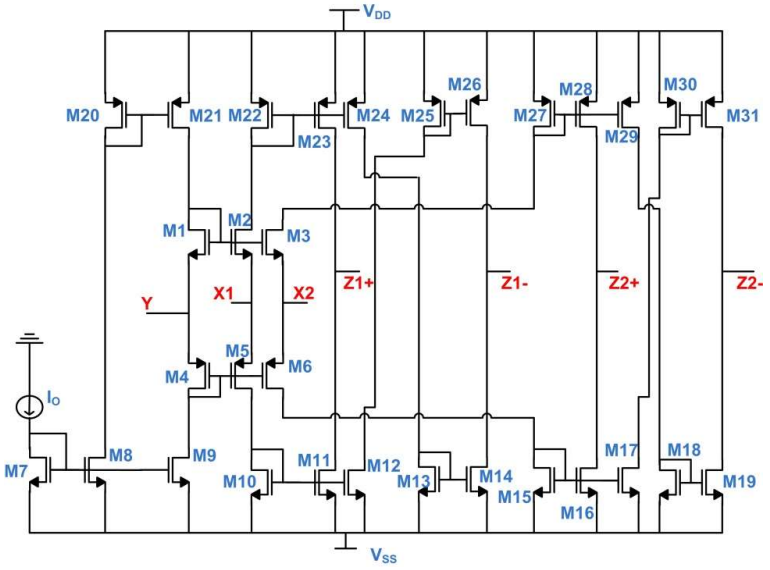


Figure 2. Internal structure of EX-CCCII.

The EX-CCCII has two current terminals (X1, X2) with low input impedance and a voltage terminal (Y) with high input impedance. All Z terminals used here are output terminals that have high output impedance. This active block has an internal bias current I_0, by which the block is electronically tunable. Multiple Z terminals can be created as needed. Additional Z+ terminals can be created by current steering circuits and negative Z terminals can be created by cross inverted current mirror circuits. The positive sign of the Z terminal indicates that the currents flowing through terminal X and terminal Z are in the same phase. However, a negative sign indicates that the current through the Z terminal is out of phase with the current flowing through the X terminal.

2.2 Current Mode instrumentation amplifier

The proposed current mode instrumentation amplifier circuit shown in Figure 3 is realized using a single EX-CCCII and a grounded resistor. The proposed circuit of CMIA has a simple structure. Two input current signals I_1 and I_2 are used to implement the proposed CMIA.

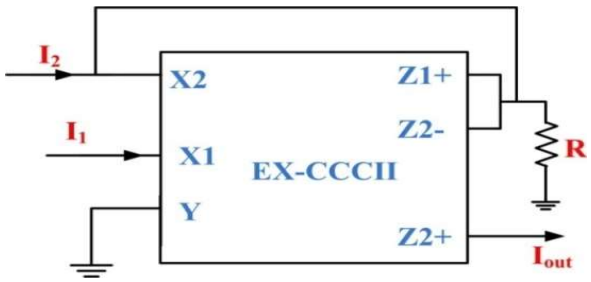


Figure 3. The schematic of the proposed CMIA.

It can be observed from Figure 3 that, $I_{X1} = I_1; V_Y = 0$.
The voltage at terminal X2 can be determined by the matrix given in (1) and can be written as,

$$V_{X2} = V_Y + I_{X2}R_{X2}. \tag{3}$$

As we know,

$$I_{Z1+} = I_{X1}\,; I_{Z2+} = I_{X2}\,; I_{Z2-} = -I_{X2}. \tag{4}$$

By analyzing the circuit shown in Figure 3, the voltage developed across resistor R or voltage at terminal X2 can be determined as,

$$V_{X2} = (I_2 - I_1)R\,. \tag{5}$$

By considering (3) and (5), the current flowing through terminal X2 can be determined as,

$$I_{X2} = \frac{R(I_2 - I_1)}{R_{X2}}. \tag{6}$$

So, the I_{out} of the proposed circuit can be determined as,

$$I_{out} = \frac{R(I_2 - I_1)}{R_{X2}}. \tag{7}$$

The differential gain (A_d) of the proposed CMIA can be determined as,

$$A_d = \frac{I_{out}}{(I_2 - I_1)} = \frac{R}{R_{X2}}. \tag{8}$$

It can be observed from (8) that the A_d of the proposed CMIA is electronically tunable with the I_0 of EX-CCCII.

2.3 Non-idealities of EX-CCCII

In this section, the influence of current and voltage gain errors on the response of the proposed instrumentation amplifier circuit is investigated. Considering non-ideal EX-CCCII, its characteristics can be rewritten as,

$$\begin{bmatrix} I_Y \\ V_{X1} \\ V_{X2} \\ I_{Z1\pm} \\ I_{Z2\pm} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ \beta_1 & R_{X1} & 0 & 0 & 0 \\ \beta_2 & 0 & R_{X2} & 0 & 0 \\ 0 & \pm\alpha_{1\pm} & 0 & 0 & 0 \\ 0 & 0 & \pm\alpha_{2\pm} & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix}. \tag{9}$$

Where, β_1 and β_2 are non-ideal voltage transfer gain coefficients from Y to X1 and X2 terminals, respectively. Whereas α_{1+}, α_{1-} are non-ideal current transfer gain coefficients from terminal X1 to Z1+ and Z1- , respectively. In a similar way, α_{2+}, α_{2-} are coefficients from X2 to Z2+ and Z2- terminals, respectively.
As explained earlier, all β coefficients are non-ideal voltage gain between X and Y terminals, whereas all α coefficients are non-ideal current gain between Z and X terminals. The non-ideal voltage and current gain [31] can be computed as in the following equations,

$$\beta(s) = \frac{\beta_0}{1+\tau_\beta s}, \tag{10}$$

$$\alpha(s) = \frac{\alpha_0}{1+\tau_\alpha s}. \tag{11}$$

Where, $\tau_\beta = \frac{1}{\omega_\beta}$ *and* $\tau_\alpha = \frac{1}{\omega_\alpha}$.

Here, ω_α and ω_β are angular pole frequencies and ideally, they are infinity. The DC voltage gain β_0 and the DC current gain α_0 are ideally unity. The DC voltage and current gain can be defined by voltage tracking error ε_β and current tracking error ε_α as stated below,

$$\beta_0 = 1 + \varepsilon_\beta \;\; and \;\; \alpha_0 = 1 + \varepsilon_\alpha. \tag{12}$$

These tracking errors are defined as, $|\varepsilon_\beta| << 1$, $|\varepsilon_\alpha| << 1$.
Considering the matrix given in (9), the voltage at terminal X2 is given as,

$$V_{X2} = \beta_2 V_Y + I_{X2} R_{X2}. \tag{13}$$

Since, $V_Y = 0$, therefore (13) is reduced as;

$$V_{X2} = I_{X2} R_{X2}. \tag{14}$$

As we know,

$$I_{Z1+} = \alpha_{1+} I_{X1} = \alpha_{1+} I_1; \quad I_{Z2-} = -\alpha_{2-} I_{X2}. \tag{15}$$

The voltage that appears at terminal X2 can be given as,

$$V_{X2} = (I_2 - \alpha_{1+} I_1 + \alpha_{2-} I_{X2} - I_{X2}) R. \tag{16}$$

Substituting (16) in (14), we get,

$$(I_2 - \alpha_{1+} I_1 + \alpha_{2-} I_{X2} - I_{X2})R = I_{X2} R_{X2}\,. \tag{17}$$

For differential mode gain,

$$I_2 = -I_1 = \frac{I_d}{2}\,. \tag{18}$$

So, by substituting (18) in (17), we get,

$$\frac{I_{X2}}{I_d} = \frac{(1+\alpha_{1+})R}{2[R_{X2} - R(\alpha_{2-} - 1)]}\,. \tag{19}$$

For common mode gain,

$$I_2 = I_1 = I_{cm}\,. \tag{20}$$

Considering (17) and (20), we get

$$\frac{I_{X2}}{I_{cm}} = \frac{(1-\alpha_{1+})R}{R_{X2} - (\alpha_{2-} - 1)R}\,. \tag{21}$$

We know that $I_{out} = I_{Z2+} = \alpha_{2+} I_{X2}$.
Then, the differential mode gain (A_d) and common mode gain (A_{cm}) can be obtained as,

$$A_d = \frac{I_{out}}{I_d} = \frac{\alpha_{2+}(1+\alpha_{1+})R}{2[R_{X2} - R(\alpha_{2-} - 1)]}\,, \tag{22}$$

$$A_{cm} = \frac{I_{out}}{I_{cm}} = \frac{\alpha_{2+}(1-\alpha_{1+})R}{R_{X2} - (\alpha_{2-} - 1)R}\,. \tag{23}$$

The *CMRR* of the proposed CMIA is given as,

$$CMRR = \frac{A_d}{A_{cm}} = \frac{(1+\alpha_{1+})}{2(1-\alpha_{1+})}\,. \tag{24}$$

It can be observed from (24) that the magnitude of *CMRR* only depends on the current transfer errors of EX-CCCII. A very high value of *CMRR* can be obtained for α_{1+} close to unity.

2.4 Effect of parasitics

The effect of parasitic elements of EX-CCCII on the response of the proposed CMIA is determined in this section. The R_{X1} and R_{X2} are very low value parasitic resistances at ports X1 and X2, respectively. Whereas parasitics R_Y//C_Y appear at port Y. Furthermore, parasitics R_{Z1+}//C_{Z1+} and R_{Z1-}//C_{Z1-} appear at ports Z1+ and Z1-, respectively while R_{Z2+}//C_{Z2+} and R_{Z2-}//C_{Z2-} are parasitics appear at terminals Z2+ and Z2-, respectively. The values of R_Y, $R_{Z1\pm}$ and $R_{Z2\pm}$ are high and that of C_Y, $C_{Z1\pm}$ and $C_{Z2\pm}$ are low.

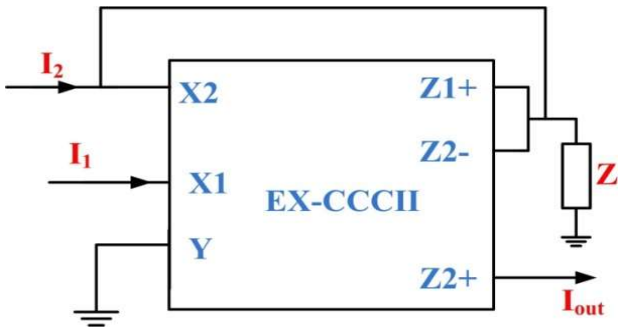


Figure 4. Proposed CMIA with parasitic elements.

The proposed current mode instrumentation amplifier under the influence of parasitic elements is given in Figure 4. To prevent mathematical complexity, some assumptions are taken into consideration and given as follows,

$$Z = \frac{R_{eq}}{1 + sR_{eq}C_{eq}}, \tag{25}$$

$$R_{eq} = R//R_{Z1+}//R_{Z2-}, \tag{26}$$

$$C_{eq} = C_{Z1+} + C_{Z2-}. \tag{27}$$

Under the parasitic influence, the voltage developed at terminal X2 is modified as,

$$V_{X2} = (I_2 - I_1)\frac{R_{eq}}{1 + sR_{eq}C_{eq}}. \tag{28}$$

By considering parasitic impedances, the I_{out} of the proposed CMIA is determined as,

$$I_{out} = (I_2 - I_1)\frac{R_{eq}}{(1 + sR_{eq}C_{eq})R_{X2}}. \tag{29}$$

Eq. (29) can be also be written as,

$$I_{out} = (I_2 - I_1)A_I \frac{1}{(1 + \frac{s}{\omega_c})}. \tag{30}$$

Here, $A_I = \frac{R_{eq}}{R_{X2}}$ *and* $\omega_c = \frac{1}{R_{eq}C_{eq}}$.

Where A_I is gain and ω_c is pole frequency of the proposed CMIA.

3 Comparative study

This section of the paper compares the proposed CMIA with the previously available IAs. A single active element based circuit is given more attention as the use of a large number of active and passive elements increases the chip area and complexity of the circuit. The IAs given in [7, 8, 11-16, 23, 25, 27-29] employ

more number of active elements, whereas circuits reported in [11, 12, 15-18, 23, 24, 27-29] employ more resistors. In modern technology, low voltage headroom is available due to reduced supply voltages. Therefore, circuits having input and/or output as voltage signal suffers from the limitation of low dynamic range and less output swing. Therefore, current mode IA is preferred over voltage mode IA. The IAs reported in [7-13,15, 17, 20, 23, 24, 28, 30] do not operate in the current mode. The electronically tunable property is absent in IAs described in [7, 9-11, 15-17, 20, 28-30]. The circuits mentioned in [7, 9-11, 13, 24, 28-30] are not cascadable as they do not have appropriate output impedance levels. Some IAs in the literature have poor frequency responses. The IAs proposed in [8, 11, 12, 15-19, 23-25, 26, 28, 30] have very low *CMRR* bandwidth whereas, circuits given in [7, 11, 17, 27, 29] have low differential gain bandwidth.

The proposed IA in this paper employs a single active element and a grounded resistor and operates in the current mode. This CMIA is electronically tunable and has a very simple structure. The proposed CMIA may be cascaded with other current mode circuits without additional buffer due to its high output impedance terminal. Furthermore, this circuit has a good frequency response.

Table 1. Comparative study.

Reference	Active block, Type , Number	No of resistors	Electronic tunability	Desired output	*Ad* (dB)	*CMRR* (dB)	-3db bandwidth (*Ad*)	-3db bandwidth (*CMRR*)	Supply voltage (V)	Power dissipation (mW)	Mode	Technology (µm)
[7]	CCII, OA, 2,2	2	No	No	0-40	55	1 MHz	---	---	---	VM	---
[8]	CCCII, 3	0	Yes	Yes	14-25	147	10 MHz	35 kHz	±2.5	---	TAM	BJT
[9]	DVCC,1	2	No	No	0-12	---	8 MHz	---	±1.5	1.74	VM	0.25
[10]	DDCC, 1	2	No	No	7-36	68	10-1 MHz	4 MHz	±0.75	0.145	VM	0.13
[11]	OFCC, 2	3	No	No	20	76	1.2 MHz	185 kHz	---		VM	---
[12]	OTRA, 3	5	Yes	Yes	26-48	64.5	10 MHz	10 kHz	±1.5	---	TIM	0.5
[13]	CCCII, 2	1 active resistor	Yes	No	16.7-28.7	51-142	70 MHz	8 MHz	±3.3		VM	0.35
[14]	CCCII, 3	1	Yes	Yes	9.6-29.8	201.8-210.9	86.1-91.9 MHz	---	±0.75	3.5-7.7	CM	0.35
[15]	OFCC, 3	2	No	Yes	14-26	93.11	10 MHz	423 kHz	±1.5	---	VM	0.5
[16]	OFCC, 4	7	No	Yes	9-23	85	20 MHz	32 kHz	±1.5	3.99	CM	0.5
[17]	FVF, 1	5	No	Yes	16-56	96	1.23 MHz	115 Hz	±1.65	0.315	VM	0.5
[18]	COA, 2	2	Yes	Yes	6.9-25	36-54.2	19.35-1.8 MHz	383-359 kHz	±0.9	0.76	CM	0.18
[19]	COA, 2	1	Yes	Yes	4.7-1.8	51.2	14.8-3 MHz	68 kHz	±0.75	0.846	CM	0.18
[20]	VB,CM, 3,1	2	No	Yes	0-18	71	85 MHz	270 MHz	±0.9	0.77	VM	0.18
[21]	CDTRA,1	2	Yes	Yes	30.8-47.6	72.6	17.8-40.7 MHz	---	±1.5	---	CM	0.18
[22]	CFDITA, 2	0	Yes	Yes	25-27.6	52.8-64.7	100 MHz	100-95 MHz	±0.9	1.15-1.3	CM	0.18
[23]	CCII, Op-amps, 2, 3	3	No	Yes	---	77	---	100 kHz	---	---	VM	---
[24]	DVCC, 2	2	No	No	---	107	---	1 kHz	±1.65	---	VM	0.35
[25]	EX-CCCII, 2	1	Yes	Yes	6.15-20.54	58	233-52.67 MHz	370 kHz	±1.25	0.502	CM	0.25
[26]	CDCCC, 1	1	Yes	Yes	73.35	93.58	44.8 MHz	5.5 kHz	± 2.5	0.132	CM	0.18
[27]	DZC-CDTA, CDTA, 1, 1	2	Yes	Yes	55-81	90.4-116.5	9.5-165 kHz	---	± 0.9	1.44	CM	0.18
[28]	OFCC, 2	5	No	No	62	99	---	10 kHz	1.2	0.022	VM	0.18
[29]	CCII, Feedback amplifier, 2, 1	4	No	No	61.1	67.9	136 Hz	---	1.8	21.94	CM	0.18
[30]	DDCC, 1	2 active resistors	No	No	0-19	146	83 MHz	100 kHz	± 0.8	0.492	VM	0.18
Proposed work	EX-CCCII,1	1	Yes	Yes	5.93-27.21	38-66.15	6.3-31.6 MHz	60-6.5 MHz	± 0.9	0.3-1.2	CM	0.18

4 Simulation results

The operation of the presented CMIA is verified using 0.18 µm UMC technology parameters. This circuit is implemented in CADENCE VIRTUOSO and simulated through the SPECTRE simulator under a supply voltage of ± 0.9 V. Table 2 indicates the aspect ratio of the transistors employed to implement the circuit shown in Figure 2.

Table 2. Transistor dimensions of EX-CCCII.

Transistors	W(µm)/L(µm)
M1-M3	10/0.5
M4-M6	18/0.5
M7-M19	12/0.5
M20-M31	20/0.5

The suggested CMIA's differential gain is determined by the external resistor value and the intrinsic resistance of EX-CCCII, which is a function of bias current I_0. As a result, the gain of the suggested CMIA can be adjusted in two ways. First, the differential gain can be changed by changing the value of the external resistor while keeping the bias current constant. Second, the gain can be adjusted by taking the resistor constant and adjusting the I_0 of the EX-CCCII. Figure 5 demonstrates how the differential gain varies with frequency at I_0=100 µA for various R values. Different values of R are taken as 2 kΩ, 5 kΩ, 10 kΩ and 20 kΩ. The simulated differential gain obtained for resistances 2 kΩ, 5 kΩ, 10 kΩ and 20 kΩ are 8.89 dB, 17.06 dB, 22.99 dB and 27.41 dB with 3-dB bandwidth of 65 MHz, 30.4 MHz, 17.86 MHz and 10.4 MHz, respectively.

The frequency response of differential gain at various bias currents is shown in Figure 6. The external grounded resistor is set to 5 kΩ to get this frequency response. For I_0 of 30 µA, 50 µA, and 100 µA, the simulated differential gain is 15.8 dB, 16.62 dB, and 17.02 dB, respectively with 3-dB bandwidth of 19.9 MHz, 22.3 MHz, and 30.4 MHz, respectively. This small deviation in the response is due to the small value of bias current.

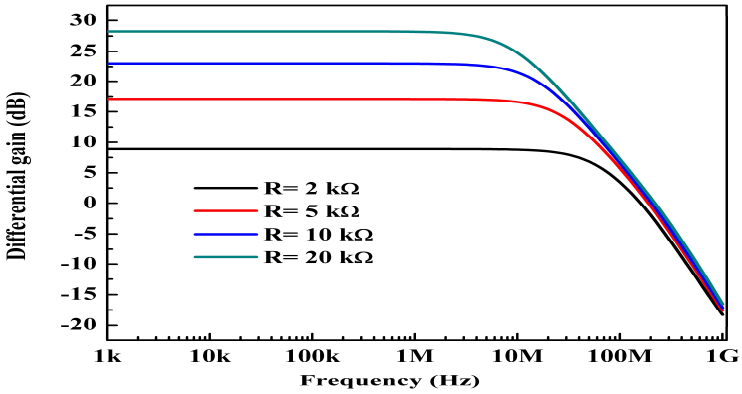


Figure 5. Differential gain of the proposed CMIA for different values of R.

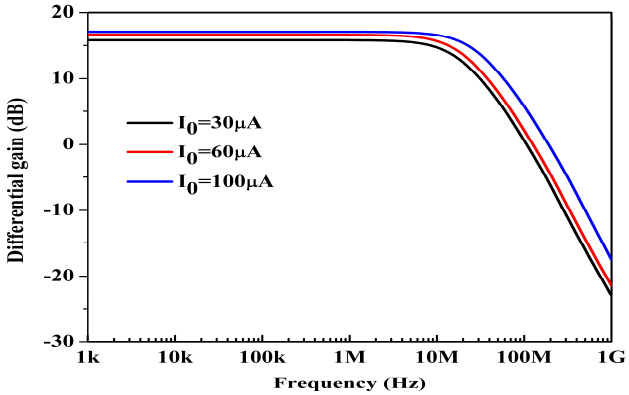


Figure 6. Differential gain of the proposed CMIA for different values of I_0.

Next, the effect of bias current on the *CMRR* of the proposed CMIA is investigated. Figure 7 shows the variation of *CMRR* with frequency at different bias currents. The value of *R* is taken as 5 kΩ. The simulated values obtained are 61.36 dB, 62.77 dB, and 63.2 dB for bias current of 30 µA, 50 µA, and 100 µA with the bandwidth of 21.8 12.1 MHz, 11.8 MHz, and 10.9 MHz, respectively.

To investigate the performance of the proposed current mode IA against mismatches, Monte-Carlo simulations are performed for 500 runs. Figure 8 indicates the Monte-Carlo histogram for maximum differential mode gain with the mean value of 16.9 dB and Figure 9 shows the histogram for maximum *CMRR* with the mean value of 63.05 dB. These histograms are obtained for I_0=100 µA and *R*=5 kΩ. The average values observed are very near to the theoretical value with a slight deviation.

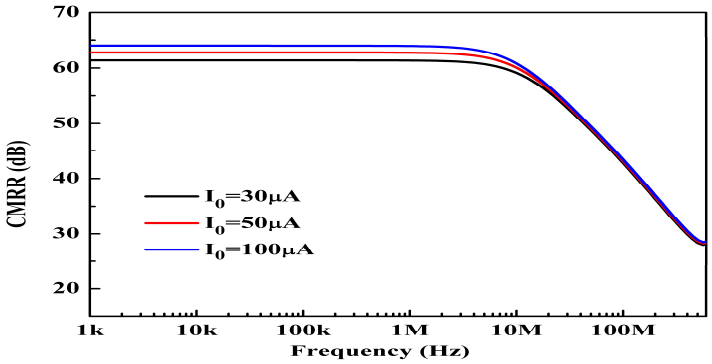


Figure 7. Variation of CMRR for different values of I_0.

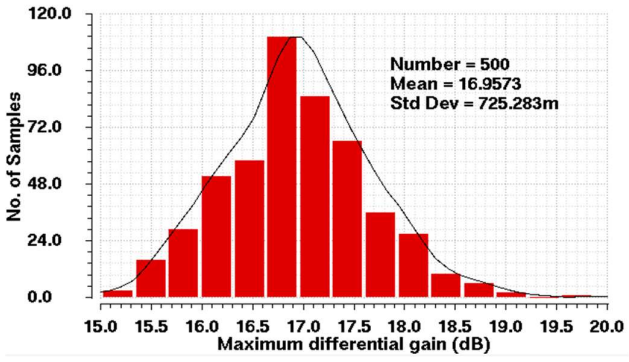


Figure 8. Monte-Carlo histogram for maximum differential gain.

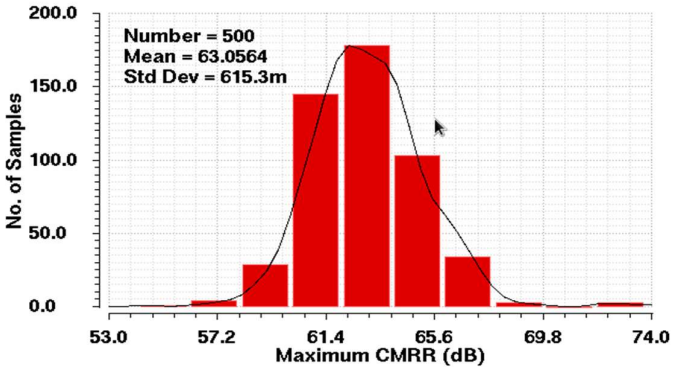
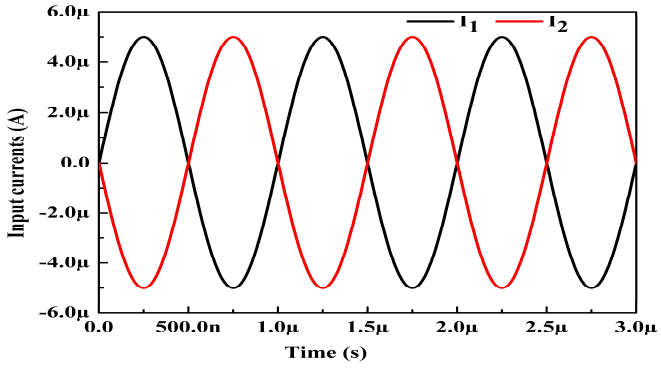


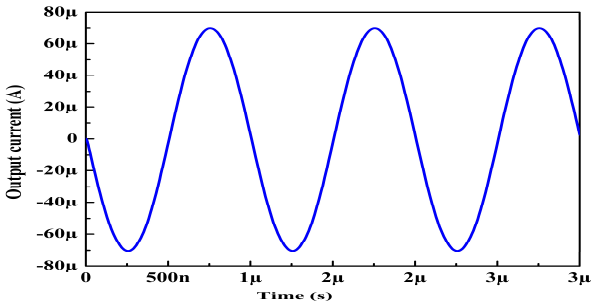
Figure 9. Monte- Carlo histogram for maximum CMRR.

The transient behavior of the proposed CMIA can be determined by applying two sinusoidal currents I_1 and I_2 in a differential manner with a peak to peak value of 10 µA and frequency of 1 MHz. As a result, the peak to peak magnitude for I_1-I_2 becomes 20 µA. The transient response of the proposed circuit is observed for I_0=100 µA and R=5 kΩ. Figure 10(a) shows the time domain input signals applied in differential mode. Figure 10(b) shows the amplified time domain output current of the proposed CMIA with an amplitude of 69.8 µA.

To test the noise immunity of the proposed CMIA, a noise analysis simulation is performed. Figure 11(a) shows the input noise with a maximum value of $6.9\text{x}10^{-10}$ A/√Hz, and Figure 11(b) shows the output noise with a maximum value of $4.89\text{x}10^{-9}$ A/√Hz at a frequency of 1 kHz. Since the maximum noise is low in magnitude therefore proposed circuit is resilient to noise. Table 3 shows input and output noise for different values of bias current at a frequency of 1 kHz and Table 4 shows input and output noise at different frequencies for I_0=100 µA.

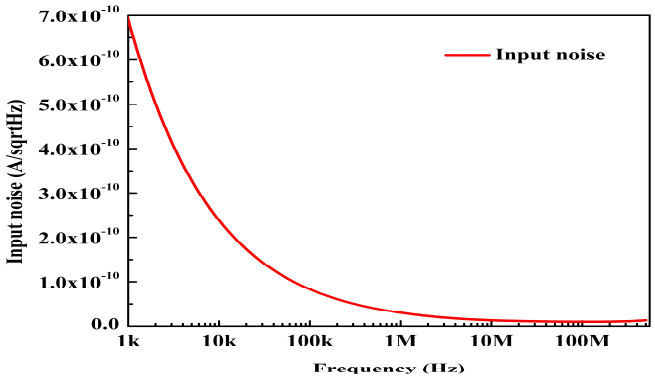


a) Input signal

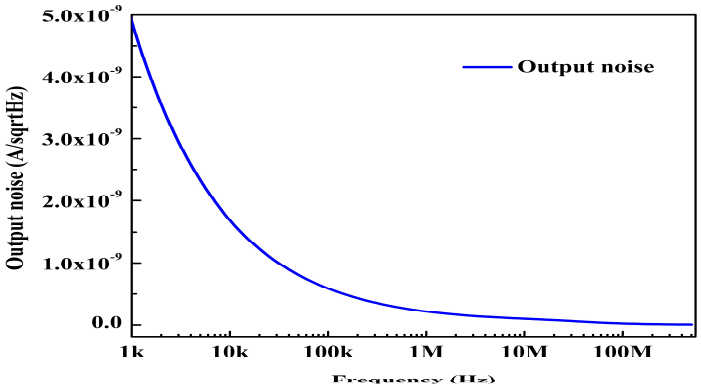


(b) Output signal

Figure 10. Time domain response of the proposed CMIA.



(a) Input noise



(b) Output noise

Figure 11. Frequency response of noise.

Table 3. Input and output noise for different bias current (I_0).

I_0	Output noise (A/√Hz)	Input noise (A/√Hz)
30µA	1.52×10^{-9}	2.48×10^{-10}
50µA	2.8×10^{-9}	3.99×10^{-10}
100µA	4.86×10^{-9}	6.9×10^{-10}

Table 4. Input and output noise at different frequency.

Frequency	Output noise (A/√Hz)	Input Noise (A/√Hz)
1 mHz	3.4×10^{-6}	4.8×10^{-7}
1 Hz	1.22×10^{-7}	1.7×10^{-8}
1 kHz	4.86×10^{-9}	6.9×10^{-10}
100 kHz	5.88×10^{-10}	8.3×10^{-11}
1 MHz	2.16×10^{-10}	3.05×10^{-11}
100 MHz	2.3×10^{-11}	1.16×10^{-11}
500 MHz	6.55×10^{-12}	1.47×10^{-11}

The impact of process corner analysis on the proposed CMIA is examined next and represented in Figure 12. The five corners used for the corner analysis are Fast-Fast, Fast-Slow, Slow-Fast, Slow-Slow, and typical. The differential gain obtained is 18.7 dB, 16.92 dB, 17.13 dB, 15.37 dB, and 17.07 dB for Fast-Fast, Fast-

Slow, Slow-Fast, Slow-Slow, and typical corners, respectively. The effect of supply voltage change on the differential gain of the proposed CMIA is shown in Figure 13. For the supply voltages of V_{DD}= -V_{SS} = 0.85 V, 0.9 V, and 0.95 V, the differential gain attained is 15.68 dB, 17.07 dB, and 18.26 dB, respectively. The effect of temperature change on the differential gain of the proposed CMIA is shown in Figure 14. For temperatures of -50^{0}C, 0^{0}C, 27^{0}C, and 50^{0}C, the simulated differential gains are 18.14 dB, 17.59 dB, 17.07 dB, and 16.67 dB, respectively. It's worth noting that the process, temperature and supply variations have a minor impact on differential gain.

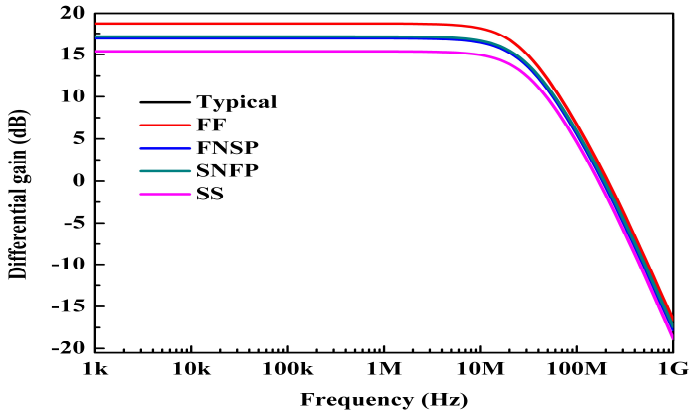


Figure 12. Process corner analysis of proposed CMIA.

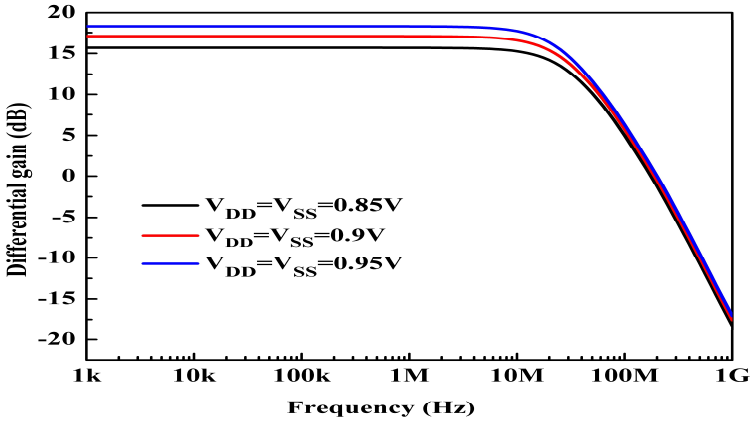


Figure 13. Supply voltage variation effect on differential gain.

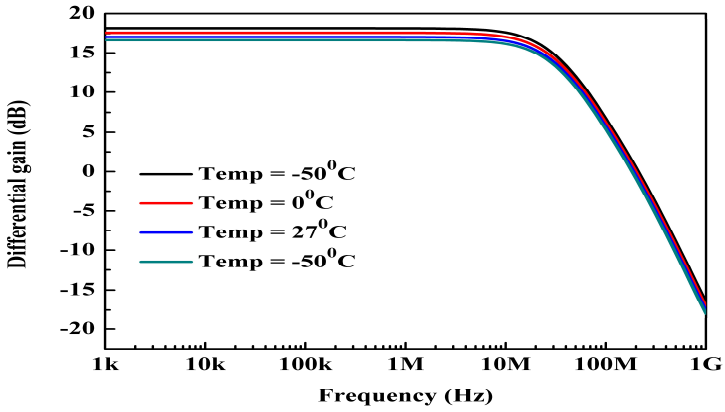


Figure 14. Temperature variation effect on differential gain.

By adjusting the peak to peak magnitude of sinusoidal differential input current, total harmonic distortion (*THD*) of the recommended CMIA at the output terminal can be observed. Figure 15 shows % *THD* at a frequency of 1 MHz for peak to peak differential input varying from 2 µA to 20 µA. The curve shows that the % *THD* increases as the differential input increases. *THD* is then measured at the output terminal for a peak to peak differential input current of 4 µA at various frequencies. The % *THD* at the output terminal is shown in Figure 16 for frequencies ranging from 1 mHz to 100 MHz. This curve indicates that the *THD* is increasing with the increase in frequency. The performance parameters of the proposed CMIA at different bias currents are summarized in Table 5.

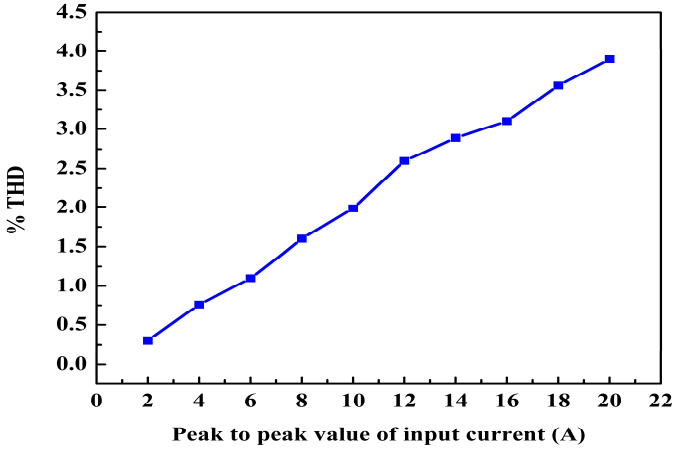


Figure 15. THD variation for different input current.

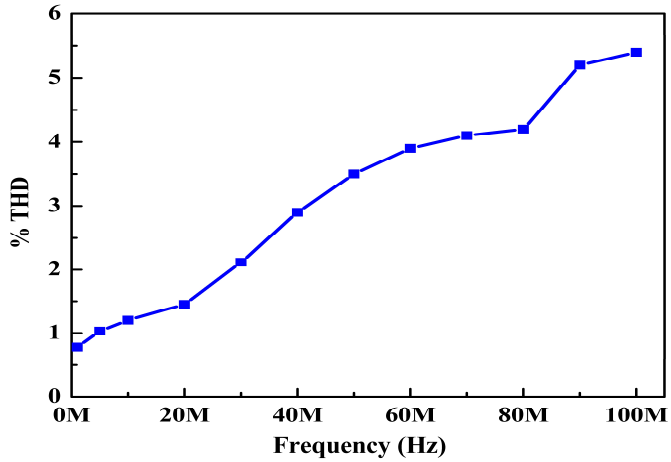


Figure 16. THD variation for different frequency.

Table 5. Performance parameters of proposed CMIA for different bias currents (I_0).

I_0	A_d (dB)	-3 dB frequency of A_d (MHz)	*CMRR* at 1Hz (dB)	*CMRR* at 100 MHz (dB)	-3 dB frequency of *CMRR* (MHz)	Power dissipation (mW)
30 µA	15.8	19.9	61.35	42.76	12.1	0.3
50 µA	16.62	22.3	62.77	43.08	11.8	0.8
100 µA	17.02	30.4	63.2	43.35	10.9	1.2

5 Conclusion

In this paper, an electronically adjustable CMIA is proposed. This CMIA uses a single EX-CCCII as the active element and a grounded resistor as the passive component. Therefore, the circuit design is simple and suitable for IC implementation. Moreover, the output terminal of the proposed CMIA is at a high output impedance, making the circuit cascadable with other current-mode circuits. The presented instrumentation amplifier has a wide differential mode bandwidth and *CMRR* bandwidth. The effects of non-idealities of EX-CCCII and parasitic elements on the performance of the proposed CMIA are also explored. Various simulations are performed to verify the performance of the proposed CMIA.

References

[1] C. Toumazou and F. J. Lidgey, "Novel Current-Mode Instrumentation Amplifier," *Electronics Letters*, vol. 25, no. 3, pp. 228-230, February 1989.

[2] G. Ferri, V. Stornelli, and A. Di Simone, "A CCII-Based High Impedance Input Stage for Biomedical Applications," *Journal of Circuits, Systems, and Computers*, vol. 20, no. 8, pp. 1441-1447, June 2011.

[3] P. Prasopsin and W. Wattanapanitch, "Design of a Low-Power High Open-Loop Gain Operational Amplifier for Capacitively-Coupled Instrumentation Amplifiers," *International Journal of Circuit Theory and Applications*, vol. 45, no. 11, pp. 1552-1575, February 2017.

[4] S. Franco, Design with Operational Amplifiers and Analog Integrated Circuit. 4th ed., San Francisco: McGraw-Hill, 2015.

[5] K. Koli, "*CMRR* Enhancement Techniques for Current-Mode Instrumentation Amplifiers", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 47, no. 5, pp. 622-632, May 2000.

[6] B. Wilson, "Universal Conveyor Instrumentation Amplifier," *Electronics Letters*, vol. 25, no. 7, pp. 470-471, 1989.

[7] S. J. Gift, "An Enhanced Current-Mode Instrumentation Amplifier," *IEEE Transactions on Instrumentation and Measurement*, vol. 50, no. 1, pp. 85-88, February 2001.

[8] S. Maheshwari, "High *CMRR* Wide Bandwidth Instrumentation Amplifier Using Current Controlled Conveyors," *International Journal of Electronics*, vol. 89, no. 12, pp. 889-896, April 2003.

[9] T. M. Hassan and S. A. Mahmoud, "New CMOS DVCC Realization and Applications to Instrumentation Amplifier and Active-RC Filters," *AEU-International Journal of Electronics and Communications*, vol. 64, no. 1, pp. 47-55, January 2010.

[10] E. Yuce, "Novel Instrumentation Amplifier and Integrator Circuits Using Single DDCC and Only Grounded Passive Elements," Indian Journal of Pure & Applied Physics, vol. 52, no. 11, pp. 767-775, June 2015.

[11] Y. H. Ghallab, W. Badawy, K. V. Kaler, and B. J. Maundy, "A Novel Current-Mode Instrumentation Amplifier Based on Operational Floating Current Conveyor," IEEE Transactions on Instrumentation and Measurement, vol. 54, no. 5, pp. 1941-1949, October 2005.

[12] R. Pandey, N. Pandey, and S. K. Paul, "Electronically Tunable Transimpedance Instrumentation Amplifier Based on OTRA," Journal of Engineering, November 2012.

[13] H. Ercan, S. A. Tekin, and M. Alçi, "Voltage-and Current-Controlled High *CMRR* Instrumentation Amplifier Using CMOS Current Conveyors," Turkish Journal of Electrical Engineering and Computer Sciences, vol. 20, no. 4, pp. 547-556, 2012.

[14] Z. M'harzi, M. Alami and F. Temcamani, "Low Voltage, High *CMRR*, and Wide Bandwidth Novel Current Mode Current Controlled Instrumentation Amplifier," Analog Integrated Circuits and Signal Processing, vol. 90, no. 1, pp. 199-205, January 2017.

[15] D. Nand and N. Pandey, "A New Proposal for OFCC-Based Instrumentation Amplifier," International Journal of Electrical and Computer Engineering, vol. 7, no. 1, pp. 134, February 2017.

[16] N. Pandey, D. Nand, and R. Pandey, "Generalised Operational Floating Current Conveyor Based Instrumentation Amplifier," IET Circuits, Devices & Systems, vol. 10, no. 3, pp. 209-219, May 2016.

[17] G. Zamora-Mejía, J. Martínez-Castillo, J. M. Rocha-Pérez, and A. Díaz-Sánchez, "A Current Mode Instrumentation Amplifier Based on the Flipped Voltage Follower in 0.50 μm CMOS," Analog Integrated Circuits and Signal Processing, vol. 87, no. 3, pp. 389-398, June 2016.

[18] L. Safari, and S. Minaei, "A Novel COA-Based Electronically Adjustable Current-Mode Instrumentation Amplifier Topology," AEU-International Journal of Electronics and Communications, vol. 82, 285-293, December 2017.
[19] L. Safari, S. Minaei, G. Ferri, and V. Stornelli, "Analysis and Design of a New COA-Based Current-Mode Instrumentation Amplifier with Robust Performance Against Mismatches," AEU-International Journal of Electronics and Communications, vol. 89, pp. 105-109, May 2018.
[20] L. Safari, S. Minaei, G. Ferri, and V. Stornelli, "A Low-Voltage Low-Power Instrumentation Amplifier Based on Supply Current Sensing Technique," AEU-International Journal of Electronics and Communications, vol. 91, pp. 125-131, July 2018.
[21] M. C. Dikbaş and U. E. Ayten, "Current and Transimpedance Mode Instrumentation Amplifier Using a Single New Active Component Named CDTRA," AEU-International Journal of Electronics and Communications, vol. 91, pp. 24-36, July 2018.
[22] B. Chaturvedi and A. Kumar, "Electronically Tunable Current-Mode Instrumentation Amplifier with High *CMRR* and Wide Bandwidth," AEU-International Journal of Electronics and Communications, vol. 92, pp. 116-123, August 2018.
[23] U. Cini, "An Enhanced Current-Conveyor Based Instrumentation Amplifier with High *CMRR*," IU-Journal of Electrical & Electronics Engineering, vol. 17, no. 2, pp. 3481-3487, July 2017.
[24] U. Cini and A. Toker, "DVCC-Based Very Low-Offset Current-Mode Instrumentation Amplifier," International Journal of Electronics, vol. 104, no. 8, pp. 1346-1357, February 2017.
[25] D. Agrawal, and S. Maheshwari, "Cascadable Current Mode Instrumentation Amplifier," AEU-International Journal of Electronics and Communications, vol. 94, pp. 91-101, September 2018.
[26] R. Das and S. K. Paul, "Current mode instrumentation amplifier with CDCCC," Analog Integrated Circuits and Signal Processing, vol. 108, no. 2, pp. 455-468, June 2021.
[27] R. Ahmad, A. Joshi, and D. Boolchandani, "A Novel Instrumentation Amplifier with High Tunable Gain and *CMRR* for Biomedical Applications," Turkish Journal of Electrical Engineering & Computer Sciences, vol. 30, no. 3, pp. 996-1015, March 2022.
[28] J. Liao, J. Yang, M. Zheng, M. S. Shiau, H. C. Wu, C. H. Cheng, and D. G. Liu, "Design of a Low-Voltage Instrumentation Amplifier at 1.2 V," In 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID), IEEE, pp. 168-171, October 2021.
[29] D. L. Shen and Y. Y. Hsu, "A Low-Mismatched Instrumentation Amplifier for ECG Front-End Readout Circuit," Analog Integrated Circuits and Signal Processing, pp. 1-7, March 2022.
[30] T. Ettaghzouti, M. Bchir, and N. Hassen, "High *CMRR* Voltage Mode Instrumentation Amplifier Using A New CMOS Differential Difference Current Conveyor Realization," International Journal of Electrical Engineering & Telecommunication, vol. 9, no. 3, pp. 132-141, May 2020.
[31] A. Fabre, O. Saaid, and H. Barthelemy, "On the Frequency Limitations of the Circuits Based on Second Generation Current Conveyors," Analog Integrated Circuits and Signal Processing, vol. 7, no. 2, pp. 113-129, March 1995.