STABILITY ANALYSIS OF VSC-HVDC SYSTEM BASED ON NEW PHASE-LOCKED-LOOP LESS VOLTAGE ORIENTED CONTROL METHOD

Guessabi Anwar[1]* – Gherbi Ahmed[1] – Chebabhi Ali[2]

[1]LAS Laboratory, Faculty of Technology, Ferhat Abbas University Setif 1, Campus El Bez, Setif 19137, Algeria
[2]EE Laboratory, Department of Electrical Engineering, Faculty of Technology, University of M'sila, 28000 M'sila, P.O.B. 166, MSila, Algeria

ARTICLE INFO	Abstract:
	Voltage Source Converters-based High Voltage Direct Current (VSC-HVDC) systems are generally implemented to transmit power across long distances due to their low cost and flexibility. This paper will discuss a new simple and low-computational-burden phase-locked loop less voltage-oriented control strategy (PLL-less-VOC strategy) for controlling and synchronizing a VSC-HVDC system in a synchronous rotating frame (dq frame). The proposed method is used not only to control the VSC-HVDC but also to obtain the mathematical model of both VSCs-based HVDC systems in the dq frame using the basics of the direct instantaneous power control theory (DPC) without using PLL and Park transformations. The proposed PLL-less-VOC strategy is equivalent to the conventional VOC strategy for steady-state stability, but it has the benefit of both conventional VOC and DPC, better transient stability performance, and low computational burden in the implementation. The experimental tests using STM32F407G microcontroller demonstrate that the proposed control strategy has better dynamic stability under certain exceptional conditions such as step changes on DC-link voltage change, powers change, and three-phase fault.

1 Introduction

Today, HVDC transmission lines are widely used to move electricity across long distances (below 700 km) [1]. The VSC-HVDC topology is characterized by other high-power converter topologies used in HVDC technology by its black start capability, grid reactive power support capabilities, and capacity to reverse the direction of power flow without changing the DC link voltage polarity [2]. Generally, the instability of HVDC transmission system is caused by rapid load demand variations and variations in renewable energy output [3]. The HVDC transmission system must respond to the load changes depending on demand to stabilize the power system and maintain acceptable system voltages. Therefore, it has been demonstrated by various studies that the control strategy used in HVDC systems directly influences the power system's stability [4]. To enhance the AC power system voltage stability, VSC-HVDC has become a viable solution. Most controllers for VSC-based HVDC systems depend on vector-oriented control (VOC) based on linear PI techniques that may be utilized indirectly to control active and reactive grids powers by regulating d-q axes currents separately, which must be in synchronism with the utility grid voltage in the case of standard VOC [5].

This synchronisation is achieved using a phase-locked loop (PLL) device, which is the widely used synchronisation method [6]. It detects the phase of VSC terminal voltage and transfers and converts this information into the d-q axes currents control loop and the firing pulses for the VSC's insulated-gate bipolar transistor (IGBT) switches through pulse-width modulation (PWM) technique [7]. However, the PLL device

---

* Corresponding author
E-mail address: anwar.guessabi@univ-setif.dz

_____

will lead to a sluggish transient response, which might cause instability in such conditions, including unbalanced grid voltages, short circuit ratios (SCRs), and mal PLL gains determination [8]–[11].

Previous research has demonstrated that the converters of HVDC system become unstable due to PLL instability in weak connections [12]. PLL gains and damping could have an impact on the VSC system's efficiency and maximum power limitations [13]. Whereas Ref. [14] illustrates through simulation that PLL gains affect the stability of a VSC with a high grid impedance, while in [15], it has been established that both large and small proportional gains of PLL may cause system instability. Results from [7] depict that with low SCRs, the gains of the PLL have a major effect on the VSC-HVDC converter functioning. Any kind of PLL failure could cause instability issues for HVDC systems. Ref. [16] focused on the PLL impact on the stability of the whole VSC system, including both the internal inner current loop and external DC-link voltage control loop. While in [17], voltage angle and power control methods were used to show the impact of PLL on the small signal stability. According to [18], the small-signal and large-disturbance stability of the DC-link voltage is decreased by the PLL dynamics. The large bandwidth of PLL could impact the small-signal stability of a VSC under a weak grid condition [19].

For such a PLL to operate successfully, the voltage at the point of common coupling (PCC) must be in phase with the VSC output voltage. Since the traditional VOC strategy uses a PLL system for the coordinate transformation under unbalanced grid voltages, its main drawback is a sluggish transient response. In addition, harmonic problems form in the weak grid due to the coupling of PLL systems and grid current control loop, which can make the system unstable [20], [21]. To solve the above-mentioned problems of the conventional VOC-based VSC-HVDC system, a new PLL-less-VOC method in the synchronous rotating frame (dq frame) is proposed in this work for a VSCs-HVDC system. The proposed method is used not only to control the currents of two grids in the dq frame but also to derive the mathematical model of both VSCs-based HVDC systems in the dq frame on the basis of the direct instantaneous power control theory (DPC) without using the PLL and Park transformation [22].

As we obtain the grid currents in the dq frame of both VSCs based HVDC systems via the new PLL-less-VOC method, the suggested strategy is expected to share the same advantages as the conventional VOC. In comparison to the conventional VOC, the proposed method improved the control performance and dynamic response of VSC-HVDC when considering the slow dynamics of PLL after neglecting Park transformation and PLL. We noticed that our proposal is identical to the methods designed in [23], [24]. However, the suggested strategy combines the benefits of the conventional VOC method and DPC method, which are: the elimination of PLL by directly calculating the grids power and so synchronizing both VSCs to the grids and the direct regulation of current to ensure optimal control performance and dynamic response which are the most common demands in the industry. In addition, the success of the suggested strategy is unaffected by the PLL mechanism, which could create instability of the system in a weak grid if it fails to predict the right grid voltage phase angle during the transient [25] - [27]. It would be interesting to add some variety instead of using an Intel CPU, the recommended technique's control method might be implemented on a Processor-In-the-Loop (PIL). The 8051, AVR, PIC, and ARM microcontroller families are only a few examples of the many possible options. Companies such as NXP, STMicroelectronics, Texas Instruments, and Silicon Labs all produce ARM microcontroller processors that are low-priced, high-performance, and power-efficient. The Cortex-M family of ARM microcontrollers is the most popular of those now available, and it is implemented in virtually all fields of activity. The details of how this card was used to create PIL co-simulation are discussed in [28] and [29]. In order to demonstrate the viability, performance, and effectiveness of our proposed control method, a PIL co-simulation of the system has been performed using the STM32F407G development board as an experimental study based on the Runge-Kutta method with a sample period of 10μsec. In the end, the theoretical predictions are quite close to what we see both in simulation and in experimentation.

The rest of the paper is structured as follows: Section II illustrates the system description of the VSC-HVDC system. In Section III, we design a PLL-less-VOC and conventional VOC strategy with mathematical demonstration. Section IV shows the simulation results using MATLAB/Simulink, in addition; we evaluate the proposed method by experimental tests using an STM32F407G microcontroller. Finally, Section V presents the conclusion of this article.

_____

2   System description

As can be seen in Figure 1, the VSC-HVDC system analyzed contains two VSCs converters connected back-to-back via DC lines [30]. The two VSCs have the same architecture but are controlled differently; one regulates the DC-link voltage (rectifier) and the other regulates the active and reactive power sent to the grid (inverter) [31]. In most cases, power transformers and an AC filter are used to connect converters to the AC grids; however, if the converter's output voltage is particularly high, the filter may be ignored. When the VSCs are switched on and off, both grids contain high-frequency harmonics that must be reduced by employing equivalent phase reactors to regulate these currents and hence both grid's active and reactive powers. VSCs ensure voltage stability because they can generate or absorb reactive power independently of the active power supplied by the system. Moreover, VSC-HVDC can quickly adjust the direction and magnitude of active power and quickly supply active and reactive power support during failures. When compared to other techniques, VSC-HVDC has many benefits such as: practically immediate (about 50-100 msec), reversal power flow, black start ability, the potential of performing islanded systems, little contribution to AC disturbances, and giving voltage and frequency support, enhancement the safety and stability of the power grid by controlling the power.
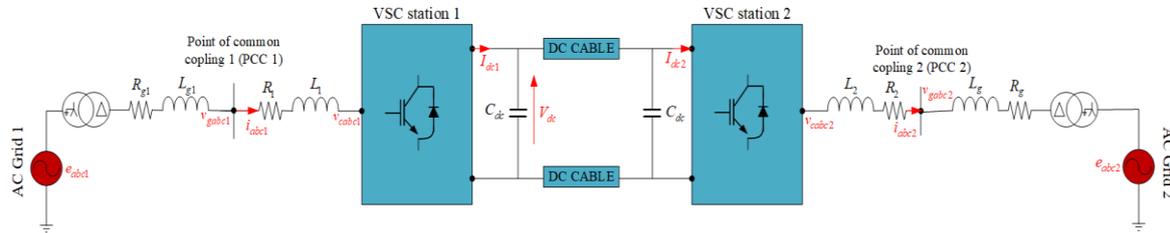
Figure 1. Structure of the VSC HVDC system studied in a simplified diagram.

3   System Basics of conventional and proposed PLL-less-VOC strategies

The stated purpose of the VSC-HVDC regulation scheme is to stabilize the oscillations of the transmission power to a minimum when the reference is changed. Another goal is to keep the DC voltage within a certain range while the equipment (mostly the power switches) is subjected to extensive operation further than the allowed voltage range [32].

3.1 VSC-HVDC system modelling using conventional VOC strategy

The conventional VOC strategy is the most adopted control method for VSC based HVDC systems in which the instantaneous voltage vector of both grids is always oriented to the d-axis current of both grids. This strategy controls both grids' currents and DC-link voltage to track their references. The conventional VOC design of the VSC-HVDC system includes the outer and inner control loops, the PLL, and the Park transformations as shown in Figure 2. This figure shows that the outer and inner control loops are commonly used to adjust the powers and currents in both grids. In the conventional VOC strategy, both grid currents are controlled separately in the dq frame by a proportional-integral (PI) controller [33]. In this section, the traditional modeling of the two VSCs based HVDC systems in the dq frame used in the design of outer and inner control loops based on Park transformation and the PLL system is presented. Accordingly, the three-phase average model of both stations that describes both VSCs voltages in the abc-reference-frame is presented:

$$v_{cabcx} = v_{g\,abcx} + L_x \frac{d\,i_{abcx}}{d\,t} + R_x i_{abcx} \tag{1}$$

where v_{gabcx} and v_{cabcx} are the three phase PCC and VSC voltages in station x (x=1,2), respectively, i_{abcx} are the three phase currents of x grid. L_x and R_x are respectively the inductance and internal resistance of the x VSC coupled filter.

_____
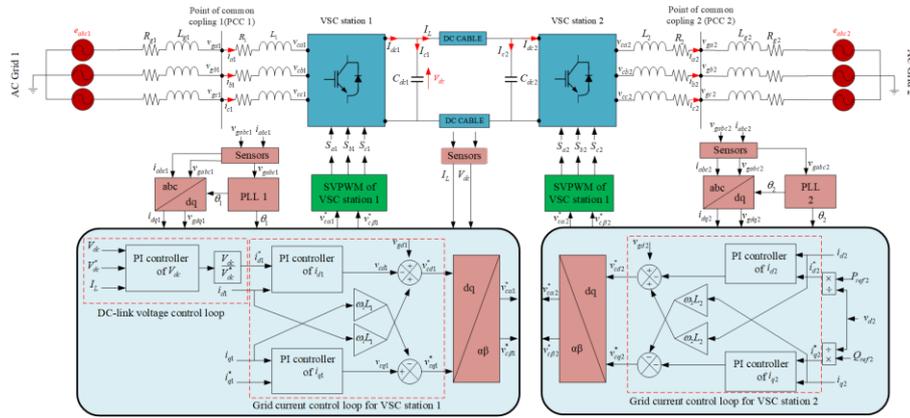
Figure 2. Block diagram of conventional VOC for VSC HVDC system.

The dynamic equations of both grids' currents in abc-reference-frame are expressed as:

$$
\begin{cases}
L_x \dfrac{d i_{ax}}{dt} = v_{cax} - v_{gax} - R_x i_{ax} \\[2mm]
L_x \dfrac{d i_{bx}}{dt} = v_{cbx} - v_{gbx} - R_x i_{bx} \\[2mm]
L_x \dfrac{d i_{cx}}{dt} = v_{ccx} - v_{gcx} - R_x i_{cx} \\[2mm]
C_{dc} \dfrac{d v_{dc}}{dt} = (S_{ax} i_{ax} + S_{bx} i_{bx} + S_{cx} i_{cx}) + I_L
\end{cases}
\tag{2}
$$

Using Park transformation, the existing model of both stations may be written in the dq frame as:

$$
\begin{cases}
\dfrac{d i_{dx}}{dt} = -\dfrac{R_x}{L_x} i_{dx} + \omega_x i_{qx} + \dfrac{v_{gdx}}{L_x} - \dfrac{v_{cdx}}{L_x} \\[2mm]
\dfrac{d i_{qx}}{dt} = -\dfrac{R_x}{L_x} i_{qx} - \omega_x i_{dx} - \dfrac{v_{cqx}}{L_x} \\[2mm]
\dfrac{d v_{dc}}{dt} = \dfrac{v_{gdx}}{C_{dc} V_{dc}} i_d + \dfrac{V_{dc}}{C_{dc} R_L}
\end{cases}
\tag{3}
$$

where i_{dx} and i_{qx} are the d-q axes grids currents respectively, v_{cdx} and v_{cqx} are the d-q axes converters voltages respectively.

Using Concordia transformation, the equation (1) may be written in the stationary reference frame (αβ-frame) as:

$$
\begin{cases}
v_{cax} = v_{gax} - R_x i_{ax} - L_x \dfrac{d i_{ax}}{dt} \\[2mm]
v_{c\beta x} = v_{g\beta x} - R_x i_{\beta x} - L_x \dfrac{d i_{\beta x}}{dt}
\end{cases}
\tag{4}
$$

where v_{gax} and $v_{g\beta x}$ indicate the x grids voltages, i_{ax}, and $i_{\beta x}$ are the x grids currents, and v_{cax}, $v_{c\beta x}$ represent the x VSC voltages in the αβ frame.

3.2 VSC-HVDC system modelling using PLL-less-VOC strategy

In this work, we take a close look at the advantages and disadvantages of the proposed PLL-less-VOC and traditional VOC, both are developed in the dq frame for a three-phase VSC. Since there is no PLL involved, PLL-less-controller may achieve the same steady-state performance as VOC while also providing superior tracking performance, low complexity, low dependence on system parameters, minimal ripple in power response, and constant switching frequency while maintaining a fast dynamic response [34]. The absence of Park transformation and PLL mechanism in PLL-less-controller also means that it requires fewer computing resources to implement than VOC. As a result, the PLL-less-control approach shown in Figure 3 might be adapted to address new challenges in a wide range of industries.
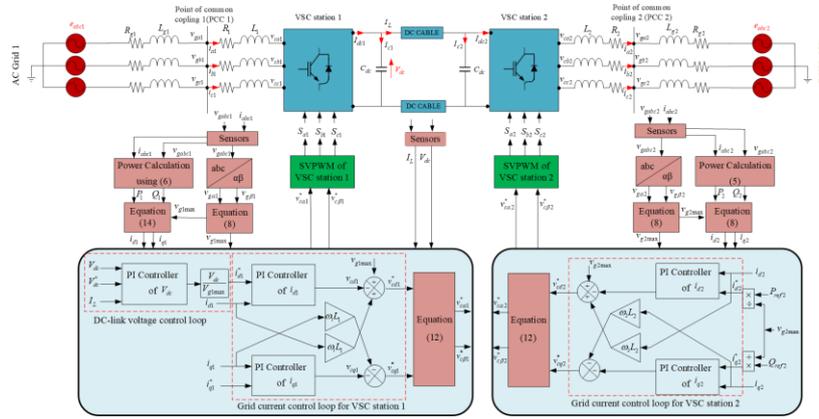
Figure 3. A block diagram of the proposed PLL-less-control strategy for VSC HVDC system.

In this section, the model of VSC based HVDC systems is determined based on DPC modeling without using the synchronization method and the Park transformations using the instantaneous power theory concept, as follows:

Both grids' active and reactive power can be given in the three-phase reference frame based on a sequence of three-phase grids voltages and currents, as shown in (5):

$$\begin{cases} P_x = v_{gax}i_{ax} + v_{gbx}i_{bx} + v_{gcx}i_{cx} \\ Q_x = \frac{1}{\sqrt{3}}\left[(v_{gbx}-v_{gcx})i_{ax} + (v_{gcx}-v_{gax})i_{bx} + (v_{gax}-v_{gbx})i_{cx}\right] \end{cases} \quad (5)$$

In the αβ-frame, both the instantaneous active and reactive powers (P_x and Q_x) of x grid are represented by:

$$\begin{cases} P_x = v_{g\alpha x}i_{\alpha x} + v_{g\beta x}i_{\beta x} \\ Q_x = v_{g\alpha x}i_{\alpha x} - v_{g\beta x}i_{\beta x} \end{cases} \quad (6)$$

Both grid voltages in the αβ-frame can be obtained by considering a non-distorted grid as:

$$\begin{cases} v_{g\alpha x} = V_{gx\max}\cos(\omega_x t) \\ v_{g\beta x} = V_{gx\max}\sin(\omega_x t) \end{cases} \quad (7)$$

where $\omega_x = 2\pi f_x$ is the x grid voltage angular frequency, and $V_{gx\max}$ symbolizes the x grid voltage magnitude, which given by:

$$V_{gx\max} = \sqrt{v_{g\alpha x}^2 + v_{g\beta x}^2} \tag{8}$$

By deriving equation (7), the grid voltage dynamics in the αβ-frame are obtained as follows:

$$\begin{cases} \dfrac{dv_{g\alpha x}}{dt} = -\omega_x v_{gx\max}\sin(\omega_x t) = -\omega_x v_{g\beta x} \\[2mm] \dfrac{dv_{g\beta x}}{dt} = \omega_x v_{gx\max}\cos(\omega_x t) = \omega_x v_{g\alpha x} \end{cases} \tag{9}$$

Using the power-current equation in (5), and equations (6) and (7), we get the model of dynamic powers in state space of the instantaneous active and reactive powers that may be expressed as:

$$\begin{cases} \dfrac{dP_x}{dt} = \dfrac{R_x}{L_x}P_x - \omega_x Q_x + \dfrac{1}{L_x}(v_{g\alpha x}v_{c\alpha x} + v_{g\beta x}v_{c\beta x} - v_{gx\max}^2) \\[2mm] \dfrac{dQ_x}{dt} = \omega_x P_x - \dfrac{R_x}{L_x}Q_x + \dfrac{1}{L_x}(v_{g\beta x}v_{c\alpha x} - v_{g\alpha x}v_{c\beta x}) \end{cases} \tag{10}$$

where $v_{c\alpha x}$ and $v_{c\beta x}$ represent the voltage control of each converter and P_x and Q_x served as outputs.

$$\begin{cases} U_{Px} = v_{g\alpha x}v_{c\alpha x} + v_{g\beta x}v_{c\beta x} \\[2mm] U_{Qx} = v_{g\beta x}v_{c\alpha x} - v_{g\alpha x}v_{c\beta x} \end{cases} \tag{11}$$

where U_{Px} and U_{Qx} are the new inputs of the control for x grid converter.

By using equation (7), the new inputs of the control U_{Px} and U_{Qx} given in equation (11) are changed into dq-frame as follows:

$$\begin{bmatrix} U_{Px} \\ U_{Qx} \end{bmatrix} = V_{gx\max}\begin{bmatrix} \cos(\omega_x t) & \sin(\omega_x t) \\ \sin(\omega_x t) & -\cos(\omega_x t) \end{bmatrix}\begin{bmatrix} v_{c\alpha x} \\ v_{c\beta x} \end{bmatrix} = V_{gx\max}\begin{bmatrix} v_{cdx} \\ v_{cqx} \end{bmatrix} \tag{12}$$

where v_{cdx} and v_{cqx} are the x VSC voltages in the dq-frame, it is important to keep in mind that the PLL is not used in the approach described in (10), but that the inputs are still reflected in the dq-frame.
Substituting (11) and (12) into (10), we may rewrite the relationship of real and reactive powers as:

$$\begin{cases} \dfrac{dP_x}{dt} = -\dfrac{R_x}{L_x}P_x - \omega_x Q_x + \dfrac{1}{L_x}(V_{gx\max}v_{cdx} - V_{gx\max}^2) \\[2mm] \dfrac{dQ_x}{dt} = \omega_x P_x - \dfrac{R_x}{L_x}Q_x + \dfrac{1}{L_x}(V_{gx\max}v_{cqx}) \end{cases} \tag{13}$$

Since the synchronous frame has a d-axis which coincides with the instantaneous voltage vector $v_{gdx} = V_{gx\max}$ and a q-axis which is in quadrature with it $v_{gqx} = 0$, therefore the following expressions can be used in the dq-frame, to calculate the active and reactive powers:

$$\begin{cases} P_x = V_{gx\max}i_{dx} \\[2mm] Q_x = -V_{gx\max}i_{qx} \end{cases} \tag{14}$$

By substituting (14) into (13) and multiplying both sides by $1/V_{gx\max}$, we obtain the new model:

$$\begin{cases} \dfrac{di_{dx}}{dt} = -\dfrac{R_x}{L_x}i_{dx} - \omega_x i_{qx} + \dfrac{1}{L_x}(v_{cdx} - V_{gx\max}^2) \\ \dfrac{di_{qx}}{dt} = \omega_x i_{dx} - \dfrac{R_x}{L_x}i_{qx} + \dfrac{1}{L_x}v_{cqx} \end{cases} \tag{15}$$

According to the obtained model in (15), there are coupling terms between the d-axis grid current i_{dx} and the q-axis grid current i_{qx}. These coupling terms are mitigated using the PI controllers which are represented in the next subsection.

3.3 Grids Currents regulations based on both control strategies

In this section, both control strategies, traditional VOC and the proposed PLL-less-VOC in the dq-frame based on a simple linear PI controller are represented and analyzed. The mains advantages of the current controller are: better power quality as the current-controller converter is less influenced by grid harmonics and disturbances, decoupled control of active and reactive powers, and the control mode can be easily extended to compensate for line harmonics and other power quality issues.

The system in (15) should be modified to include HVDC converters voltages components in the dq frame obtained from the grids and feed-forward terms to eliminate the cross-coupling as shown below:

$$\begin{cases} v_{cdx}^* = \underbrace{u_{dx}}_{\text{feedback}} - \underbrace{\omega_x L_x i_{qx} + V_{gx\max}}_{\text{feedforward}} \\ v_{cqx}^* = \underbrace{u_{qx}}_{\text{feedback}} + \underbrace{\omega_x L_x i_{dx}}_{\text{feedforward}} \end{cases} \tag{16}$$

The output control variables of both PI controllers used in the two grid current loops of both control strategies are given in the subsequent expression:

$$u_{dqx} = (k_{p-c} + \dfrac{k_{i-c}}{s})(i_{dqx} - i_{dqx}^*) \tag{17}$$

From these equations, it is clear that the d-axis grid current i_{dx} and the q-axis grid current i_{qx} can be regulated by the decoupled control variables u_{dx} and u_{qx} separately.
where k_{p_c} and k_{i_c} are the proportional and integral gains of the PI controllers, which are calculated using the pole placement method as follows:

$$\begin{cases} k_{p-c} = 2L_x \xi_c \omega_{n-c} \\ k_{i-c} = L_x \omega_{n-c}^2 \end{cases} \tag{18}$$

where ω_{n-c} and ξ_c are respectively the natural frequency and the damping factor of both grids currents PICs,

The damping factor is chosen as $\xi_c = 1$ for the appropriate transient process, and the natural frequency is chosen as $\omega_{n-c} = 500$ rad/s for the adjustment between dynamic responses and immunity versus grid distortion, and grid currents ripples.

The second grid references currents i_{dq2}^* are provided from the references grids active and reactive powers through the open-loop control using (14) as:

_____

$$\begin{cases} i_{dx}^* = \dfrac{P_x^*}{V_{gx\max}} \\[3ex] i_{qx}^* = \dfrac{Q_x^*}{V_{gx\max}} \end{cases} \tag{19}$$

The second grid reactive power reference Q_2^* is set to zero to ensure unity power factor and compensate the reactive power in the second grid, when the first grid reference current i_{d1}^* are provided from the control of DC link voltage as presented in the next subsection.

3.4 DC-link voltage regulation

The main purposes of DC-link voltage regulation are to ensure that it follows its reference without error, to control the balanced power exchange between the DC side and both AC sides, and to provide the first grid active reference current i_{d1}^*, which is achieved through an external control loop as shown in Figures 2 and 3.

By regulating the DC link voltage, the first VSC ensures that the active power present in the DC grid is transported to the AC grids. As a result, the VSC serves as an energy storage device between the DC and AC sides, where any unbalance between the AC and DC powers causes a voltage fluctuation across the DC capacitor. The DC-link capacitor current reference, obtained from the regulation of DC-link voltage, is expressed as:

$$I_c^* = (V_{dc}^* - V_{dc})(k_{p\_v} + \frac{k_{i\_v}}{s}) \tag{20}$$

k_{p_v} and k_{i_v} are the proportional and integral parameters of the closed loop DC-link voltage PI controller of the first VSC station, which are calculated using the pole placement method as:

$$\begin{cases} k_{p\_v} = 2C_{dc}\xi_v\omega_{n\_v} \\ k_{i\_v} = C_{dc}\omega_{n\_v}^2 \end{cases} \tag{21}$$

ω_{n_v} and ξ_v are the cut-off frequency and the damping factor of the DC-link voltage PI controller of the x grid, respectively.

The DC side reference current is given by:

$$I_{dc}^* = I_c^* + I_L \tag{22}$$

where I_L is the measured DC line current.

To guarantee the balanced power exchange, the active powers of the AC sides are given in terms of DC power by:

$$P_{dc}^* = P_x^* \tag{23}$$

where $P_{dc}^* = I_{dc}^* V_{dc}$ and $P_x^* = i_{dx}^* V_{gx\max}$ are respectively the DC power and AC sides active powers.

Knowing the DC current reference and equalizing the powers of the AC and DC sides, the first active reference current i_{d1}^* of the network is calculated as follows:

$$i_{d1}^* = \frac{V_{dc}}{V_{g1\max}} I_{dc}^* \tag{24}$$

The first reactive reference current i_{q1}^* of the network is set to zero to ensure unity power factor and compensate the reactive power in the first grid.

_____

The original reference VSCs voltages $v_{c\alpha\beta x}$ of both VSCs in the αβ-frame can be obtained using the inverse of equation (12) and the reference VSCs voltages v_{cdqx} in equation (16) as follows:

$$\begin{bmatrix} v_{c\alpha x}^* \\ v_{c\beta x}^* \end{bmatrix} = \frac{1}{V_{gx\max}} \begin{bmatrix} v_{g\alpha x} & v_{g\beta x} \\ v_{g\beta x} & -v_{g\alpha x} \end{bmatrix} \begin{bmatrix} v_{cdx}^* \\ v_{cqx}^* \end{bmatrix} \tag{25}$$

4   Results and discussion

The studied system depicted in Figure 1 and its control illustrated in Figure 2 and 3 are simulated in MATLAB/Simulink environment, to study the VSC-HVDC dynamic behaviour and evaluate the responsiveness of the proposed control, under different conditions and transients. All simulation results are implemented and validated using an STM32F407G development board as illustrated in Figure 4 with its PIL structure. Detailed parameters of VSC-HVDC system are provided in Table 1.

The STM32F407VG has 1MB of flash storage, a 32-bit ARM®-Cortex®-M4F-CPU, a Digital-Signal-Processor (DSP), a Floating-Point Unit (FPU), and 192kB SRAM with a maximum operational frequency of 168 MHz.

Table 1. Values of system and simulation parameters

Parameter	Value
Maximal voltage of both AC source	31.1 kV
The fundamental frequency of both grids	50, 60 Hz
DC-link voltage V_{dc}	90 kV
Capacitor of DC link C_{dc}	6 mF
DC cable resistance R	5 Ω
filter inductances L_1, L_2	0.006 mH
filter resistances R_1, R_2	0.25 Ω
Switching frequency f_s	8 kHz
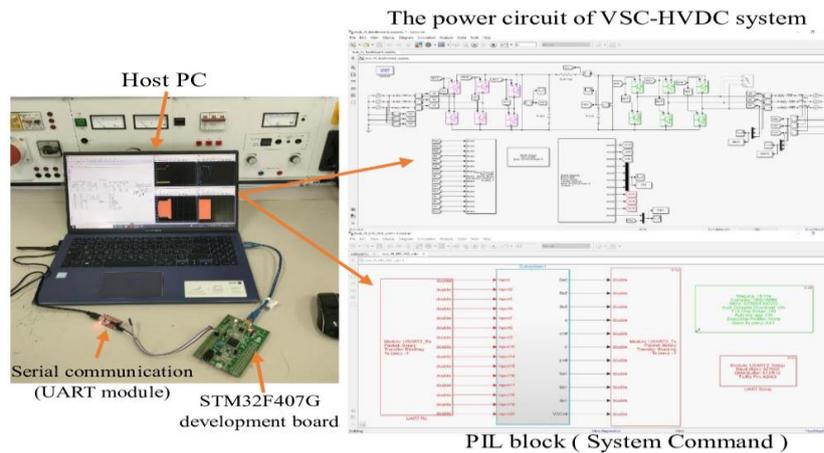
Figure 4. Structure of the VSC-HVDC system using an STM32F407G microelectronic.

The suggested PLL-less-control approach for VSC-HVDC systems is realized by integrating all control algorithms into a new single control circuit and specifying the required microcontroller and the inputs/outputs of the proposed PLL-less-VOC strategy in MATLAB/Simulink. The proposed control circuit's algorithms are transformed into C code from the simulation model using Simulink Blockset (Waijung). As illustrated in Figure 4, we combine the created C code in the PIL block into a new Simulink model to run the suggested control strategy on the STM32F407G development board through a serial connection interface (UART module) [30]. After that, the microcontroller calculates the VSC-HVDC's state vectors and transmits them to

_____

the host PC, which stores the Simulink power circuit of the VSC-HVDC through the same serial connection interface for operating it (Figure 4).

The following simulation scenarios are used to test the model:

Test 1 (Impact of PLL on system stability): This scenario investigates the effect of change in ω_{n_v1} while keeping the nominal value of ζ_{v1} on system dynamics.

Test 2 (dynamic behavior of the system under different grid conditions): The adaptability of the suggested control is tested against active and reactive power reference variation and direct voltage reference variation.

Test 3 (dynamic behavior of the system under three phase fault): In this test, the adaptability of the suggested control is tested against three phase faults.

4.1 Test 1. Impact of PLL on system stability

In this part, we illustrate how the PLL and its control settings affect the stability of VSC HVDC systems. The PLL is a phase-tracking control system that operates in real time. Its purpose is to guarantee system stability by ensuring that the angle of rotation at the PLL's output θ_{PLLx}, is in ideal phase with the signal at the point of common coupling, θ_{PCCx}. In this study, we just cover the most fundamental ideas about how PLL dynamics impact the effect of DC-link voltage regulation and how PLL might enhance DC-link voltage stability. Figure 5 depicts the DC-link voltage response of VSC HVDC with different values of ω_{n_v1} considering ζ_{v1} at nominal condition.
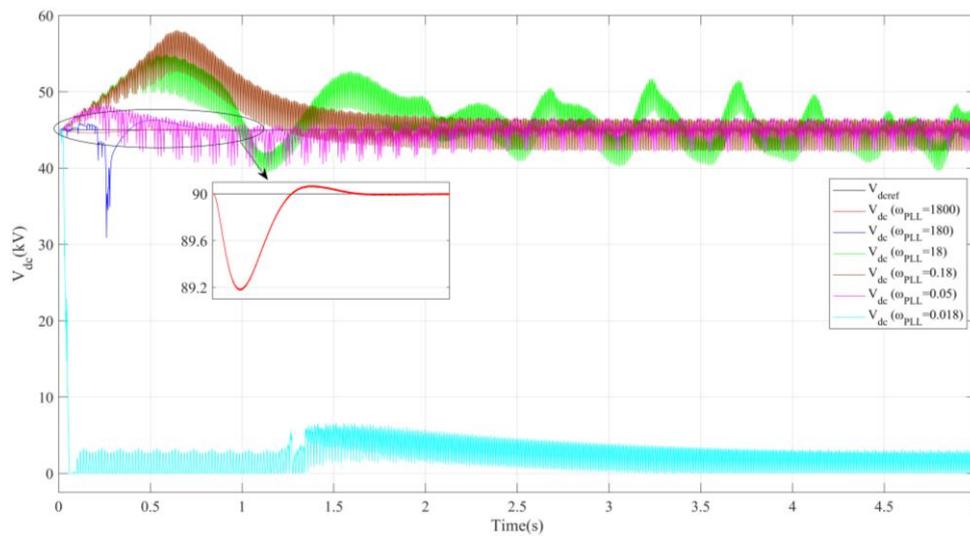
Figure 5. Response of DC-link voltage of VSC HVDC with various PLL bandwidths

Results in Figure 5 show that, particularly at high value of ω_{n_v1} (e.g., for the case of ω_{n_v1} =800 rad/s), the VSC system works well and the tracking error almost converges to zero. It can be noted that increasing the value of ω_{n_v1} improves DC-link voltage stability. For lower value of ω_{n_v1} ($\omega_{n\_v1} = 0.018$, 0.05, 0.18, 18, 180 rad/s), it greatly affects the operation of the VSC-HVDC converter which causes DC-link voltage instability; there is a big failure in tracking performance. So, it is clear that a negative effect on VSC HVDC system stability results from a variation in ω_{n_v1}, since voltage instability in DC converters is occurred which reduces the maximum power transfer capability of the VSC converters.

Considering ζ_{v1} at a nominal state, Figure 6 shows the power deviations in VSC HVDC transmission lines over a range of ω_{n_v1} values. It is obvious that the system becomes unstable as ω_{n_v1} decreases and more oscillations will appear.

_____
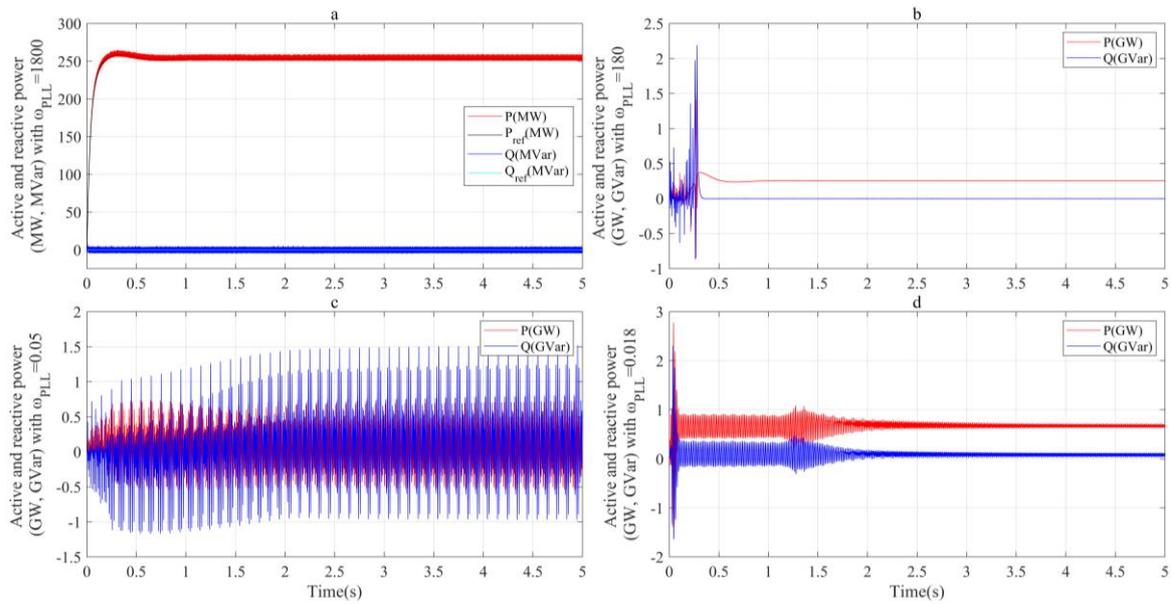
Figure 6. Response of power deviations in VSC HVDC with various PLL bandwidths.

4.2 Test 2. Dynamic performance of system under different grid conditions

In order to study the dynamic stability of the proposed control technique, a comparative study between the conventional VOC and proposed PLL-less-VOC strategy was achieved, during sudden change of active and reactive power reference from 250 to 300 MW at 1.5 sec and from 0 to 50 MVAR at 2.5 sec, respectively, and DC-link voltage reference variation from 90 to 92 kV at 3.5 sec are performed. The oscillation magnitude values for each dynamic response (V_{dc}, P, and Q) are analyzed and illustrated in Figures 7 and 8.
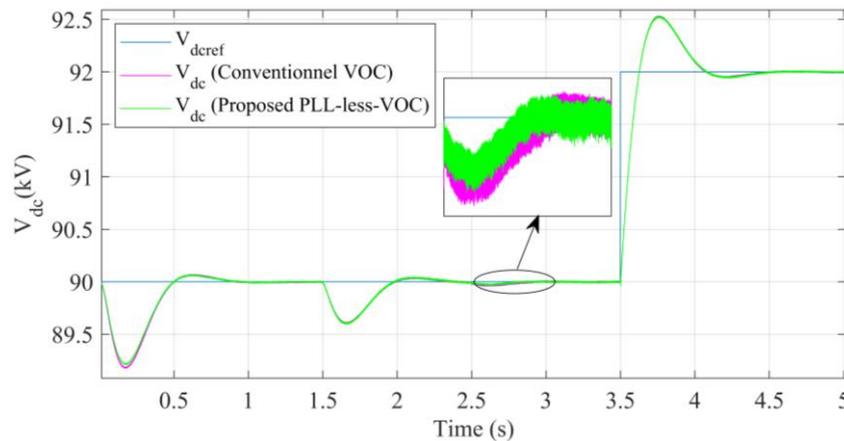
Figure 7. Responses of DC-link voltage under the second test.

Figure 7 illustrates the responses of the DC-link voltage under second test. At the start of the simulation, a little drop of about 0.8 kV smaller than the reference of 90 kV can be noticed in the system output for both controllers with little reduction of their oscillation by using the PLL-less-controller as shown in Figure 7. This is due to the fact that the system is just starting out and the controller is starting from 0V, then the system stabilizes out in about 1.15 sec. The DC-link voltage also drops and stabilizes after 0.5 sec when the active power reference is changed using both controllers, the DC-link voltage also varies slightly with the change of reactive power reference, but both controllers try to adjust the direct voltage V_{dc} to follow the reference. This is evident in the zoomed portion shown in Figure 7. In addition, at 3.5 sec the DC-link voltage reference is changed from 90 to 92 kV, and the direct voltage trucks its reference with an overshoot of 0.5 kV and stabilized

_____

after 1 sec for both control strategies. In conclusion, the proposed control technique is identical to the traditional control technique.
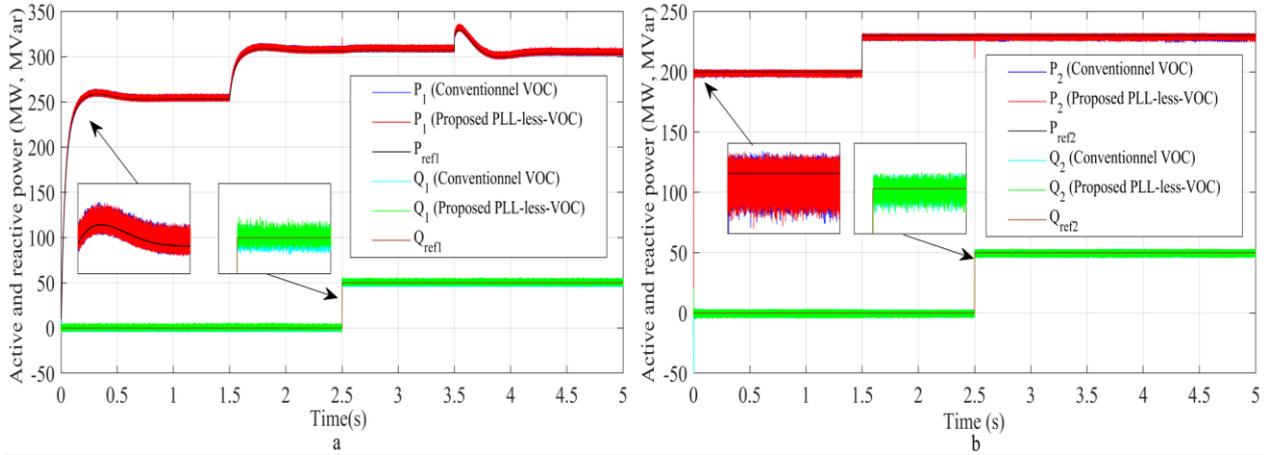
Figure 8. Responses of active and reactive power transmitted in both grids under the second test: a- P₁ and Q₁ of grid 1, b- P₂ and Q₂ of grid 2.

The active power reference in VSC-HVDC station 2 is instantly changed at 1.5 sec from 200 to 250 MW, we observe that the active power of the HVDC station 2 correctly trucks the reference and stabilized at the new reference value using both controllers, the reactive power is not affected. Also, at 2.5 sec, the reactive power reference in VSC-HVDC station 2 is suddenly changed from 0 to 50 MVAR, the system reactive power Q follows the desired reactive power Q_{ref}. Furthermore, the active and reactive powers are not affected at 3.5 sec with the changing of the direct voltage reverence as shown in Figure 8(a). Figure 8(b) shows that the active power reference in VSC-HVDC station 1 is changed at 1.5 sec from 250 to 300 MW when the active power reference in VSC-HVDC station 2 is instantly changed at 1.5 sec from 200 to 250 MW, but at 3.5 sec with the change of direct voltage reference, an overshoot of 0.38 kV of active power occurs and return to the controlled range after 0.55 sec.

The reactive power is still not affected until the reactive power reference variation at 2.5 sec. After this change, the reactive power trucks its reference. This tracking can be observed to be very rapid with almost 0 percentage overshoot. This is due to the fact that the control signal for Q has fewer variables it depends on.

_____
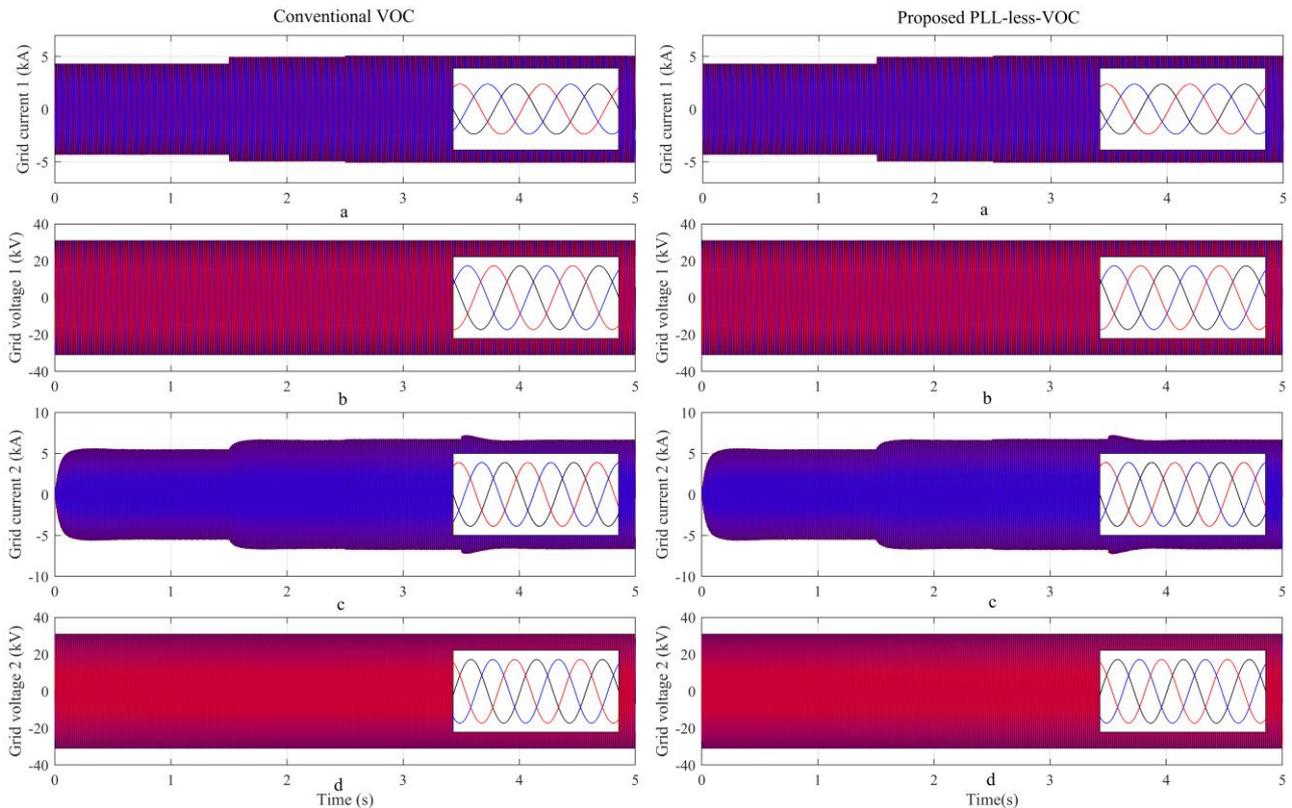
Figure 9. Responses of both grids voltages and currents using both control strategies under the second test.

Figure 9 shows the current and voltage in both grids during the second test. The voltages in grid 1 and 2 unaffected by the active, reactive power step and DC-link voltage step for both controllers. In the other hand, the current displays a transient to adjust the variations step which produce the variation in phase angle. The grid voltages and currents for both controllers are sinusoidal. This is clearly shown in the zoomed portion in the Figure 9.

As conclusion, this figure shows that the responses of the DC voltage, active and reactive power using the conventional VOC or the PLL-less-VOC strategy are identical and the control loops are really successful.

4.3 Test 3. Dynamic performance of the system under three phase faults

In order to demonstrate the superiority of the suggested PLL-less strategy over the standard PLL-based control (standard VOC strategy), a three-phase fault of 150 msec is imposed to the grid 1 at t = 1.4 sec, the responses of voltages and powers of VSC-HVDC system are achieved for two types of topologies as shown in Figure 10.
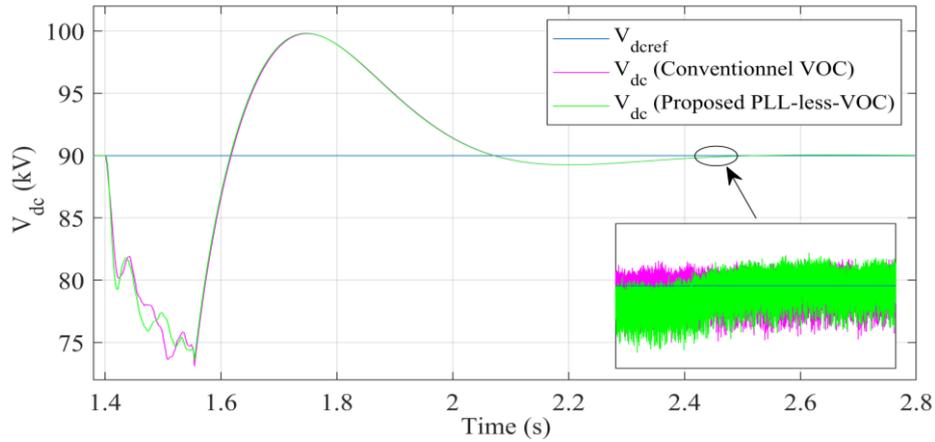
Figure 10. Responses of DC-link voltage under the third test.

The DC-link voltage behavior is identical trend for both controllers, which may be observed from Figure 10. It can be noted that the DC-link voltage reduces to 74 kV when the fault occurs, then settled to the reference value within 1 sec once the fault is cleared while it has nearly the same oscillatory response for both controllers as shown in the zoomed portion.
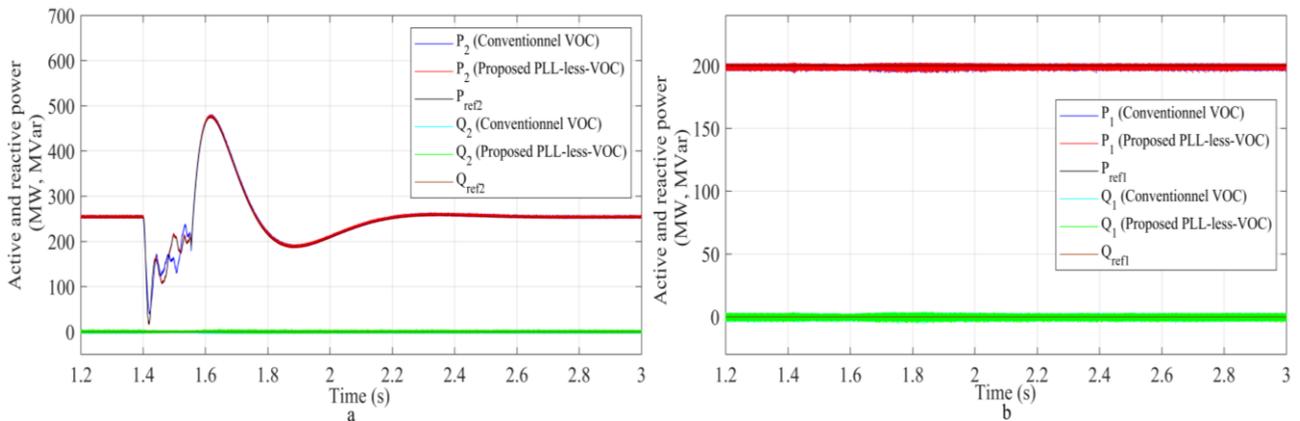
Figure 11. Responses of active and reactive power transmitted in both grids under the third test: a- P1 and Q1 of grid 1, b- P2 and Q2 of grid 2.

The behavior of active and reactive powers of the two controllers follows the same trend, as shown in Figure 11. We observe that, the real powers of grid 1 (P_1) quickly converge close to zero when the fault occurs, and return to their initial values after a transient of 230 MW with a time delay of 0.9 sec, when the fault is cleared, for both controllers. On the other hand, the reactive power of grid 1 (Q_1), and the active and reactive power of grid 2 (P_2, Q_2) are not affected for both control strategies.

These results are in a similar performance in the DC-link voltage, active and reactive power output from VSC for both controllers. This is a consequence of PLL's ability to ensure accurate synchronization between both the grid and the VSC during the fault due to the use of nominal conditions of PLL parameters (ω_n and ζ).

Figure 12 shows the responses of grid voltage and current during a three-phase fault of 150 msec imposed on grid 1 at t = 1.4 sec. The current on grid 1 quickly converges to zero. There is a fast-reducing oscillation of the current and not a direct exponential convergence. In the same framework, when the fault is cleared, the current stabilizes to its original value after a small transient of 0.75 sec for both controllers as shown in Figure 12 (c and g). The current on grid 2 is affected by the fault occurrence and stabilizes after the fault clearance for both controllers as shown in Figure 12 (a and e).

The AC voltages of grid 1 and grid 2 are not affected with the fault occurrence for both controllers as shown in Figure 12 (b, d, f, and h).
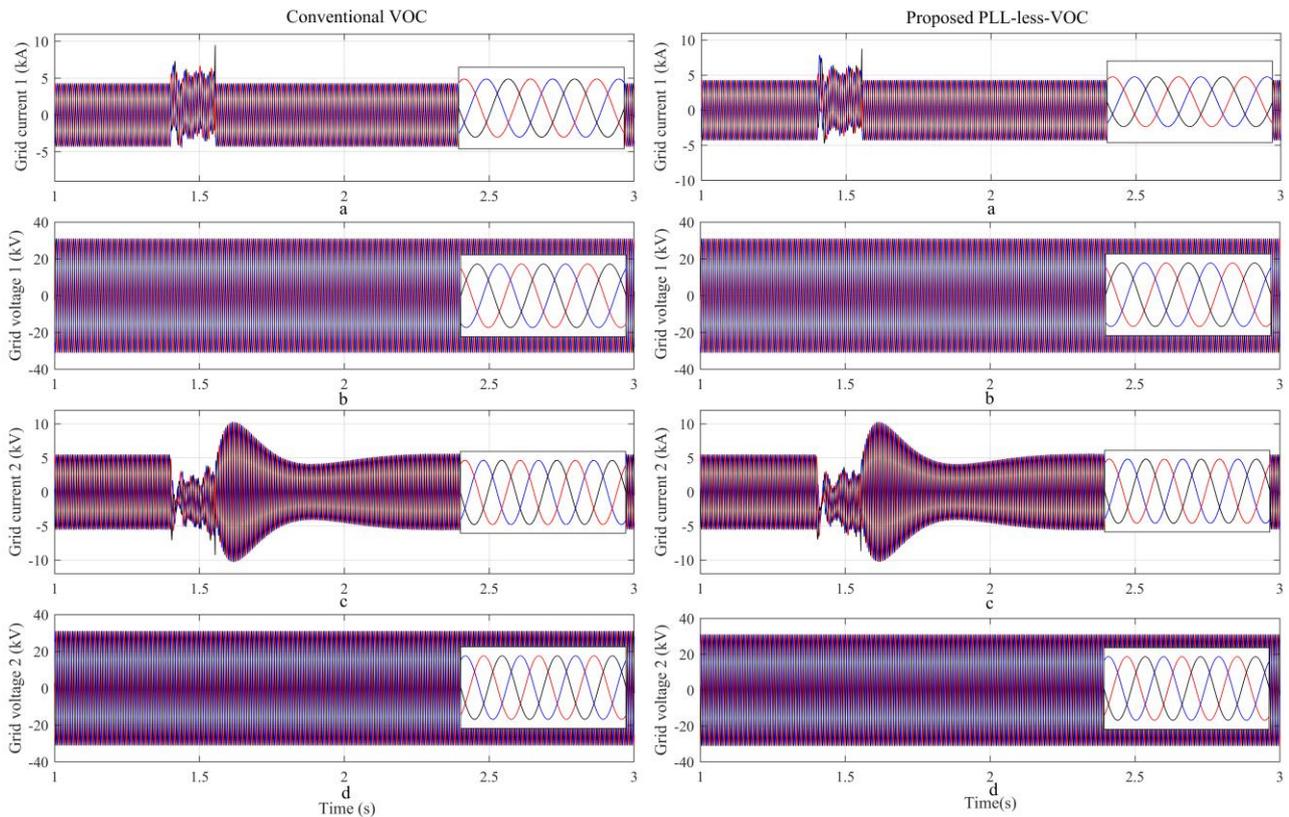
Figure 12. Responses of grids voltages and currents using both control strategies under the third test.

5   Conclusion

VSC-HVDC transmission technology is growing in applicability as it becomes more common in renewable power energy applications. This article investigated the conventional VOC strategy using a PLL with a new proposed PLL-less-VOC strategy that does not employ a PLL for study and analysis of VSC HVDC system stability. An analogy between the traditional VOC strategy and the new proposed PLL-less-VOC strategy for the VSC-HVDC system is shown first. Then, we demonstrated mathematically that PLL-less-controller is the same as the conventional VOC in the synchronous rotating reference frame. This indicates that by removing the PLL from the new control method, we can have the same steady state performance as a traditional VOC but improved tracking performance since the proposed control method does not require either Park transformations or PLL systems. It significantly reduces the computational burden. The experimental tests of the system using the STM32F407G microcontroller demonstrate that the proposed PLL-less-VOC strategy is capable of synchronizing and stabilizing both converters of HVDC system. The suggested PLL-less-VOC strategy has the same property as the conventional VOC strategy under standard conditions, but it has better dynamic and transient stability in certain exceptional conditions in which the PLL system creates problems. Hence, it can easily be implemented in cost-effective microcontrollers.

References

[1]   A. Kalair, N. Abas and N. Khan, " Comparative study of HVAC and HVDC transmission systems," *Renewable and Sustainable Energy Reviews*, vol. 59, pp. 1653-1675, 2016, doi: https://doi.org/10.1016/j.rser.2015.12.288.

[2]   A. Kaushal, and D. Van Hertem, " An overview of ancillary services and HVDC systems in European context," *Energies*, vol. 12, no 18, p. 3481, 2019, doi: https://doi.org/10.3390/en12183481.

[3]   A. Nadheer, and Yasar N. Lafta. " PSS/E based placement wind/PV hybrid system to improve stability of Iraqi grid," *International Journal of Electrical and Computer Engineering*, vol. 10, no 1, p. 91, 2020, doi: https://doi.org/10.11591/ijece.v10i1.pp91-104

[4]   Y. Wang, C. Zhao, and C. Guo, " Comparison study of small-signal stability of MMC-HVDC system

_____

in different control modes," *International Journal of Electrical Power & Energy Systems,* vol. 111, p. 425-435, 2019, doi: https://doi.org/10.1016/j.ijepes.2019.04.017.

[5]   Y. Gui, X. Wang, and F. Blaabjerg, " Vector current control derived from direct power control for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 34, no 9, p. 9224-9235, 2018, doi: https://doi.org/10.1109/TPEL.2018.2883507.

[6]   F. Hassan, A. Kumar and A. Pati, " Recent advances in phase locked loops for grid connected systems: A Review," *2022 IEEE Delhi Section Conference (DELCON),* pp. 1-6, 2022, doi: 10.1109/DELCON54057.2022.9752810.

[7]   J. Z. Zhou, H. Ding, S. Fan, Y. Zhang, and A. M. Gole, " Impact of short-circuit ratio and phase-locked-loop parameters on the small-signal behavior of a VSC-HVDC converter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2287-2296, Oct. 2014, doi: 10.1109/TPWRD.2014.2330518.

[8]   W. Wang, G. Li, and J. Guo, " Large-scale renewable energy transmission by HVDC: Challenges and proposals," *Engineering*, 2022, doi: 10.1016/j.eng.2022.04.017.

[9]   M. Farrokhabadi et al., " Microgrid stability definitions, analysis and examples," *IEEE Transactions on Power Systems*, vol. 35, no. 1, pp. 13-29, Jan. 2020, doi: 10.1109/TPWRS.2019.2925703.

[10]   J. Zhao, M. Huang, H. Yan, C. K. Tse and X. Zha, " Nonlinear and transient stability analysis of phase-locked loops in grid-connected converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 1018-1029, Jan. 2021, doi: 10.1109/TPEL.2020.3000516.

[11]   M. G. Taul, X. Wang, P. Davari and F. Blaabjerg, " An Overview of Assessment Methods for Synchronization Stability of Grid-Connected Converters Under Severe Symmetrical Grid Faults," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9655-9670, Oct. 2019, doi: 10.1109/TPEL.2019.2892142.

[12]   J. Khazaei, P. Idowu, A. Asrari, A. B. Shafaye, and L. Piyasinghe, " Review of HVDC control in weak AC grids," *Electric power systems research*, vol. 162, p. 194-206, 2018, doi: https://doi.org/10.1016/j.epsr.2018.05.022.

[13]   B. Yuan, J. Xu, C. Zhao, and Y. Yuan, " An improved phase-locked-loop control with alternative damping factors for VSC connected to weak AC system," *Journal of Control Science and Engineering*, 2016, vol. 2016, doi: https://doi.org/10.1155/2016/9537342.

[14]   M. Davari and Y. A. -R. I. Mohamed, " Robust Vector Control of a Very Weak-Grid-Connected Voltage-Source Converter Considering the Phase-Locked Loop Dynamics," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 977-994, Feb. 2017, doi: 10.1109/TPEL.2016.2546341.

[15]   Y. Li and Z. Du, " Stabilizing Condition of Grid-Connected VSC as Affected by Phase Locked Loop (PLL), " in *IEEE Transactions on Power Delivery*, vol. 37, no. 2, pp. 1336-1339, April 2022, doi: 10.1109/TPWRD.2021.3115976

[16]   R. Shah, J. C. Sanchez, R. Preece, and M. Barnes, " Stability and control of mixed AC–DC systems with VSC-HVDC: a review," *IET Generation, Transmission & Distribution*, vol. 12, no 10, p. 2207-2219, 2018, doi: https://doi.org/10.1049/iet-gtd.2017.1140.

[17]   H. Wu and X. Wang, " Transient Stability Impact of the Phase-Locked Loop on Grid-Connected Voltage Source Converters," *International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pp. 2673-2680, 2018, doi: 10.23919/IPEC.2018.8507447.

[18]   P. Zhou, X. Yuan, J. Hu, and Y. Huang, " Stability of DC-link voltage as affected by phase locked loop in VSC when attached to weak grid," *2014 IEEE PES General Meeting| Conference & Exposition*, vol. 593, pp. 1-5, July. 2014, doi: https://doi.org/10.1109/PESGM.2014.6939460.

[19]   S. Jeong and G. Jang, " Stability Analysis of a Weak-Grid-Connected Voltage-Sourced Rectifier Considering the Phase-Locked Loop Dynamics," *IEEE Transactions on Power Systems*, vol. 38, no. 1, pp. 436-446, Jan. 2023, doi: 10.1109/TPWRS.2022.3169176.

[20]   S. Dedeoglu and G. C. Konstantopoulos, " PLL-Less Three-Phase Droop-Controlled Inverter with Inherent Current-Limiting Property," *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, pp. 4013-4018, 2019, doi: 10.1109/IECON.2019.8927219.

[21]   B. Hu, H. Nian, M. Li, Y. Liao, J. Yang, and H. Tong, "Impedance Characteristic Analysis and Stability Improvement Method for DFIG System Within PLL Bandwidth Based on Different Reference Frames," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 1, pp. 532-543, Jan. 2023, doi: 10.1109/TIE.2022.3150092.

[22]   M. S. Eslahi, S. Vaez-Zade, & A. Jabbarnejad, " A comparative study of control methods for grid side

converters in PMSG-based wind energy conversion systems," *In 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*, pp. 979-984, 2020, June, doi: https://doi.org/10.1109/ISIE45063.2020.9152427.

[23]   A. Chebabhi, S. Barkat, A. Kessal, "Combined voltage oriented control and direct power control based on backstepping control for four-leg PWM rectifier under unbalanced conditions," *Engineering Review*, 42 (3), 0-0, 2022, doi: https://doi.org/10.30765/er.2020.

[24]   J. Zhao, M. Huang, and X. Zha, " Nonlinear Analysis of PLL Damping Characteristics in Weak-Grid-Tied Inverters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 11, pp. 2752-2756, Nov. 2020, doi: 10.1109/TCSII.2020.2978026.

[25]   J. F. Morris, K. H. Ahmed, and A. Egea-Àlvarez, " Analysis of Controller Bandwidth Interactions for Vector-Controlled VSC Connected to Very Weak AC Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 7343-7354, Dec. 2021, doi: 10.1109/JESTPE.2020.3031203.

[26]   A. Cataliotti et al., " Experimental evaluation of an hybrid communication system architecture for Smart Grid applications," *IEEE International Workshop on Applied Measurements for Power Systems (AMPS)*, pp. 96-101, 2015, doi: 10.1109/AMPS.2015.7312745.

[27]   F. Shahriyar, M. Islam, A. Chakraborty, M. Hasan, H. U. Zaman, and A. H. Siddique, " Fault and System Analysis Model of Voltage Source Control Based HVDC Transmission System," *12th International Conference on Computing Communication and Networking Technologies (ICCCNT), 2021*, pp. 1-6, 2021, doi: 10.1109/ICCCNT51525.2021.9579990.

[28]   Zhu, S., & Hu, B., "Key technologies of active power filter for aircraft: a review," *Engineering Review*, vol. 36 no. 3, pp. 221-237, 2016, er.riteh.hr//index.php/ER/article/view/686.

[29]   Faddel, S., Saad, A. A., El Hariri, M., & Mohammed, O. A., "Coordination of hybrid energy storage for ship power systems with pulsed loads," *IEEE Trans*. Ind. Appl, vol. 56, no. 2, pp. 1136-1145, 2019, doi:10.1109/TIA.2019.2958293.

[30]   C. Li, Y. Cao, Y. Yang, L. Wang, F. Blaabjerg, and T. Dragicevic, " Impedance-based method for DC stability of VSC-HVDC system with VSG control," *International Journal of Electrical Power & Energy Systems*, vol. 130, p. 106975, 2021, doi: https://doi.org/10.1016/j.ijepes.2021.106975.

[31]   J. Lamterkati, L. Ouboubker, M. Khafallah, and A. El Afia, " Implementation on the dSPACE 1104 of VOC-SVM based anti-windup PI Controller of a three-phase PWM rectifier," *International Journal of Power Electronics and Drive Systems*, vol. 12, no 3, p. 1586, 2021, doi: https://doi.org/10.11591/ijpeds.v12.i3.pp1586-1597.

[32]   C. Diaz-Sanahuja, I. Peñarrocha-Alós, and R. Vidal-Albalate, " Multivariable phase-locked loop free strategy for power control of grid-connected voltage source converters," *Electric Power Systems Research*, vol. 210, p. 108084, 2022, doi: https://doi.org/10.1016/j.epsr.2022.108084.

[33]   J. Geis-Schroer, A. R. Nair, S. Patel, and S. Kamalasadan, " Modeling and Analysis of Weak Grid Considering Phase Locked Loop and Synchronous Condenser Effect on Grid Stability," *IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, pp. 1–6, 2020, doi: 10.1109/PESGRE45664.2020.9070728.

[34]   Y. Gui, X. Wang, F. Blaabjerg, and D. Pan, " Control of Grid-Connected Voltage-Source Converters: The Relationship Between Direct-Power Control and Vector-Current Control," *IEEE Industrial Electronics Magazine*, vol. 13, no. 2, pp. 31-40, June 2019, doi: 10.1109/MIE.2019.2898012.