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Simulation of an integrated spiral inductor and inter-digital capacitor in a buck micro converter

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ABSTRACT

In this paper, a novel radiofrequency circuit is designed and developed for an integrated on-chip spiral inductor and inter-digital capacitor of the substrate. Results of extensive simulations concerning the influence of both spiral inductor and inter-digital capacitor geometrical parameters on quality factor value are presented. Two scenarios are considered in the simulation; the first operation of buck converter including an ideal capacitor and inductor and then its operation including an inter-digital capacitor and integrated spiral inductor. For both scenarios, we observed that their respective output voltages as well as their respective output currents present the same time responses.

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KEYWORDS
Buck converter; spiral inductor; inter-digital capacitor; integrated; substrate

Nomenclature

N	turns number of spiral inductor
S	spacing between turns of spiral inductor
W	conductor width of spiral inductor
t	conductor thickness of spiral inductor
d_{in}	inner diameter of spiral inductor
d_{out}	outer diameter of spiral inductor
l	average length of spiral inductor
L_s	series inductance of integrated inductor
R_s	series resistance of integrated inductor
C_s	series capacitance of integrated inductor
C_{ox}	oxide capacitance of integrated inductor
C_{sub}	substrate capacitance of integrated inductor
R_{sub}	substrate resistance of integrated inductor
ρ_{sub}	resistivity of the substrate
t_{sub}	thickness of the substrate
ε_o	free space dielectric constant
t_{ox}	oxide thickness
d_{avg}	average diameter of spiral inductor
A	fill factor of spiral inductor
δ	skin depth
ρ	resistivity
Q_L	quality factor of integrated inductor
Q_C	quality factor of integrated capacitor
n	fingers number of inter-digital capacitor
l	finger length of inter-digital capacitor
w	finger width of inter-digital capacitor
s	finger gap of inter-digital capacitor
s_e	end gap of inter-digital capacitor
C	series capacitance of integrated capacitor
R	series resistance of integrated capacitor
C_1, C_2	Parasitic capacitances of integrated capacitor
ε_{eff}	effective dielectric constant

1. Introduction

Because of the increased demand for undersize portable and multifunctional electronic devices, it is natural to say that these requirements are key incentives for researchers in the improvement of miniaturized DC–DC converters in recent years [1–3]. Hence, the research trend objective is to develop small size converters, which operate with high efficiency when shifting voltage levels in electronic devices. These converters can be used in a wide range of small size and/or portable electronic devices. These include, not limited to, smartphones, tablet PCs, micro-electromechanical system (MEMS) sensors, data storage devices and cameras. Thus, if the converter is miniaturized the overall size of the aforementioned devices will further reduce [4].

It is worth emphasizing that it has been reported that the main factors influencing the overall size, cost and performance of portable devices are the passive components. Owing to that, the research focus is recently on the task of passive functions as a drive to further miniaturize and integrate portable electronic devices [5,6].

It is desirable to integrate passive devices within the silicon substrate to reduce parasite due to interconnection, reduce the units' size and cost, and increase radio frequency circuits' operating frequencies. Furthermore, it has been reported that radiofrequency circuits are

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heavily dependent on inductors and capacitors components [7].

The aim of our work is the modelling of an on-chip spiral inductor and inter-digital capacitor that will be integrated in a DC–DC buck converter, for low powers and high frequencies.

The conception of the inductor and capacitor follows several phases. First, the calculation of different geometric and electric parameters, the planar integrated two components (inductor and capacitor) are completely different from the classical geometric form. Then, the study of the different geometrical parameters effects of spiral inductor and inter-digital capacitor is carried out by the MATLAB simulation software.

Finally, the simulation of the integrated two components (inductor and capacitor) in buck converter to validate the studies, we used the PSIM software.

The second objective is to reduce the component size at a low manufacturing cost.

2. Design and modelling of the spiral inductor

Inductors can be designed in various geometric parameters as shown in Figure 1: (d_{in}) as the inner diameter, (d_{out}) is outer diameter, (S) expresses the spacing between turns, (W) is the conductor width and (N) is the turn's number.

The accepted expression for the low-frequency inductance of planar spiral inductors is the modified Wheeler formula [8]:

$$L_s = \frac{K_1 \cdot \mu_0 \cdot N^2 \cdot d_{avg}}{1 + K_2 \cdot A} \tag{1}$$

where (d_{avg}) is the average diameter, (A) is the fill factor, and (K_1) = 2.34 and (K_2) = 2.75 are the inductor square-shaped coefficients.

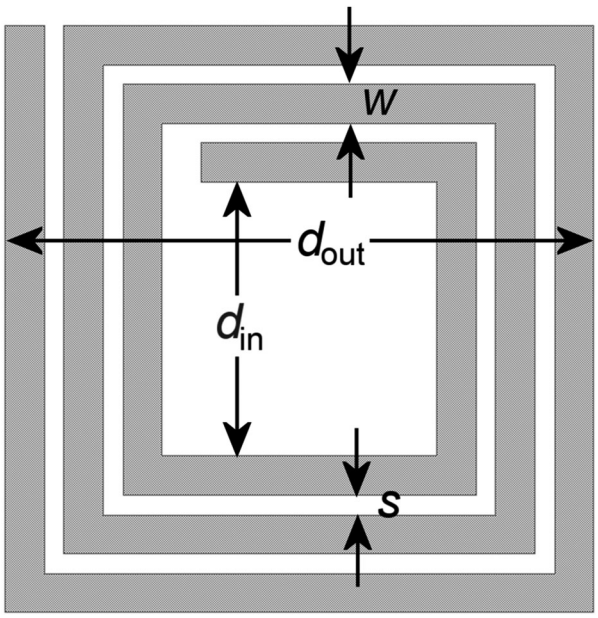

Figure 1. Square spiral inductor [8].

Table 1. Square spiral inductor design parameters.

Geometric parameters	Symbol	Value
Turns number	N	3
Spacing between turns	S	40 µm
Conductor width	W	30 µm
Conductor thickness	t	23 µm
Inner diameter	d_{in}	100 µm
Outer diameter	d_{out}	440 µm
Average length	l_T	2.36 mm

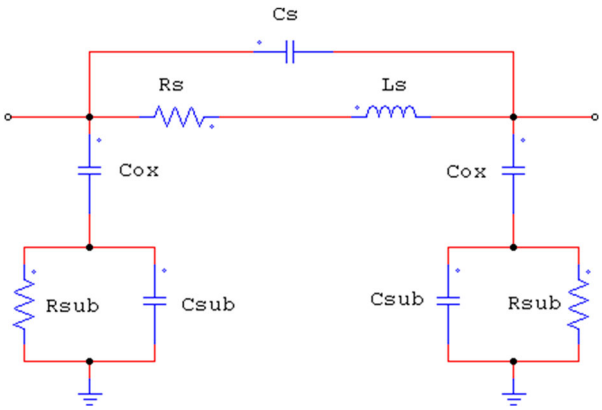

Figure 2. Integrated inductor equivalent electrical circuit [9].

$$d_{avg} = \frac{(d_{out} + d_{in})}{2} \tag{2}$$

$$A = \frac{(d_{out} - d_{in})}{(d_{out} + d_{in})} \tag{3}$$

The values of square spiral inductor design parameters are indicated in Table 1.

The equivalent electrical model of the integrated spiral inductor is depicted in Figure 2.

The series resistance (R_S) is computed conventionally as [10]:

$$R_S = \frac{l_T \cdot \rho}{W \cdot \delta(1 - e^{-(t/\delta)})} \tag{4}$$

where the skin depth, δ, is expressed as [11]:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f}} \tag{5}$$

The series capacitance (C_S) is calculated as the capacitance of the cross-overlapping between the underpass and the spiral. It can be expressed as [12]:

$$C_S = \frac{N \cdot W^2 \cdot \varepsilon_o}{t_{ox}} \tag{6}$$

where (ε_o) is the free space dielectric constant and (t_{ox}) is the oxide thickness.

The total oxide capacitance (C_{ox}) between the spiral and silicon can be calculated by using an expression

Table 2. Integrated inductor electrical parameters.

Electricals parameters	Symbol	Values
Series inductance	L_s	1.2 µH
Series resistance	R_s	0.083 Ω
Series capacitance	C_s	0.682 pF
Oxide capacitance	C_{ox}	8.951 pF
Substrate capacitance	C_{sub}	6.265 pF
Substrate resistance	R_{sub}	0.0028 Ω

from [13]:

$$C_{ox} = \frac{l_T \cdot W \cdot \varepsilon_o}{2 \cdot t_{ox}} \tag{7}$$

The substrate capacitance (C_{sub}) is given by the following expression:

$$C_{sub} = \frac{l_T \cdot W \cdot \varepsilon_o}{2 \cdot t_{sub}} \tag{8}$$

The substrate resistance (R_{sub}) can be estimated as:

$$R_{sub} = \frac{2 \cdot \rho_{sub} \cdot t_{sub}}{l_T \cdot W} \tag{9}$$

where (ρ_{sub}) is the resistivity of the substrate and (t_{sub}) is the thickness of the substrate.

The integrated spiral inductor efficiency is computed as follows [14]:

$$Q_L = 2\pi \frac{\text{stocked energies}}{\text{s dissipated energies}} \tag{10}$$

The mathematical equations used to calculate the electrical parameters of an integrated spiral inductor are presented in detail as follows (1)–(9). The essential electrical parameters are collated in Table 2.

3. Design and modelling inter-digital capacitor

Figure 3 shows the geometrical structure of an inter-digital capacitor. As shown in Figure 3, the geometry design parameters are fingers number ($n = 6$), finger length ($l = 310\,\mu m$), finger width ($w = 45\,\mu m$), finger gap ($s = 30\,\mu m$) and end gap ($s_e = 15\,\mu m$).

The equivalent circuit model of the integrated inter-digital capacitor is shown in Figure 4. In this model, the series capacitance (C) accounts for the capacitance between the fingers, whereas the series resistance (R) resulting from a finite conductivity of metallic components of the element. The capacitors (C_1) and (C_2) connected to the ground are the parasitic capacitances.

The following expressions characterizing the element equivalent circuit model [16]:

$$C_1 = C_2 = \frac{0.5 \cdot l \cdot \sqrt{\varepsilon_{eff}}}{150 \cdot 10^8} \tag{11}$$

$$C = \frac{\varepsilon_{eff} \cdot 10^{-3} \cdot K(k)}{18 \cdot \pi \cdot K'(k)}(n-1) \cdot l \tag{12}$$

where (ε_{eff}) is the effective dielectric constant.

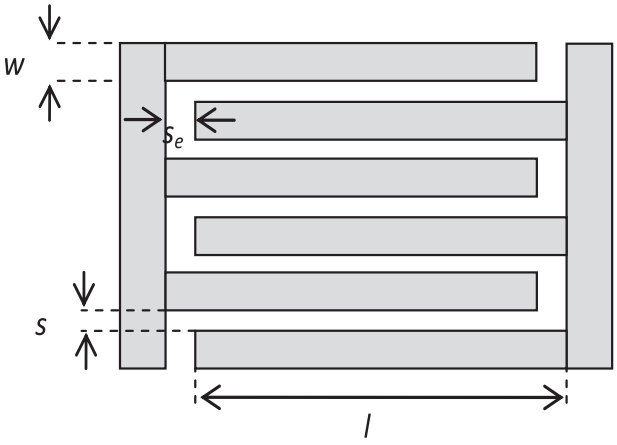

Figure 3. Geometrical structure of an inter-digital capacitor [15].

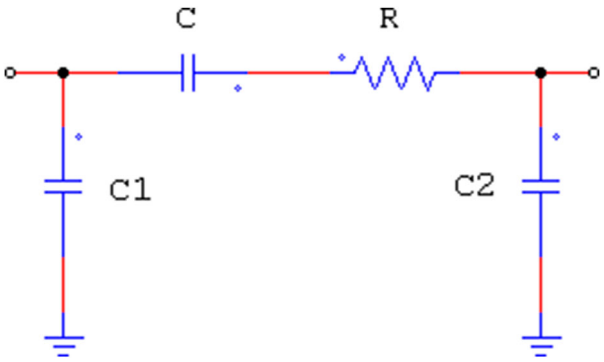

Figure 4. Equivalent circuit model of the inter-digital capacitor.

The ratio of the complete elliptic integral of first kind $K(k)$ to its complement $K'(k)$ is expressed as [17]:

$$\frac{K(k)}{K'(k)} = \begin{cases} \frac{1}{\pi}\ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right) & \text{for} \quad 0.707 \le k \le 1 \\ \frac{\pi}{\ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]} & \text{for} \quad 0 \le k \le 0.707 \end{cases} \tag{13}$$

$$k = \tan\left(\frac{w \cdot \pi}{4(w+s)}\right)^2 \tag{14}$$

$$k' = \sqrt{1-k^2} \tag{15}$$

The series resistance (R) represents metallization losses and it can be calculated by the following formula [18]:

$$R = \frac{4 \cdot l \cdot \sqrt{\rho \cdot \pi \cdot \mu_0 \cdot f}}{3 \cdot w \cdot n} \tag{16}$$

Hence, making use of the above equations, the quality factor due to dielectric loss tangent is computed as follows [19]:

$$Q_c = \frac{1}{2 \cdot \pi \cdot f \cdot C \cdot R} \tag{17}$$

The calculated electrical parameters of the equivalent electrical circuit of the integrated inter-digital capacitor are shown in Table 3.

Table 3. Technological parameters of the integrated capacitor.

Electricals parameters	Symbol	Values
Series capacitance	C	0.207 pF
Parasitic capacitances	C_1,C_2	5.8 pF
Series resistance	R	$0.884 \cdot 10^{-3}$

4. Integrated inductor and capacitor using CMOS techniques

Recently, some research groups have been working on chip implementation using integrated processes such as CMOS techniques [19].

The CMOS technique is attractive for use in passive microwave circuits for various reasons, such as reduced parasitic effects, smaller chip area, lower power consumption, lower system complexity and lower integration cost.

In this paper, we demonstrate the integration of on-chip inductors and inter-digital capacitor of micro converter fabricated in a CMOS technology.

The micro converter is implemented using an inter-digital capacitor integrated into the middle of spiral inductors. In order to achieve a compact size, the capacitor is embedded inside the inductor. Also, the coil of the inductor is intertwined to enhance mutual inductance. Figure 5 shows the layout of the presented design.

The design and fabrication using a silicon substrate at 200 μm in depth following the standard CMOS fabrication process. The chip size is 900 μm × 700 μm.

5. Results and discussions

In this section, we discuss the MATLAB-based simulation results obtained from the spiral inductor and inter-digital capacitor for different geometrical parameters.

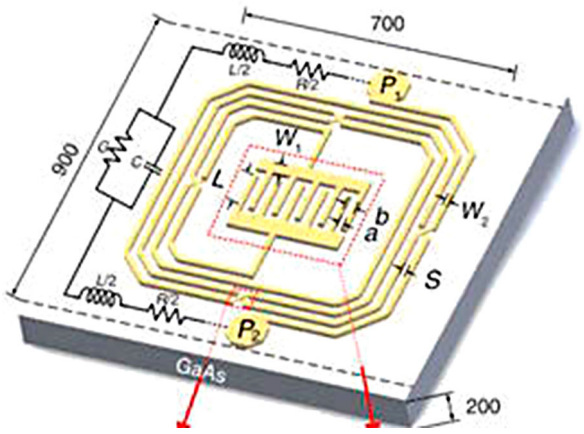

Figure 5. Layout of the integrated spiral inductor and inter-digital capacitor together.

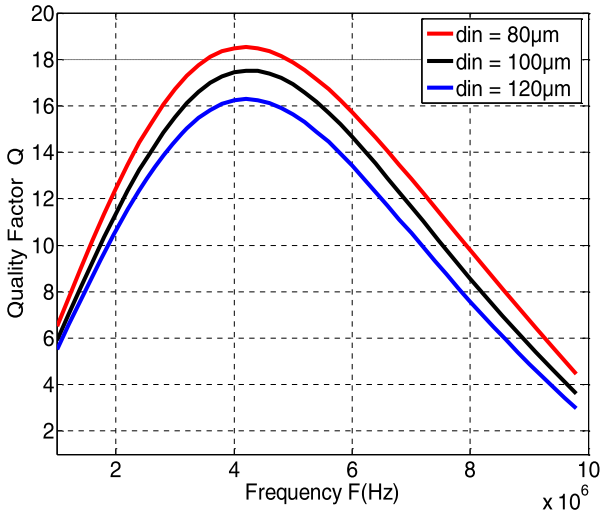

Figure 6. Influence on quality factor for different inner diameters.

5.1. Influence of the inner diameter on the quality factor versus frequency

Figure 6 shows three plots of quality factor versus frequency for three different inner diameters (80, 100 and 120 μm) with a spiral inductor area that is kept unchanged. As shown in Figure 6, an increase of the inner diameter from 80 μm to 120 μm results in a decrease of quality factor. This is due to the decreasing separation between the turns.

5.2. Influence of the number of turns on the quality factor versus frequency

Figure 7 shows the variation of quality factors versus frequency for different spiral inductor turns number ($N = 2, 3$ and 4) and illustrates the influences of diverse the number of turns on the quality factor. As shown in Figure 7, an increase turns number from 2 to 4 results in a decrease of the quality factor and this decrease is more

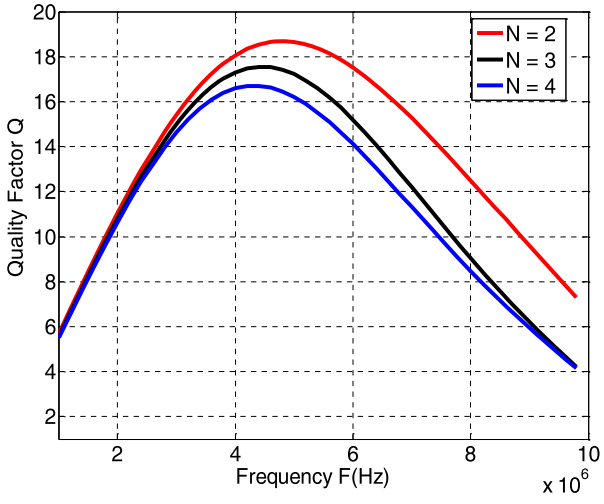

Figure 7. Influence of turns number on the quality factor.

significant at frequencies above 3 MHz. The value of the quality factor decreases because of the added conductor losses.

5.3. Influence of the width of the conductor on the quality factor versus frequency

Figure 8 shows the effects of the conductor width on the quality factor of the spiral inductor. Increasing the width from 20 µm to 40 µm means an increase in the conductor cross-section, which results in a decrease of the series resistance. This is demonstrated in Figure 8, an increase in the conductor width provides higher quality factors.

5.4. Influence of the thickness of the conductor on the quality factor versus frequency

Figure 9 shows the influences of the different thicknesses of conductor on the quality factor of the spiral inductor. A thicker conductor from 15 µm to 25 µm will increase the quality factor.

5.5. Influence of the number of fingers on the quality factor versus frequency

Figure 10 shows, the variation of quality factor as a function of frequency for a different number of fingers. As shown in Figure 10, the quality factor value is inversely proportional to the finger number. For example, as fingers number decreases from 7 to 5, the quality factor increases from 238 to 259.

5.6. Influence of the finger length on the quality factor versus frequency

The effect of finger length on the quality factor of the inter-digital capacitor is shown in Figure 11. The quality factor decreases when the finger length increases from

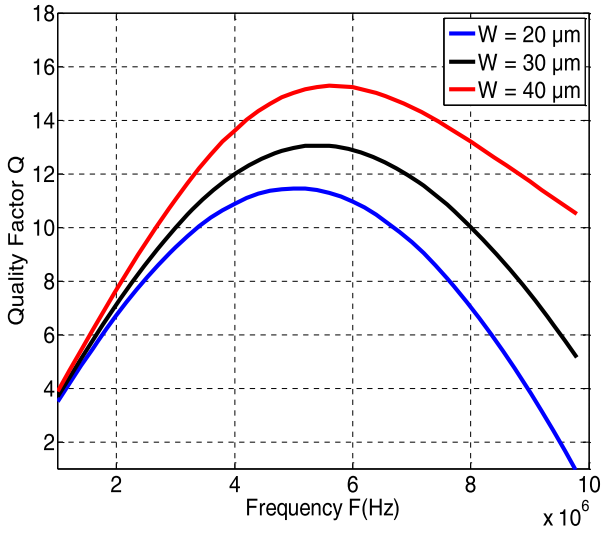

Figure 8. Influence conductor width on the quality factor.

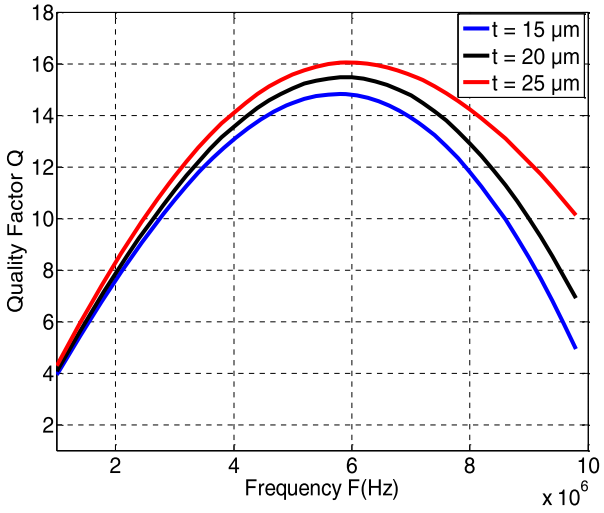

Figure 9. Influence of conductor thickness on the quality factor.

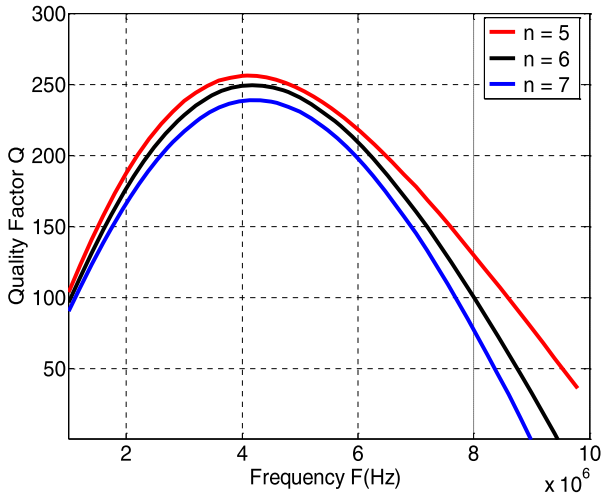

Figure 10. Influence of fingers number on the quality factor.

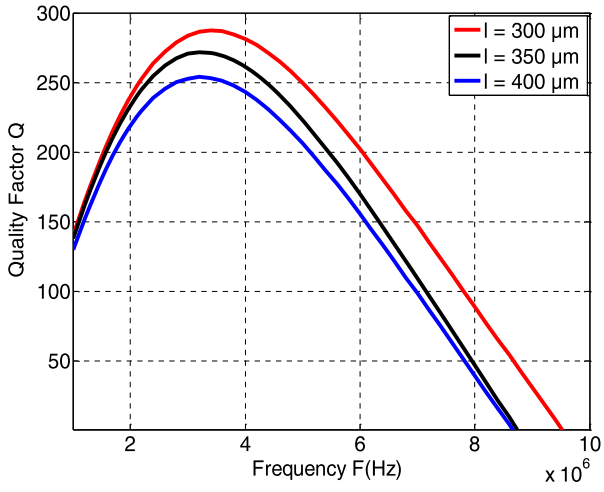

Figure 11. Influence of finger lengths on the quality factor.

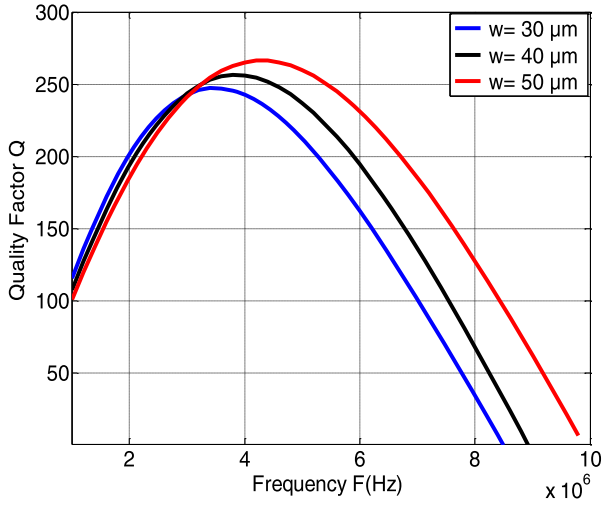

Figure 12. Influence of finger widths on the quality factor.

300 µm to 400 µm. The (Q_{max}) decreases from 256 to 288.

5.7. Influence of the finger width on the quality factor versus frequency

Figure 12 shows the effects of different finger width on the quality factor as a function of frequency. As shown in Figure 12, an increase in finger width from 30 µm to 50 µm reduces the series resistor that eventually leads to a higher quality factor at frequencies higher than 3.5 MHz.

6. Buck converter application

In this study, we have selected a buck converter shown in Figure 13 is a step-down DC–DC converter consisting primarily of inductor, capacitor and two switches (generally a transistor switch and diode) for controlling inductor and capacitor.

The freewheeling diode (D) conducts due to energy stored in the inductor; and the inductor current continues to flow through inductor (L), capacitor (C), load and diode (D). The inductor current falls until transistor (S) is switched on again in the next cycle.

The waveforms for voltage and current are shown in for continuous load current assuming that the current rises or falls linearly as depicted in Figure 14.

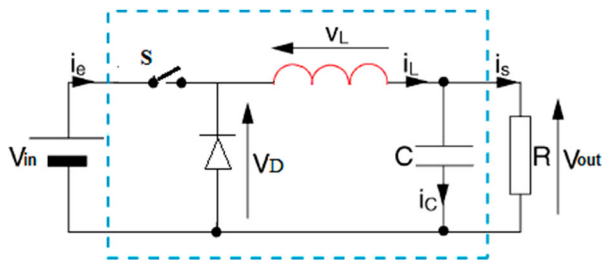

Figure 13. Circuit diagram of the Buck converter.

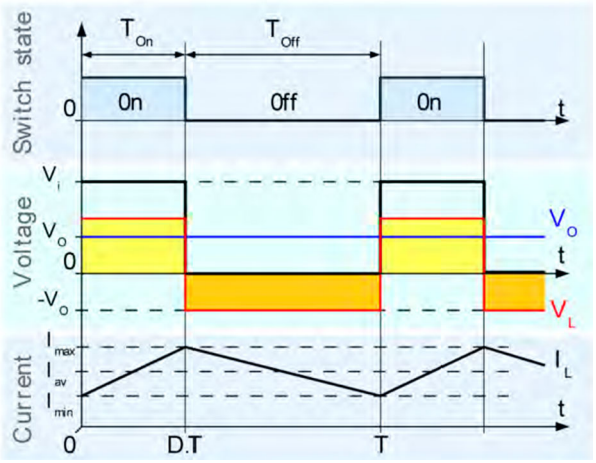

Figure 14. Waveforms of voltage and current of buck converter.

Table 4. Design specifications of buck micro converter.

Parameter	Symbol	Value
Input voltage	V_{in}	2 V
Maximum output voltage	V_{out}	0.87 V
Output ripple voltage	ΔV_{out}	21.7 mV
ripple current	ΔI	17 mA
Load current	I_{out}	0.34 A
Frequency of the converter	f	5 MHz

The design specifications of buck micro converter are indicated in Table 4:

From the data of the converter, we deduce the value of the necessary inductance.

The duty cycle is given by:

$$\alpha = \frac{V_{out}}{V_{in}} = 0.435 \tag{18}$$

$$L = \frac{(V_{in} - V_{out})\alpha}{2 \cdot \Delta I \cdot f} = 2.89\mu\text{H} \tag{19}$$

We deduce the value of the filtering capacity C according to relation:

$$C = \frac{5 \cdot (V_{in} - V_{out})\alpha}{4 \cdot V_{out} \cdot L \cdot f^2} = 9.775\text{nF} \tag{20}$$

The simulation was executed using PSIM software 6.0. The simulation is performed to test the operation of our buck micro converter for two scenarios: operation of buck converter including an ideal capacitor and inductor and then operation including an inter-digital capacitor and integrated spiral inductor

6.1. Converter including ideal inductor and capacitor

Figure 15 depicts the circuit of buck converter containing an ideal inductor and capacitor. Figure 16 shows the time responses of the output voltage, V_{out}, and current, I_{out}, of the buck converter.

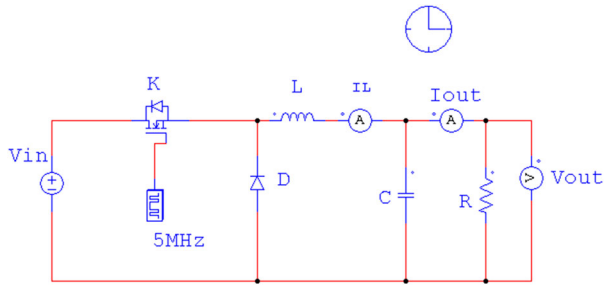

Figure 15. Buck converter with ideal inductor and capacitor.

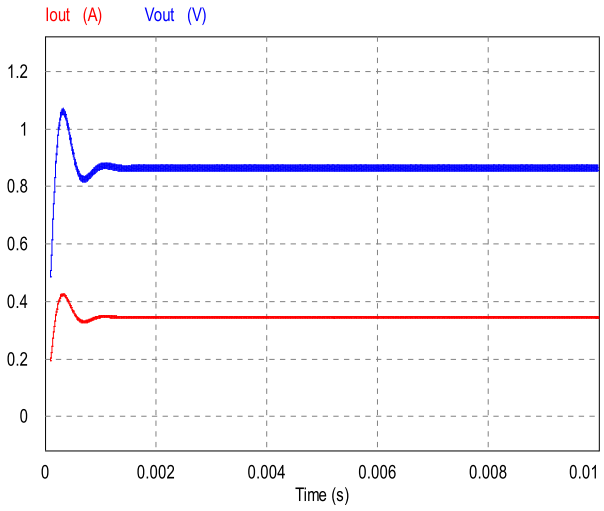

Figure 16. Time responses of output voltage and current of a buck converter with ideal inductor and capacitor.

6.2. Converter including an integrated spiral inductor and inter-digital capacitor

Converter with the integrated spiral inductor and inter-digital capacitor.

Figure 17 illustrates the circuit of a buck converter with the ideal inductor and capacitor retrofitted with an integrated spiral inductor and inter-digital capacitor. The different electrical parameters of the equivalent electrical circuit are indicated in above Tables 2 and 3.

Figure 18 shows the time responses of the output voltage, V_{out}, and current, I_{out}, of the upgraded buck converter.

Figures 16 and 18 show similar time responses of output voltage and current for both set-ups.

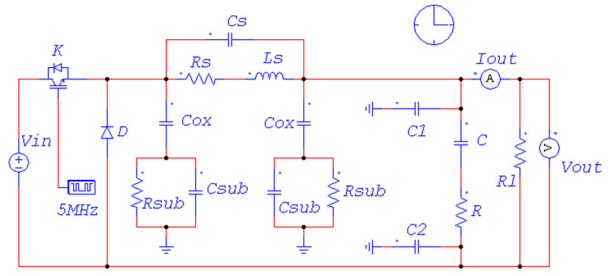

Figure 17. Buck converter with the integrated spiral inductor and inter-digital capacitor.

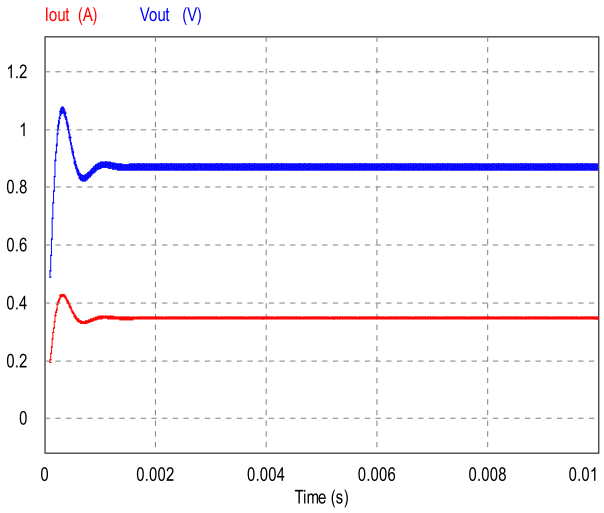

Figure 18. Output voltage and current of a buck.

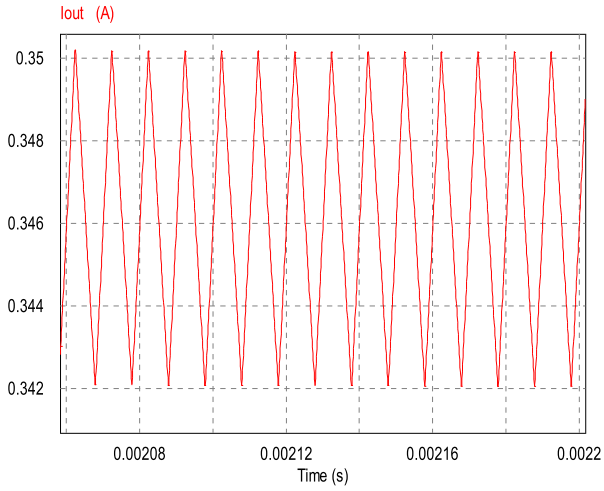

Figure 19. Ripples of a output current.

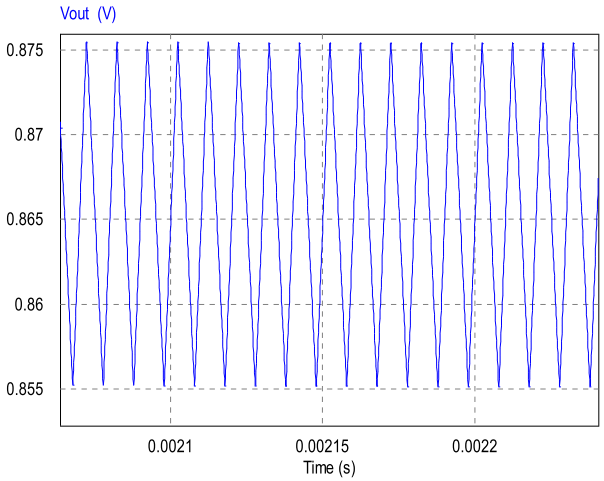

Figure 20. Ripples of a output voltage.

Figure 19 shows the ripples of the output current which varies between 0.34209 and 0.35019 A.

Figure 20 shows the output voltage is continuous with a low ripple varying between 0.85524 and 0.87548 V.

Table 5. Measured values of the output voltage and current of a buck converter with ideal inductor and capacitor.

	Average value
Time from	1.0002000e−004
Time to	1.0000000e−002
I_{out} (A)	3.4959696e−001
V_{out} (V)	8.7399274e−001

Table 6. Measured values of the output voltage and current of a buck converter with the integrated spiral inductor and inter-digital capacitor.

	Average value
Time from	1.0002000e−004
Time to	1.0000000e−002
I_{out} (A)	3.4795753e−001
V_{out} (V)	8.7685332e−001

Table 7. Comparison of the proposed buck converter with existing approaches.

Design	1. [20]	2. [21]	3. [22]	This work
Input voltage [V]	1.2	1.66	1.2	2
Output voltage [V]	0.9	0.83	0.9	0.87
Load current [A]	0.37	0.39	1	0.34
Switching frequency [MHz]	100	150	50	5
Peak efficiency %	77.9	82	88.3	89.3
area [mm^2]	2.25	/	1.47	0.63

The measured values of output and input of voltages and currents of the buck converter are given in the following Tables 5 and 6:

The simulation results are compared with several prior work, as listed in Table 7.

The switching frequency is the lowest due to the integration of the two components together, the spiral inductor and the inter-digital capacitor.

Our design occupies a smaller area than all the previously reported designs, with a comparable output voltage and load current.

These results demonstrate the applicability and advantages of integrating the spiral inductors and inter-digital capacitor for DC–DC switching buck converters.

7. Conclusion

The important issues to be considered for the design of on-chip inductor and inter-digital capacitor, which are integrated in a DC–DC buck converter, have been highlighted in this work.

To extract the technological parameters, we conceive a new electrical model of a spiral inductor and inter-digital capacitor integrated with substrate.

We also present the geometrical parameters and their influence on the value of the inductor and capacitor. This allowed us to simulate the factor quality of our two components (inductor, capacitor) and analysed the influence of different geometrical on this coefficient.

Then, the influence of various geometrical parameters was analysed in detail based on simulations using the software MATLAB.

Moreover, it was also observed that the highest maximum quality factor of spiral inductor and inter-digital capacitor are obtained with the low inner diameter (d_{in}), the number of turns (N), the number of fingers (n) and the finger length (l).

Using the software PSIM6.0, we validate the results of the integrating of the inductor and capacitor.

We compare the waveforms of currents and voltages of a buck converter in two different electrical circuits. The first circuit is a buck converter containing an ideal inductor and capacitor, without any parasitic effects; the second is equivalent circuits for a buck converter with the integration of the two components together, spiral inductor and inter-digital capacitor.

After this comparison, we conclude that the results are very encouraging, because the waveforms of currents and tensions are respected, which enables us to say that the new electrical circuit of the integrated spiral inductor and capacitor that we propose functions perfectly.

Disclosure statement

The authors declare that they have no known competing for financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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