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Fault analysis in the 5-level multilevel NCA DC–AC converter

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ABSTRACT

The existing neutral clamped active inverter has common mode voltage with the high frequency which can reduce the severity with less voltage gain. The traditional active neutral point clamped (APC) DC–AC converter maintains great common mode voltage with high-frequency (CMV-HF) reduction capability so, it has limited voltage gain. The paper presents a new 5-level active neutral point clamped DC–AC converter that can change voltage step-up in a single-stage inversion. In the suggested design, a common ground not only reduces the CMV-HF but also improves DC link voltage use. Compared with the traditional two-stage 5-level APC DC–AC converter, the proposed design has lower voltage stresses and greater uniformity. While improving the overall efficiency, the suggested clamped DC–AC converter saves three power switches and a capacitor. Modelling and actual tests have proven the suggested active neutral point clamped inverter's overall operation, efficacy and achievability. The proposed circuit is finally tested with fault clearance capability.

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KEYWORDS
Five-level inverter; fault compensation; multilevel inverter

I. Introduction

Power electronic circuits are mainly designed to convert energy from one form to another with a specified level of voltage, which can be imported/exported to the power grid [1,2]. In this power conversion scenario, different varieties of power converters are designed/identified by the researchers which are highly suitable for the particular applications. Solar energy power conversion-based applications need a transformerless DC–AC converter, to avoid the bulky size of the circuit, to reduce electromagnetic interferences (EMI) and also to increase gain [3,4].

In DC–AC conversion, circuits' isolation is required between the DC source side and the AC load side to avoid leak current emission and more common mode voltage gain issues [5,6]. High-frequency common mode voltage gain-related issue is attracting the attention over non-isolated transformer topologies. Specific modulation techniques with clamping circuits are presented in the literature survey to control inverter topology. Neutral-clamped active inverters are highly preferred in the market [6]. AC output is connected in the DC link midpoint called neutral, and also capacitor is clamped on it to stop leakage current [7,8]. A drawback of the neutral clamped active (NCA) Inverter bridge is its limited voltage gain, a part of the dc link voltage will appear across the AC terminal. Conventional 5-level converters have two-stage structures with boost conversion operation, as shown in Figure 1, and the drawback is double times the AC voltage is required to attain dc link voltage. Recent researchers attempt to combine the NCA inverter with a switched capacitor to enhance voltage gain [9,10]. To enhance the voltage gain of the circuit-switched capacitor connected with the dc link capacitor in series are discharged at the same time. While charging from the supply the same capacitor is connected parallel with the dc link capacitor for supplying the load. These topologies have disadvantages of current spikes and more components.

Advancement in power electronic circuits has hastened the incorporation of different renewable sources of power into the electric grid. In this regard, there is a rising trend towards the creation of various types of converters that are correctly matched to a wide range of conversions [11,12]. Transformerless DC–AC converters, which avoid the use of large transformers, are among the common styles of converters that have lately gained traction in solar applications [13,14]. The shortage of isolation between both the DC supply and the AC outputs, on the other hand, invariably results in a CMV-HF, which increases the danger of excessive fault current emission [15,16].

In any transformerless topology, the CMV-HF issue is critical. It has primarily been tackled by using specific modulation schemes and DC–AC converter circuits with extra circuits for clamping operation [17,18]. Nevertheless, it is worth noting that the traditional APC DC–AC converter, which is now commercialized, is capable of mitigating HFCMV just by its form. The solar cells' stray capacitor is crimped across the DC link

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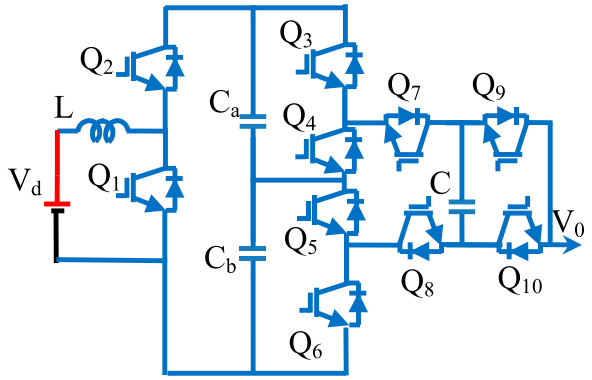

Figure 1. The conventional 5-level converter.

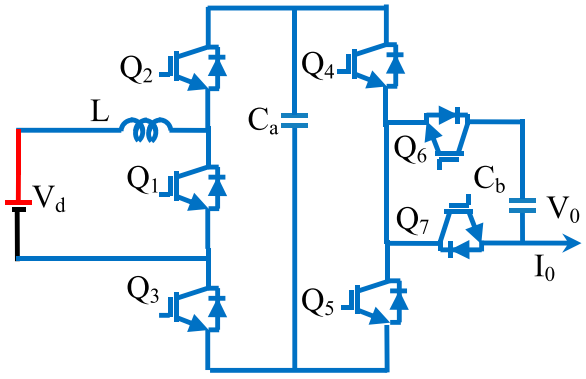

Figure 2. The proposed 5-level converter.

to avoid leakage current, when the ground of its AC load current is linked midway in the capacitor at the DC link [19,20]. The APC DC–AC inverter has a limited gain in voltage because it may create a maximal AC range of voltage that is 50% voltage of the capacitor-DC link. As a result, a dual-stage system with a first-stage power converter, as shown in Figure 1, is often necessary to achieve the voltage at the DC link need of at least twice the AC maximum voltage.

Furthermore, significant efforts have been done to boost the voltage gain by adding switching capacitors into such an APC DC–AC converter structure. The switched capacitors are exhausted in parallel with the DC link to provide a raised voltage range, resulting in increased voltage gain. It ought to be noted, nevertheless, the switched capacitors must be charging in tandem with the DC link before providing the load. These cause current spikes. Furthermore, the intermittent dc source current severely limits their use in solar power systems. The constraints found in the switched capacitor have carried topologies that rendered them less appealing than the other two stages of an APC DC–AC converter.

As shown in the Figure, this paper offers a revolutionary single-stage 5-level DC–AC converter with voltage step-up capacity. It is a replacement to the typical two-stage 5-level APC DC–AC Converter (FL-APC) shown in the figure, with the following advantages.

(1) Decreased the number of switches from 10 to 7;
(2) Decreased the number of capacitors from three to two;
(3) Increased DC link voltage use;
(4) Decreased DC–AC voltage stresses, so more efficient;
(5) The use of ground common to reduce leakage currents;
(6) Step-up voltage capability within single-stage inversion.

A new one-stage level NCA inverter with voltage step-up capability is illustrated in Figure 2, which gives a solution and also overcomes the drawbacks of conventional two-stage topology. The proposed converter has seven switches instead of ten, the capacitor requirement is only two, and it increases dc link voltageuse. Low cost, more efficiency and less voltage stress are also add-on advantages. Common ground decreasing or controlling leakage current and voltage step-up with a single stage are big advantages. This paper is organized with V sections; mathematical analysis with modes of operation is reported in Section II. A comparison between the existing and proposed topology is reported in Section III. Implementation of the proposed system at both the simulation and hardware level is reported in Section IV and finally concluded in Section V.

II. Modes of operation

The proposed 5L-NAC with common ground step-up inverter topology is implemented for voltage step-up 5L ac voltage production from one-stage operation as shown in Figure 2.

The comparison between conventional and proposed topologies shows that the number of components is reduced to enhance the conversion efficiency. To increase the utilization of the dc link voltage and control common voltage with high frequency a common ground is used between ac and dc sides. Because of this arrangement the dc link voltage and ac voltage are equal; this voltage is double the times of a conventional inverter. Modes of operation are explained with eight circuits which are shown in Figure 3. The proposed concept has a control scheme based on pulse width modulation with a level-shifted operation (PWM-LS). PWM-LS consists of two switching parts: a signal generator and a state generator.

Dc link voltage with AC voltage made decoupling control is realized for comparing constant reference with top triangular carrier for producing duty cycle which increases voltage level. The step-up component L is charged by constant (δ) duty cycle that step up voltage

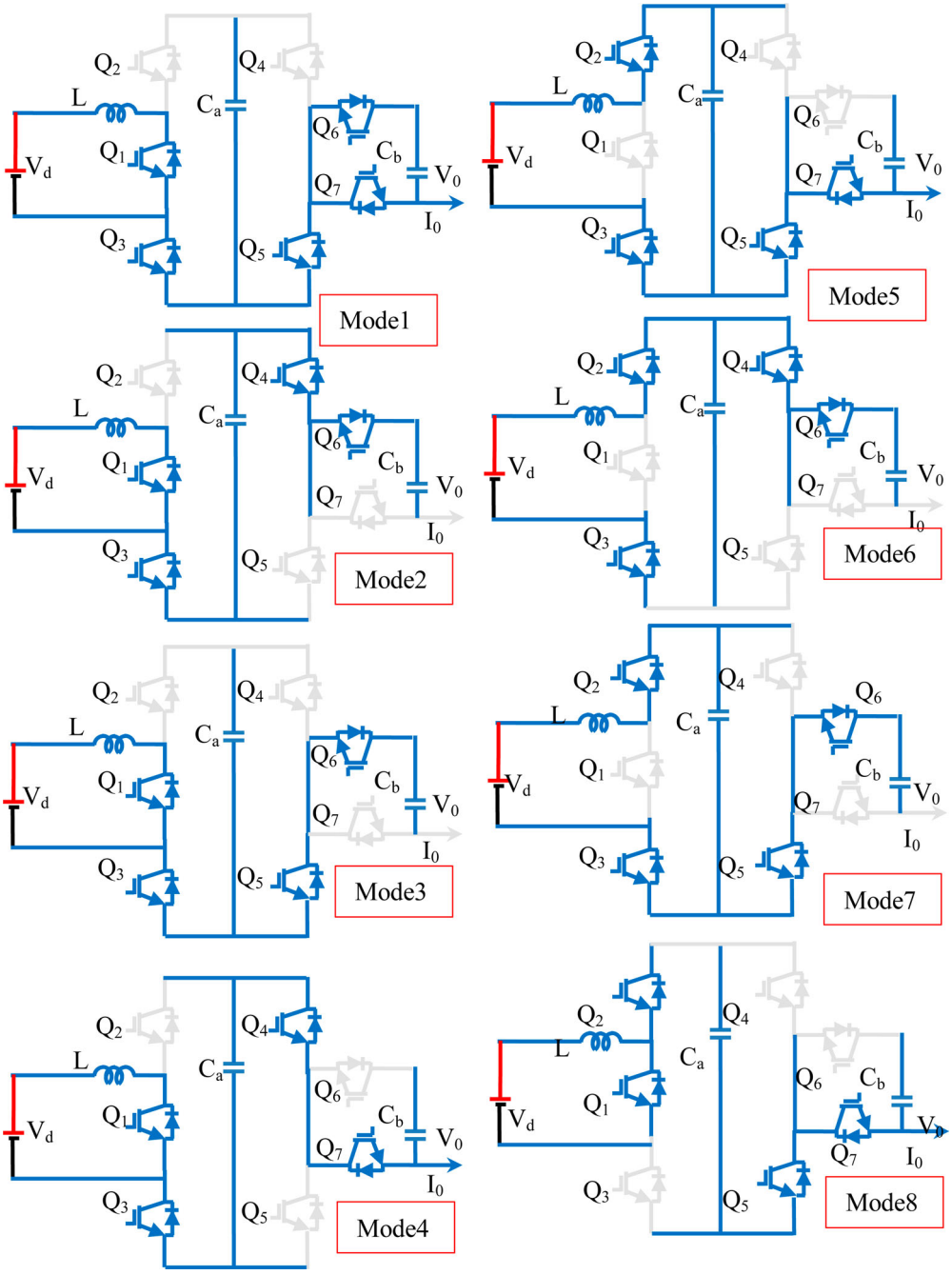

Figure 3. Modes of operation.

across C_a

$$V_D = \frac{V_d}{1-\delta} \tag{1}$$

Capacitor Cb voltage is controlled automatically at 50% of the voltage. 5L voltage is generated between $+V_{\text{dpeak}}$ and $-V_{\text{dpeak}}$. Peak AC voltage is given as

$$V_{0,1} = \frac{V_d}{1-\delta} \tag{2}$$

where the modulation index $= M$, considering duty cycle δ as a minimum, A_v is the voltage gain given as

$$A_V = \frac{V_{0,1}}{V_d} = \frac{M}{(1-M)2} \tag{3}$$

The proposed circuit operation is controlled by the PWM-LS scheme. T_1 and T_{mean} are calculated from the current waveform

$$T_1 = \frac{T_0}{2\pi}\sin^{-1}\frac{M1}{2M} \tag{4}$$

$$T_{\text{mean}} = \frac{1}{2\pi f_0}\sin^{-1}\frac{I^1 C_a}{I_{0,1}} \tag{5}$$

Change in the voltage of the capacitor, electric charge is given by

$$\Delta VC_b = \frac{I_{0,1}}{C_b \pi f_0}\left[1 + \frac{\pi}{2M} - 2\cos\left(\sin^{-1}\frac{1}{2M}\right) - \frac{1}{M}\sin^{-1}\frac{1}{2M}\right] \tag{6}$$

The capacitor voltage ripple of high-frequency component and low-frequency component is derived as

$$\Delta VC_a, f_s = \frac{\Delta I^1 C_a}{C_a, f_s} \tag{7}$$

$$I^1 C_a = \frac{I_{0,1}}{M\pi^2}\left[\pi(3M-1) + 2\left(1 - 2M0\sin^{-1}\frac{1}{2M}\right]\right. \tag{8}$$

Step-up inductor ripple current at the switching frequency induced by pulse width modulation is given as

$$\Delta I_L = \frac{DV_{dc}}{L, f_s} \tag{9}$$

The inductor value is designed from the duty cycle, voltage ripple, current ripple and supply frequency

$$L = \frac{\Delta V_c(1-D)}{\Delta I_L,\ 2\pi f_s} \tag{10}$$

III. Topology comparison

This comparison is useful to evaluate the advantages of the proposed inverter over the conventional inverter. Voltage gain and voltage in the dc link are generalized in Figure 4(i).

While considering AC voltages from the same dc source, the voltage gain produced from both topologies is the same. The proposed converter has the features of more dc link voltage utilization, lower voltage stress and standing voltage is less as shown in Figure 4(ii).

Input 100 V DC is converted to 230 V AC and its simulation waveform is noted in both conventional and proposed circuits. From this comparison the proposed converter required a DC link voltage lesser than conventional topology and also more voltage ripple in the flying capacitor during charging and discharging of capacitor C_b at the fundamental frequency. Total Harmonic Distortion (THD) is slightly higher during self-balancing of C_b due to the impact of filter component output. Triangular carrier frequency is concentrated by the proposed topology to dominate the harmonics similar to the existing topology.

Common mode voltage with high frequency is vanished by both the conventional and proposed as illustrated in Figure 4(iii) (a) and Figure 4(iii) (b), respectively.

Switches consume power and also power losses in the other components are estimated at around 1 kW. Except for cost, the proposed topology fulfils some important parameters such as the number of switches, capacitors, dc-link voltage usage, efficiency and also voltage stress.

The existing common mode voltage is above 300 V, frequency is oscillating in the existing topology,

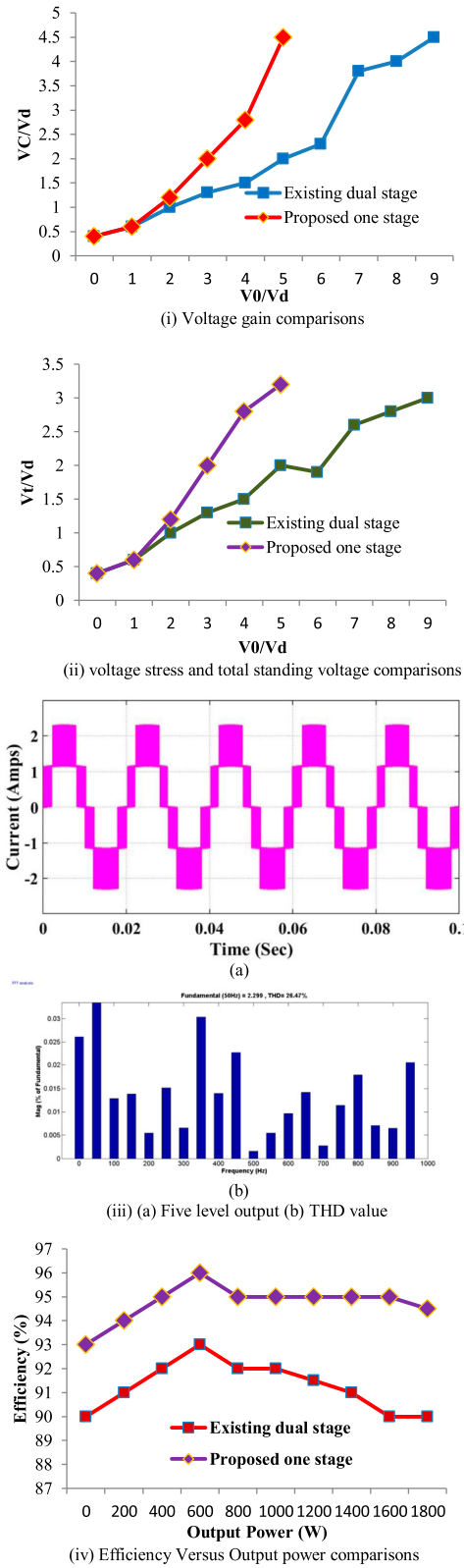

Figure 4. (i) Voltage gain comparisons. (ii) voltage stress and total standing voltage comparisons. 4 (iii) (a) Five-level output (b) THD value. (iv) Efficiency versus output power comparisons.

whereas the proposed topology has fewer ripples, which control common mode voltage. The proposed topology efficiency is also higher due to the minimal number of components in the circuit with one stage, as shown

Table 1. Comparison of components and parameters.

Parameters	5L-ANPC	5L-UGANPC	C-QSBI	E-QSBI	SL-QSBI	TZSI	VVS-DC link (Traditional)	Proposed converter
Switches	7	8	9	7	7	7	8	7
Diodes	2	–	–	8	8	11	8	7
Capacitors	3	3	3	3	3	3	3	2
Inductor	1	1	1	1	1	1	1	1
Switching stress	High	High	Low	High	High	High	Low	Low
Max. switch voltage	110	110	200	200	75	100	200	200

Table 2. Components' specification in the prototype model.

Parameters	Value
Input voltage	100 V
Capacitors	1 nF
Inductor	3.5 mH
Switching frequency	10 kHz
Load resistance	200 Ω
Load inductance	0.3 H
Duty cycle	0.75
Modulation index	0.9
Boosted output voltage	200 V

in Figure 4(iv). Components and their parameters are compared in Table 1.

IV. Power loss calculation

Total losses in the circuit are conduction loss and switching loss (Table 2). Total conduction loss in the circuit is real-time loss of all components combined over the conduction period. So the total power is the product of saturation voltage during ON time Von and current during ON time Ion.

Total conduction loss (P_{con}) is calculated in Equations (11) and (12)

$$P_{con} = P_{con(IGBT)} + P_{con(diode)} \quad (11)$$

$$P_{con} = V_{CE} * I_C + V_D * I_D \quad (12)$$

V_{CE} and V_D are obtained from the curve of IGBT and diode V–I characteristics are given in Equations (13) and (14).

$$V_{CE} = -2 * 10^{-7} * {I_C}^2 + 0.0018 I_C * 0.9661 \quad (13)$$

$$V_D = -1 * 10^{-7} * {I_D}^2 + 0.0012 I_D * 0.7796 \quad (14)$$

Switching losses are calculated from the transition of ON time and OFF time. Total switching loss (P_{sw}) is calculated as given in Equations (15) and (16).

$$P_{sw} = P_{turn(ON)} + P_{turn(OFF)} + P_{rect(diode)} \quad (15)$$

$$P_{sw} = (P_{turn(ON)} + P_{turn(OFF)}) * f_{sw} + P_{rect(diode)} * f_{sw} \quad (16)$$

Curves from approximation are given in Equations (17)–(19)

$$E_{TON} = 8 * 10^{-7} * {I_C}^2 + 0.0023 I_C * 4.016 \quad (17)$$

$$E_{TOFF} = 3 * 10^{-7} * {I_C}^2 + 0.0011 I_C * 3.158 \quad (18)$$

$$E_{Rec.diode} = 7 * 10^{-7} * {I_C}^2 + 0.0039 I_D * 6.654 \quad (19)$$

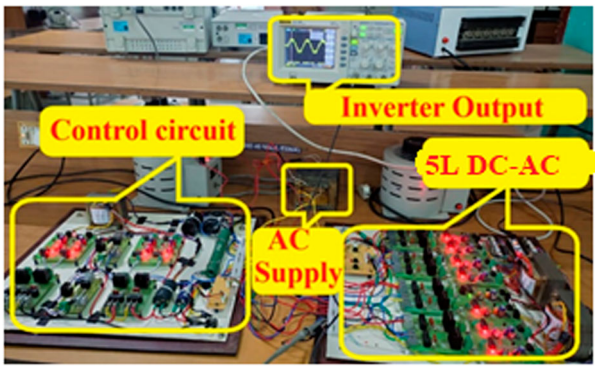

Figure 5. Experimental set-up.

V. Experimental results

Simulation results are verified at the hardware level by building a hardware prototype model from the proposed topology with parameters such as a DC input of 40 V, capacitors each 1 nF, an inductance of 3 mH, a switching frequency of 10 kHz, a load resistance of 100 Ω and a modulation index of 0.9. The duty cycle δ for converter operation is used up to 0.8; the experimental model is illustrated in Figure 5.

Experimental and simulation waveform is measured from the pure resistive load as shown in Figure 6. Boost inductor L charging from DC supply with the duty cycle δ of 0.8, which produces the output V_0 is upto 200 V. Because of the 5-level circuit output also has five-fold structured voltage between 200 V positive and negative; if DC is the continuous capacitor C_b can balance up to 100 V. For R load circuit output and positive fault clearance is obtained within 2 s, as shown in Figure 7.

The sinusoidal load current with its magnitude value is around 1.8 A. This is calculated and also obtained practically from the impedance value of 100 ohms and the input AC voltage of 180 V. Voltage gain from theoretical and practical is approximately 5. The theoretical and practical results are almost equal as shown in Figure 4 and Figure 8, respectively. Experimental result and negative fault clearance are obtained within 2 s from the proto-type model, as shown in Figure 5. The load used in the prototype model is R load and instantly load changes without affecting AC voltage. Table 3 shows the comparison of parameters. Table 4 shows power loss distribution and Table 5 shows Resistance, Modulation index and power.

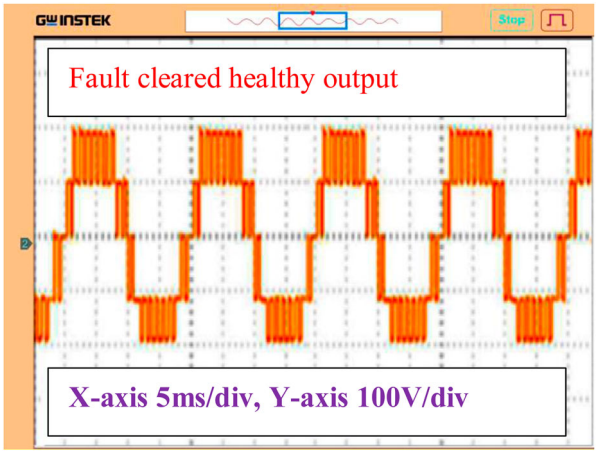

Figure 6. Normal input and output voltage.

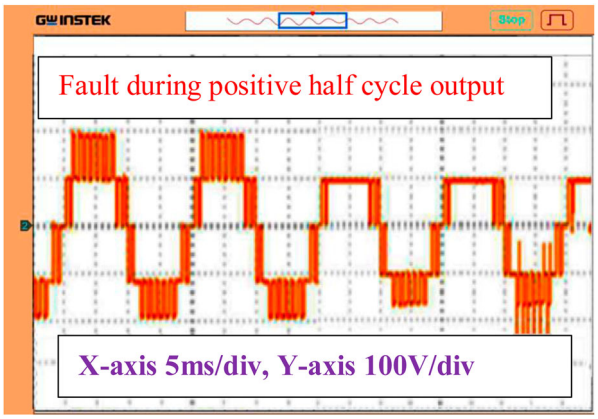

Figure 7. Positive half-cycle fault and clearance.

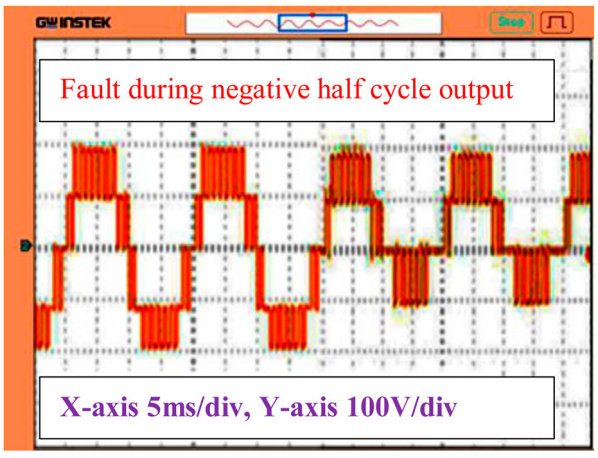

Figure 8. Negative half-cycle fault and clearance.

VI. THD calculation

Output phase voltage is expressed using Fourier series expansion expressed in Equation (20).

$$V(t) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi} V_n \sin n\alpha_n \tag{20}$$

Table 3. Parameter comparison.

Parameters	Traditional converter [12]	Proposed converter
DC side voltage	100 V	100 V
AC side grid voltage	200 V	200 V
Frequency	50 Hz	50 Hz
Power output	200 W	300 W
Switching frequency	50 KHz	50 KHz
Efficiency	96.9%	97.9%
THD full load	12.6–18.3%	5.4–16.3%

Table 4. Power loss distribution.

Components	Power loss %	Power loss
Q_1–Q_4	19%	7.98 W
Q_5–Q_6	9%	3.78 W
Q_7–Q_8	15%	6.3 W
Q_9–Q_{10}	15%	6.3 W
Inductor (L)	42%	17.64 W

Table 5. Resistance, modulation index and power.

Components/Parameters	Value
IGBT	0.10 Ω
Boost inductor	0.22 Ω
Modulation index	0.9
Input power	2000 W
Output power	1958 W

Vn is the output voltage expressed in Equation (21)

$$Vn = \frac{4(V_{dc1}\cos n\alpha_1 + V_{dc2}\cos n\alpha_2 + .. + V_{dcn}\cos n\alpha_n)}{n\pi} \tag{21}$$

THD is expressed in Equation (22)

$$\text{THD} = \sqrt{\frac{\sum_{n=1,3,5}^{\infty} \frac{4}{n\pi} V_n \sin n\alpha_n}{Vn}} \times 100 \tag{22}$$

If the output power is greater than 60% THD the obtained value is 4.5% during both modes of operation. The designed prototype converter with the specification of 48 V and 250 W achieved a THD value of 2.3%. A comparison between traditional and proposed converters [12] is given in Table 3. Efficiency and THD values show the proposed converter with the prototype model is better than the traditional converter. THD values from different power and switching power loss comparisons are shown in Figures 9 and 10, respectively, where it is obvious that much higher efficiency can be achieved by the proposed converter than the traditional converters. Detailed power loss breakdown of active switches of the proposed converter and the traditional converter is calculated.

VII. Conclusion

A newly designed 5L NCA DC–AC converter is proposed in this paper. The proposed 5L NCA DC–AC converter can suppress common mode voltage from

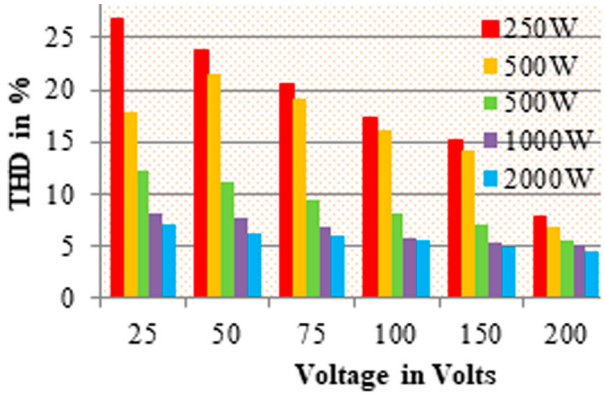

Figure 9. THD values from different powers.

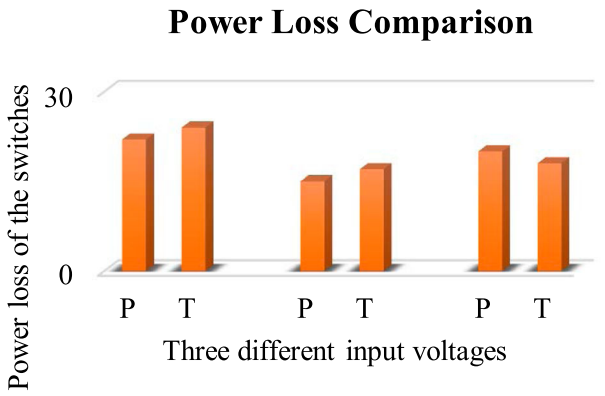

Figure 10. Switching power loss comparisons.

high frequency, with some add-on merits such as voltage step-up, voltage usage, limited stress from voltage and more compatibility. The above advantageous features are obtained from one-stage = structured topology without compromising efficiency. Validation of the proposed topology results in simulation and hardware levels. Hardware model results are feasible and also viable in all the levels of voltage from different conditions and also fault clearance is found. Fault clearance is obtained within 2 s.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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References

[1] Wang C-M. Novel zero-voltage-transition PWM DC-DC converters. IEEE Trans Ind Electron. Feb. 2006; 53(1):254–262.
[2] Venkatesan M, et al. Research on FPGA controlled three phase PV inverter using multi carrier PWM control schemes. Microprocess Microsyst. 2020;76:103089.
[3] ThuraiRaaj VB, et al. Applying three port converter with dual battery storage system for hybrid power generation. J Sci Ind Res. 2020;79(7):640–649.
[4] Cheepati KR, et al. A two-step horizon optimum switching vector-model predictive control with a novel shunt active filter reference current extraction. J Circuits Syst Comput. 2022;31(10):2250174.
[5] Pari E, et al. An efficient asymmetric direct current (DC) source configured switched capacitor multilevel inverter. J Eur Syst Autom. 2020;53(6):853–859.
[6] Lee D-Y, Lee B-K, Yoo S-B, et al. An improved full-bridge zero-voltage-transition PWM DC/DC converter with zero-voltage/zero-current switching of the auxiliary switches. IEEE Trans Ind Appl. March-April 2000;36(2):558–566.
[7] Suresh K, Parimalasundar E. Design and implementation of universal converter conception et implémentation d'un convertisseur universel. IEEE Canad J Electr Comput Eng. 2022. DOI:10.1109/ICJECE.2022.3166240.
[8] Pothuraju P, et al. HBC based three phase system for wide range power conversion. IEEE Canad J Electr Comput Eng. 2021;44(3):321–328.
[9] Dost P, Sourkounis C. On influence of non deterministic modulation schemes on a drive train system with a PMSM within an electric vehicle. IEEE Trans Ind Appl. July-Aug. 2016;52(4):3388–3397.
[10] Suresh K, et al. A novel dual-leg DC-DC converter for wide range DC-AC conversion. Automatika. 2022;63(3):572–579.
[11] Pothuraju P, et al. TPTPC and BHC integrated grid connected energy storage system for power loss reduction. Circuit World. 2022. DOI:10.1108/CW-01-2021-0006.
[12] Suresh K, Sathyaseelan B, Vijay Shankar S, et al. Multi-input multi-output converter for universal power conversion operation. J Circuits Syst Comput. 2022;44(3): 2250019.
[13] Song TT, Huang N, Ioinovici A. A zero-voltage and zero-current switching three-level DC–DC converter with reduced rectifier voltage stress and soft-switching-oriented optimized design. IEEE Trans Power Electron. Sept. 2006;21(5):1204–1212.
[14] Saravanan R, et al. Integrated DC-AC and AC-DC converter using H-converter for wide range voltage applications. Circuit World. 2021;48(1):139–146.
[15] Sathyaseelan BP, et al. Design and implementation of comprehensive converter. J Electr Eng Technol. 2021;16:3093–3101.
[16] Suresh K, Parimalasundar E. A modified multi level inverter with inverted SPWM control. IEEE Canad J Electr Comput Eng. Spring 2022;45(2):99–104. DOI: 10.1109/ICJECE.2022.3150367.
[17] Saravana Ram R, et al. Dynamic partial reconfiguration enhanced with security system for reduced area and low power consumption. Microprocess Microsyst. 2020;76:103088.
[18] Suresh K, et al. Encapsulated 3Ø converter for power loss minimization in a grid-connected system. Automatika. 2022;64(1):189–197.
[19] Suresh K, Parimalasundar E. IPWM based IBMSC DC-AC converter using solar power for wide voltage conversion system convertisseur DC-AC IBMSC basé sur l'IPWM et utilisant l'énergie solaire pour un système de conversion à large tension. IEEE Canad J Electr Comput Eng. Fall 2022;45(4):394–400. DOI:10.1109/ICJECE.2022.3207873.
[20] Dong H, Xie X, Jiang L, et al. An electrolytic capacitor-less high power factor LED driver based on a "one-and-a-half stage" forward-flyback topology. IEEE Trans Power Electron. Feb. 2018;33(2):1572–1584.