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Adaptive real-time reconfiguration gate scheduling scheme using time perceptive stream

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ABSTRACT

An adaptive real-time gate scheduling scheme for time perceptive stream or packet flow is proposed to improve the standards of Ultra Low Latency during data transmission. For highly dynamic network conditions, the conventional configuration scheme is not suitable and therefore an adaptive real-time gate scheduling method is proposed for time perceptive streams. This dynamicity reconfiguration is difficult and the scheduling problem is formulated using Field Programmable Gate Array – Boolean Satisfiability Problem (FPGA-BSP) solver. This proposed scheme highly helps in network dynamicity conditions with good bandwidth utilization and high flexibility. End-to-end latency is required to be on sub-milliseconds order deal with the applications such as Industrial Internet of Things, 5G and 6G mobile, tactile internet and so on. Simulation analysis is carried out to prove the efficiency of the proposed model.

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KEYWORDS
Bandwidth utilization; time perceptive stream; ultra low latency; gate scheduling; Boolean satisfiability problem

1. Introduction

In recent and upcoming years, most of the network applications are in need of Ultra Low Latency (ULL) transmissions [1]. Some of the applications are given for reference such as Industrial Internet of Things (IIoT) [2] and tactile Internet [3] whereas the end-to-end latency should be on the order of sub-milliseconds. The most typical application is 5G mobile frounthaul where the latency requirements are based on the support of functionality splits, e.g. 100 μs [4] and 250 μs. The IEEE 802.1 standard designed for Time Sensitive Networking (TSN) [5] provides ULL in link layer. The TSN standardization comprises of different processes like flow management, synchronization, control and integrity.

Various research works have been carried out for improving the Time Aware Streams (TAS) and utilization. Some of them were discussed here as follows. To derive the worst-case traffic delay bounds, a formal timing analysis scheme is discussed in [6]. The consequences of this formal timing mechanism provide better results for ULL transmission during shaper synchronization. However, if the condition is not satisfied, then this scheme suffers longer blocking times. Ethernet-based fronthaul networks performance with TAS is performed using Opnet simulation model [7].

A Gate Shrunk (GS) Time Aware Stream method [8] was proposed; in this scheme, the GS frame is added post to the last bit of high priority frames. If GS frame is received by the TAS Bridge, then the corresponding gate closes immediately and the gates for other data traffic are opened. This process improves link utilization. Based on the real-time fluctuations with the consideration of traffic amount, the dynamic reconfiguration of time windows becomes effective. Ontology-based plug and play scheme was used for in-vehicle network for reducing TSN configuration overheads.

To determine the gate control list, a heuristic algorithm model was proposed at the runtime. Thereby the queue usage is reduced for accumulating the non-express flows and satisfies the delay requirements [9]. The stream reservation protocol of standard IEEE 802.1 Qcc was investigated [10] to configure the TAS enabled switches. This model is not suitable for high dynamic network conditions since it is based on network statistics. If the time sensitive streams changed frequently, then the statistic-based model leads to traffic loses and also latency increases. Time Aware Shaper of standard IEEE 802.1Qbv was proposed for ULL and it is specifically designed for TSN that processes typical flow control mechanism. This TAS-ULL scheme [11] was proposed to provide ULL transmission for high prioritized packets. A flattened FPGA reconfiguration-based Priority Queue (PQ) scheduler [12] was proposed to reduce the resource cost of look up tables. The non-priority schedulers are converted to priority scheduler to improve the resource efficiency [13–16].

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2. Proposed methodology

A real-time-based adaptive gate scheduling method for Time Perceptive Stream (TPS) is proposed. In this method, the active devices sent the time sensitive packets through the TPS enabled node. The system architecture of real-time TPS is shown in Figure 1. High dynamicity devices are included along with the potential characteristics of position changing and states of activation as the potential characteristic [17–19]. Based on the environmental situation, the devices get activated and deactivated to preserve the energy consumption. With respect to the state transition of nodes, the TPS gates reserve the activated streams instantly to perform ultra-low latency transmission [20,21]. Meanwhile the TPS gate reservations get cancelled immediately for the deactivated streams for bandwidth optimization.

The proposed algorithm adaptive gate scheduling using TPS is executed with the device status reports through the edge server. The optimization of routes and gate scheduling is formulated using Boolean Satisfiability problem and in this method, FPGA-based Boolean Satisfiability Problem (BSP) solver model is applied for faster computation also it deals the dynamicity of network conditions well. To ensure the ULL transmission, the gate control list of all enabled nodes should be configured in the synchronized manner.

The gate time setting problem can be addressed which seems to be a significant issue during employing TPS for real-time reconfiguration that dynamically satisfies the delay requirements. The other nodes or service class can efficiently forward the data traffic by cancelling the redundant gate reservations that improves the bandwidth utilization.

It is assumed to be that TPS has periodicity so that the upcoming data transmission times can be predicted and the transmission time can be scheduled accordingly in TPS enabled nodes as a premise of employing TPS. Delay requirements and maximum burst size are pre-determined through the employment of TPS in the nodes which helps in timing reconfiguration. The time interval length is referred as T_{Window} which is defined as window slot and it is computed using Equation (1):

$$T_{Window} = \frac{B}{L} + \sigma \tag{1}$$

Here the maximum burst size is denoted as B and link speed is denoted as L, where σ represents for a small fixed variable and it is defined for computing the transmission delay between nodes and time consumption for signal processing.

The goal of the FPGA-based reconfiguration is to identify the forwarding paths of TPS which satisfies the

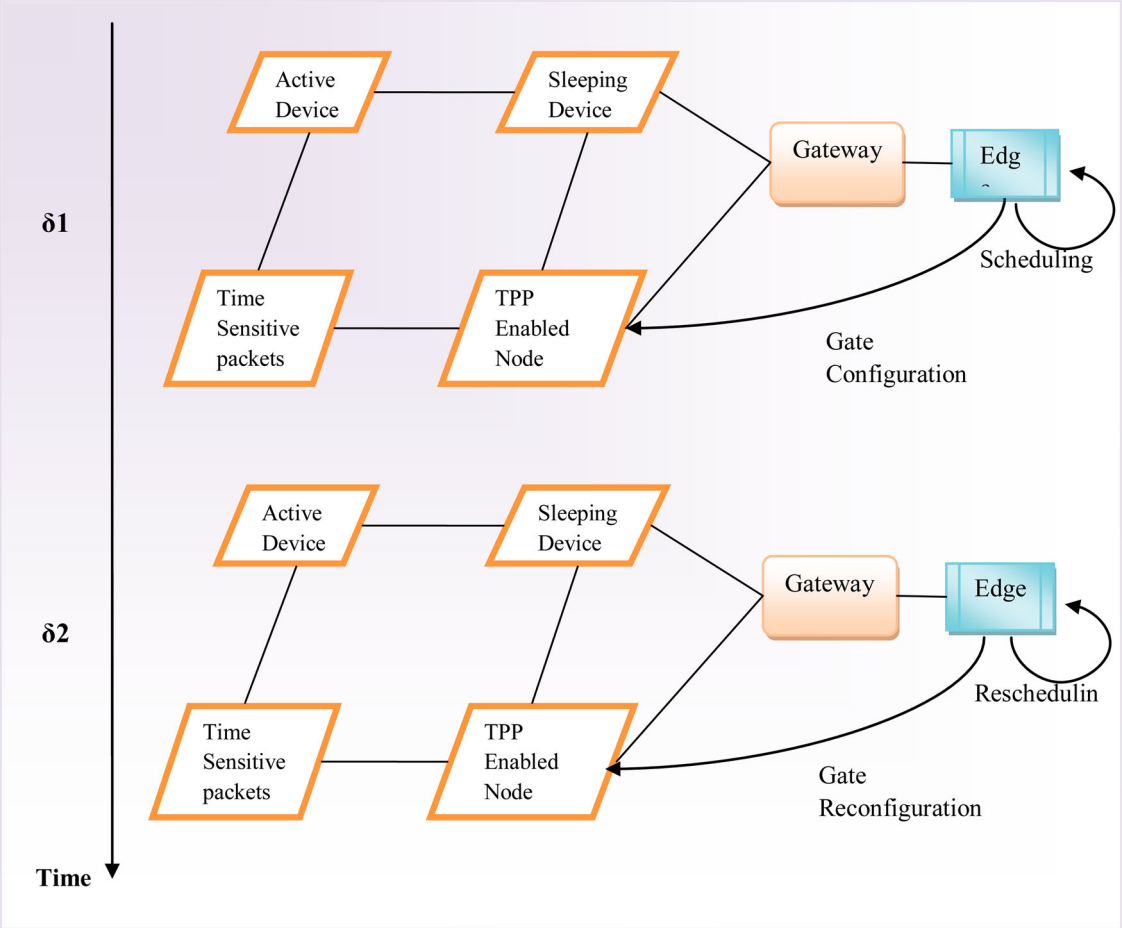

Figure 1. Proposed methodology system architecture.

capability of delay requirement in worst-case scenarios. The TPS-enabled node device should have the capability of handling maximum burst size that is sent from all the active devices. Hop by hop data transmission is performed along with synchronized gates of TPS-enabled nodes since on the basis of time synchronization among nodes the TPS is enabled and it is defined as the time slots. Therefore, the objective of defined BSP is whether all the TPS reach their destined nodes within the allotted time window slot. If multiple packet flows or stream from the different activated nodes reaches at the same destined node at the same time, then the stream suffers from queuing delay. The delay requirements determine the number of time slot windows along with the slot size. BPS objective is to check whether the time sensitive streams reach within the time slots.

Let us consider the nodes (I, J) and the connection between the nodes is determined using binary variable ($L_{I,J}$). If the binary variable $L_{I,J} = 1$, then the node I and node J are connected and if the binary variable $L_{I,J} = 0$, then the nodes I and J are not connected and the transmission between the nodes may not takes place. The streams between the nodes are processed only when the binary variable between them is 1. The number of presented time slot windows is denoted as T_{Window} and the streams transmitted between the nodes have s limit with respect to size and time T_{Limit}. The time computation for stream transmission is given in Equation (2):

$$Time = \frac{T_{Limit}}{T_{Window}} \tag{2}$$

The gate control list cycle length for the number of time interval is set as 50 and cycle time is set as 450 μs. The cycle time is periodically repeated for every 450 μs. Therefore, the activated source devices are started to transmit the packet streams at the beginning of each 450 μs. High flexibility and high utilization of bandwidth are the advantages of this proposed adaptive gate scheduling TPS model.

3. Results and discussion

The scalability of the proposed TPS model is evaluated with various numbers of packet streams, nodes and slot windows. At every 450 μs, the active TPS-enabled nodes send 1250 bytes to the gateway node. The time slot window length is set as 10 μs with the assumption of $\sigma = 0.5$ μs. TPS-enabled nodes receive random non-express traffic or streams and the clock frequency of the implemented FPGA BSP solver is 156.6 MHz. The average computation time is 0.72 μs and the TPS gates can be computed efficiently for the data transmission path.

3.1. Worst-case delay

The worst-case delay for express traffic with respect to the simulation time is shown in Figure 2 for the proposed adaptive gateway scheduling TPS model and the conventional models PQ and TAS-ULL. The proposed TPS model minimizes the delay of express data traffic by applying the FPGA-BPS dynamic reconfiguration of the gate control list. The transmission time of the gate control list is modified with respect to the prior flow distribution of the activated nodes.

3.2. Bandwidth utilization

The bandwidth utilization is computed by taking the amount of data that is received during each cycle of 450 μs. This is included for total utilization with both types of traffics such as express streams and non-express streams. The percentage level of bandwidth utilization for the proposed TPS model and the existing TAS-ULL and PQ are shown in Figure 3.

It is clearly shown that the proposed TPS model achieves better percentage level of bandwidth utilization when compared to the existing schemes. The proposed TPS model alters the bandwidth for the non-express traffic that is transmitted from the other activated nodes. Therefore the proposed model

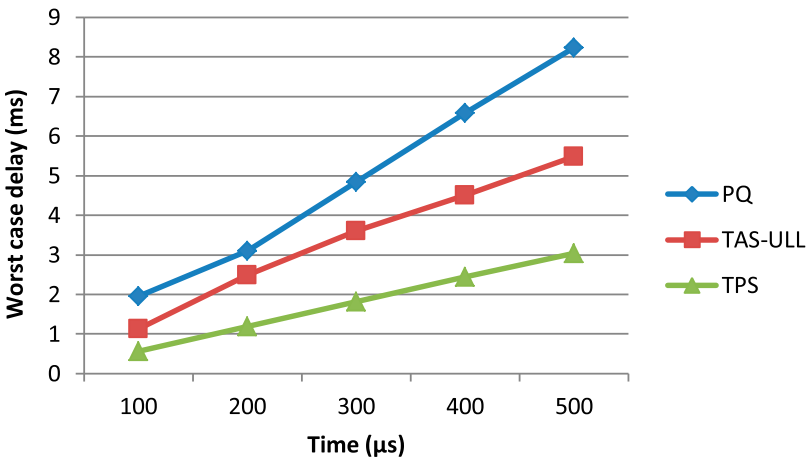

Figure 2. Worst-case delay traffic.

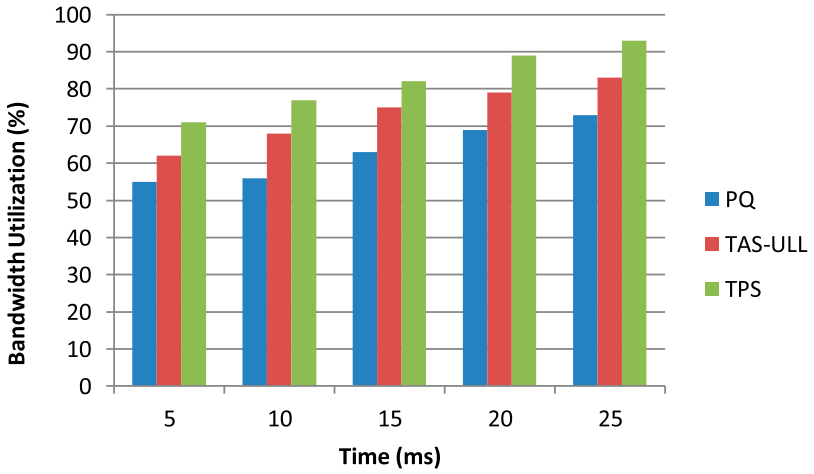

Figure 3. Bandwidth utilization (%).

achieves better bandwidth utilization due to the reconfigure gate control list of the TPS enabler compared to PQ and TAS-ULL.

4. Conclusion

The proposed TPS algorithm of adaptive gate scheduling is executed with the device status reports through the edge server. The optimization of routes and gate scheduling is formulated using BSP and in this method FPGA-based BSP solver model is applied for faster computation also it deals the dynamicity of network conditions well. To ensure the ULL transmission, the gate control list of all enabled nodes is configured in the synchronized manner. Simulation analysis proves the proposed TPS model efficiency in terms of delay requirements and bandwidth utilization.

Disclosure statement

No potential conflict of interest was reported by the author(s).

References

[1] Nasrallah A, Thyagaturu AS, Alharbi Z, et al. Ultra-low latency (ULL) networks: The IEEE TSN and IETF DetNet standards and related 5G ULL research. IEEE Commun Surv Tutor. 2018;21(1):88–145.

[2] Schulz P, Matthe M, Klessig H, et al. Latency critical IoT applications in 5G: Perspective on the design of radio interface and network architecture. IEEE Commun Mag. 2017;55(2):70–78. doi:10.1109/MCOM.2017.1600435CM

[3] Maier M, Chowdhury M, Rimal BP, et al. The tactile internet: Vision, recent progress, and open challenges. IEEE Commun Mag. 2016;54(5):138–145. doi:10.1109/MCOM.2016.7470948

[4] Interface C.P.R. Common public radio interface: eCPRI interface specification (Vol. 1, p. 0). Technical Report eCPRI specification. 2018.

[5] Bhattacharjee S, Schmidt R, Katsalis K, et al. Time-sensitive networking for 5G fronthaul networks. ICC 2020–2020 IEEE International Conference on Communications (ICC) (pp. 1–7). IEEE; 2020.

[6] Thiele D, Ernst R, Diemer J. Formal worst-case timing analysis of Ethernet TSN's time-aware and peristaltic shapers. 2015 IEEE Vehicular Networking Conference (VNC) (pp. 251–258). IEEE; 2015.

[7] Al-Hares MK, Assimakopoulos P, Muench D, et al. Modeling time aware shaping in an Ethernet fronthaul. GLOBECOM 2017–2017 IEEE Global Communications Conference (pp. 1–6). IEEE; 2017.

[8] Farzaneh MH, Knoll A. An ontology-based Plug-and-Play approach for in-vehicle Time-Sensitive Networking (TSN). 2016 IEEE 7th Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON). (pp. 1–8). IEEE; 2016.

[9] Nasrallah A, Thyagaturu AS, Alharbi Z, et al. Performance comparison of IEEE 802.1 TSN time aware shaper (TAS) and asynchronous traffic shaper (ATS). IEEE Access. 2019;7:44165–44181. doi:10.1109/ACCESS.2019.2908613

[10] Raagaard ML, Pop P, Gutiérrez M, et al. Runtime reconfiguration of time-sensitive networking (TSN) schedules for fog computing. 2017 IEEE Fog World Congress (FWC). (pp. 1–6). IEEE; 2017.

[11] Nakayama Y, Yaegashi R, Nguyen AHN, et al. Real-time reconfiguration of time-aware shaper for ULL transmission in dynamic conditions. IEEE Access. 2021;9:115246–115255. doi:10.1109/ACCESS.2021.3105420

[12] Li Z, Wan H, Deng Y, et al. A resource-efficient priority scheduler for time-sensitive networking switches. CCF Trans Network. 2020;3(1):21–34. doi:10.1007/s42045-020-00034-x

[13] Ballesteros A, Barranco M, Proenza J, et al. An infrastructure for enabling dynamic fault tolerance in highly-reliable adaptive distributed embedded systems based on switched ethernet. Sensors. 2022;22(18):7099, doi:10.3390/s22187099

[14] Safari S, Ansari M, Khdr H, et al. A survey of fault-tolerance techniques for embedded systems from the perspective of power, energy, and thermal issues. IEEE Access. 2022;10:12229–12251. doi:10.1109/ACCESS.2022.3144217

[15] Shashank, Sreedevi I. Distributed network of adaptive and self-reconfigurable active vision systems. Symmetry (Basel). 2022;14(11):2281, doi:10.3390/sym14112281

[16] Nakayama Y, Yaegashi R, Nguyen AHN, et al. Real-time reconfiguration of time-aware shaper for ull transmission in dynamic conditions. IEEE Access.

2021;9:115246–115255. doi:10.1109/ACCESS.2021.3105420

[17] Ji X, Yin Z, Zhang Y, et al. Real-time autonomous dynamic reconfiguration based on deep learning algorithm for distribution network. Electr Power Syst Res. 2021;195:107132. doi:10.1016/j.epsr.2021.107132

[18] Nakayama Y, Hisano D. Multi-stream gate control of time aware shaper for high link utilization. 2021 IEEE International Conference on Communications Workshops (ICC workshops). (pp. 1–6). IEEE; 2021.

[19] Nasrallah A, Balasubramanian V, Thyagaturu A, et al. Reconfiguration algorithms for high precision communications in time sensitive networks. 2019 IEEE Globecom Workshops (GC Wkshps). (pp. 1–6). IEEE; 2019.

[20] Podobas A, Sano K, Matsuoka S. A survey on coarse-grained reconfigurable architectures from a performance perspective. IEEE Access. 2020;8:146719–146743. doi:10.1109/ACCESS.2020.3012084

[21] Maile L, Hielscher KSJ, German R. Delay-guaranteeing admission control for time-sensitive networking using the credit-based shaper. IEEE Open J Commun Soc. 2022;3:1834–1852. doi:10.1109/OJCOMS.2022.3212939