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PSPICE modelling and design of a snubber circuit for the matrix converter

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SUMMARY

In matrix converters one of the basic commutation strategies is the dead time current commutation. Although the application of this commutation strategy is simple and easy, the design of snubber parameters becomes crucial to control the voltage spikes across the switches due to the open circuiting of the motor winding during the dead time. This paper deals with the design of a simple snubber circuit for the matrix converter. Complicated power circuit of the converter and its operation make the design of the snubber circuit difficult even for a simple snubber arrangement. The matrix converter power circuit applying dead time strategy is built up from 9-bidirectional switches and each switch should have a snubber due to the absence of freewheeling paths. In this work, an R-C turn-off snubber circuit connected across to each bidirectional switch is used to limit the device voltage to an appropriate level. This snubber arrangement has been analyzed and then the PSPICE modelling of the matrix converter including snubbers has been performed for various operating conditions. A 2.2 kW matrix converter power circuit using IGBT devices has been constructed by considering the analysis and simulation results. Experimental results are presented to confirm the theoretical results and therefore to correct operation of the system.

***Key words**: PSPICE, snubber circuit, matrix converter.*

1. INTRODUCTION

Matrix converters are direct AC-AC converters and can perform frequency and voltage transformation without the need for intermediate energy storage elements such as the DC link filter which is required by the more common rectifier-voltage source inverter circuit is complicated because of the power circuit structure of the converter and its operation. This simple snubber circuit arrangement has the disadvantage of high current stress in the devices at turn-on resulting in higher switching and snubber losses.

In order to determine appropriate snubber parameters, some conditions has to be considered regarding the operation of the matrix converter. That is, the input voltages, output current, switching sequences of the bidirectional switches and time delay (dead time) are effectively important parameters. First, the snubber circuit has been analyzed for a certain condition. Second, the PSPICE modelling (including the semiconductor models) of the complete system has been obtained and then, the behaviour of the snubber circuit for different snubber parameters and conditions has been simulated by using this model. Finally, regarding these results a snubber circuit has been designed for the prototype converter and very good correlation between the theoretical and measured results were obtained.

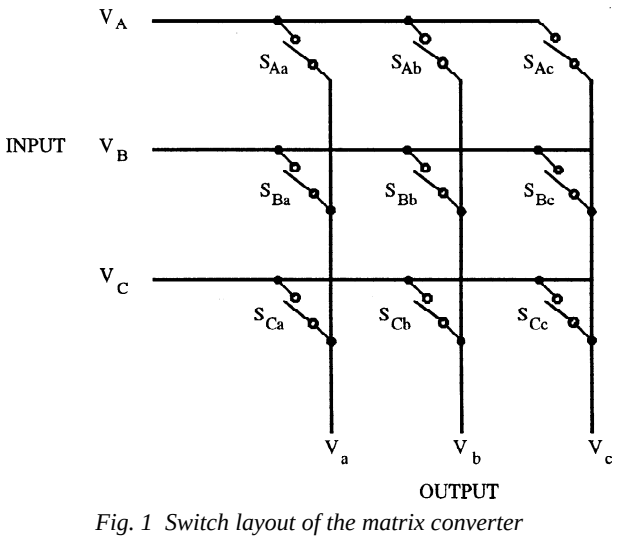

Fig. 1 Switch layout of the matrix converter

2. ANALYSIS OF THE SNUBBER CIRCUIT

One output phase of the matrix converter shown in Figure 2 has been considered for the analysis. The matrix converter under consideration is rated at an input voltage of 250 V line and an output current of 7.2 A. IRGBC2OU ultrafast IGBT has been used in the converter as controlled switch. This device has max. 375 ns turn-off time and does not contain body diode [9]. Therefore, a delay of 500 ns is found suitable between drive signals to avoid a short circuit of the input lines. It has been assumed that the 3-phase input voltage and the output current of the converter stay constant during one period of the switching frequency, which is 2 kHz. In addition, stray inductances in the commutation path are ignored. The worst case operating condition for the snubber circuit occurs when maximum output current flows when any one of the line to line input voltages is a maximum. This situation is depicted in Figure 2 by considering the voltage and current ratings of the converter. The snubber parameters in Figure 2 are determined by considering the device ratings and circuit operation. Selection of the snubber resistance depends on two criteria. First, this resistor discharges the snubber capacitance at turn-on. Therefore, the value of the snubber resistor should be chosen in a way that discharge time of the snubber capacitor must be equal or smaller than the minimum duty cycle of any switch in the converter. Second, the snubber resistor determines peak value of the discharge current and hence the switch current stress. For this reason, an appropriate snubber resistor should be chosen to keep the device peak current below its rating and fully to discharge the capacitor at turn-on. On the other hand the selection of the snubber capacitor is also important respect to the device voltage. During the dead time the load current is taken over by the snubber circuit and value of the snubber capacitance determines the voltage across the device at turn-off. when this capacitor is chosen, the device voltage rating must be considered. According to the criteria mentioned above the snubber parameters, R and C have been estimated for the operating conditions as 21 Ω and 0.022 μF, respectively. However, optimum snubber design for various conditions is given in the next section where the complete system is modelled.

The snubber circuit operation is analyzed for a complete switching sequence assuming initially that S_{Aa} is on followed by commutation to S_{Ba} then to S_{Ca} and finally back to S_{Aa}. The analysis is started assuming that the bidirectional switch, S_{Aa} has been on and the switches S_{Ba} and S_{Ca} have been off for some time. This condition can be represented by the equivalent circuit shown in Figure 3a. During this interval the output current is supplied by S_{Aa} bidirectional switch and the voltages across the bidirectional switches stay at constant level.

Figure 3b shows the equivalent circuit for the instant in which S_{Aa} is just turned-off. During this interval where all three bidirectional switches are off, the load current is supplied by the three snubbers. If the equivalent circuit shown in Figure 3b is analyzed, it is found that the snubber currents are equal and add to give the output current. Assuming a maximum output current of 10 A peak the snubber currents are given by:

$$I_{S1} = I_{S2} = I_{S3} = 3.33A \tag{1}$$

Therefore, the voltages across the snubber resistance and capacitance during this interval are given by:

$$\begin{aligned} V_R &= I_S \cdot R \\ V_C &= \frac{I_S}{C} t + V_C(0) \end{aligned} \tag{2}$$

where, I_S is the snubber current, V_C is the capacitor voltage and $V_C\,(0)$ is the initial capacitor voltage.

Since the snubber current is constant during this interval the voltages across the snubber resistances remain constant at 70 V. The change of the snubber

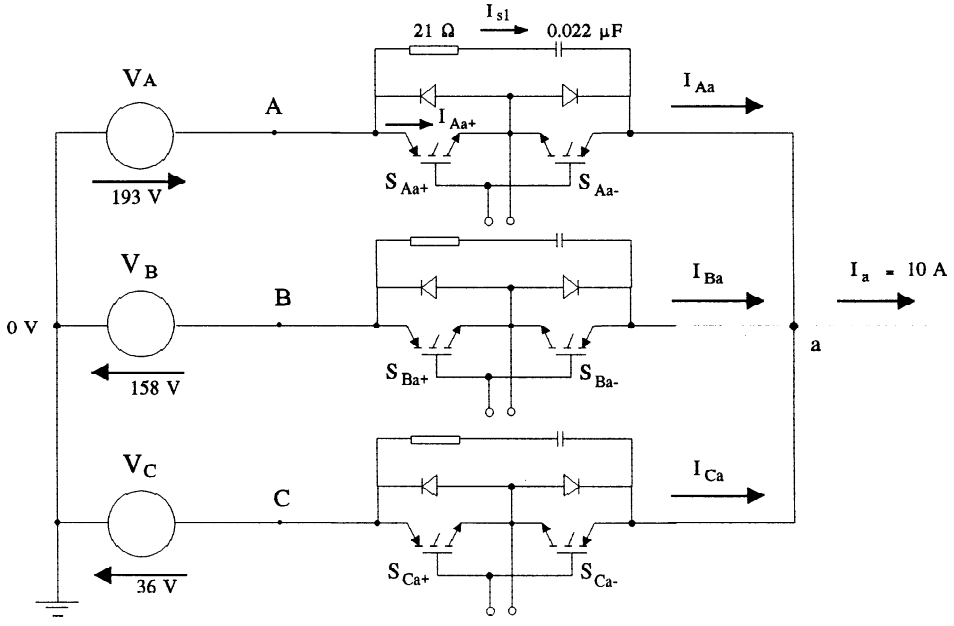

Fig. 2 Snubber circuit with the bidirectional switches

capacitance voltage after the 500 ns delay time can be calculated by using Eq. (2):

$$DV_C = \frac{3.33}{0.022 \cdot 10^{-6}} 0.5 \cdot 10^{-6} = 75.75\,V \qquad (3)$$

This condition is shown in Figure 3c. Figure 3d shows the equivalent circuit for the instant at which S_{Ba} is turned-on. Again, if this condition is analyzed, the snubber currents can be found to be:

$$I_{S1} = I_{S2} = I_{S3} = 13.1\, e^{-t/RC} A \qquad (4)$$

It is important to note from Figure 3d that, the snubber current, I_{S2} is taken over by the switch, S_{Ba}. This explains why this snubber arrangement causes an increase in the device current rating mentioned earlier. This also increases the switching losses. If the analysis is carried on until the end of the switching period, the worst case the snubber current waveform, I_{S1} and the device voltage, V_{Aa} are obtained as shown in Figure 4.

As can be seen from the analysis results, the device voltage and current waveforms at switching mainly depend on the time delay introduced between the complementary switches, input voltages, output current and snubber parameters. The snubber loss depends on the snubber capacitance, the dead time and a number of parameters and is given in Section 4.

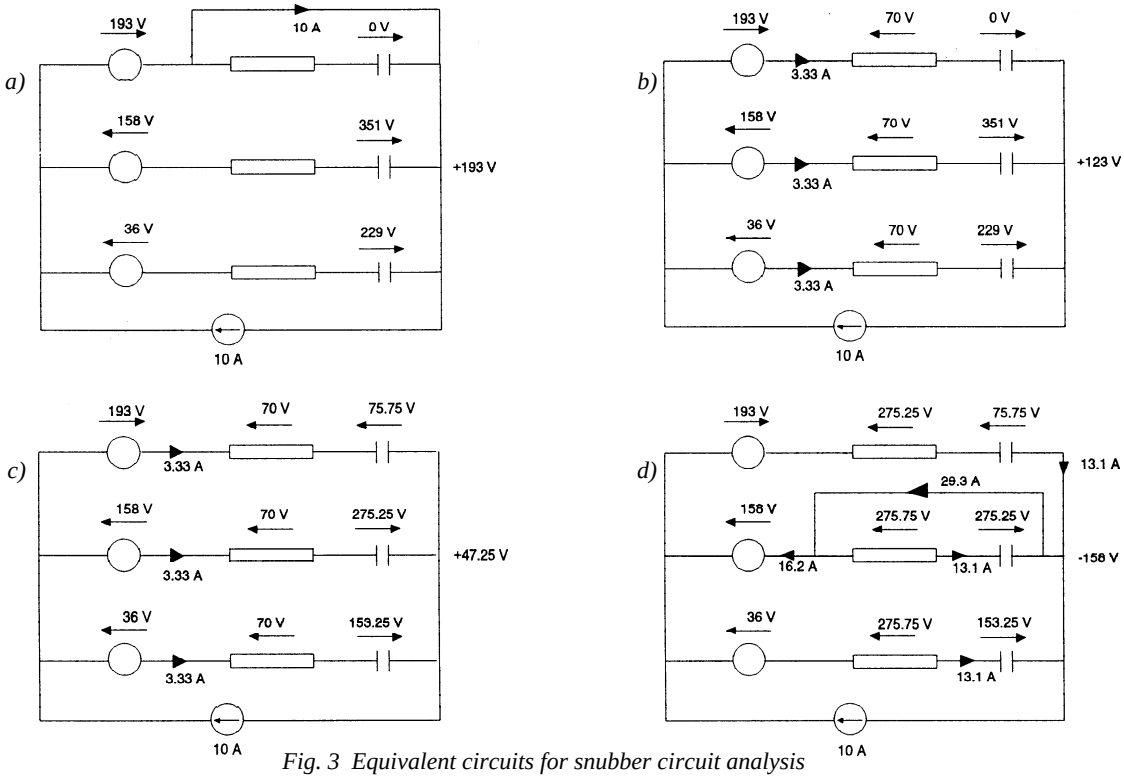

Fig. 3 Equivalent circuits for snubber circuit analysis

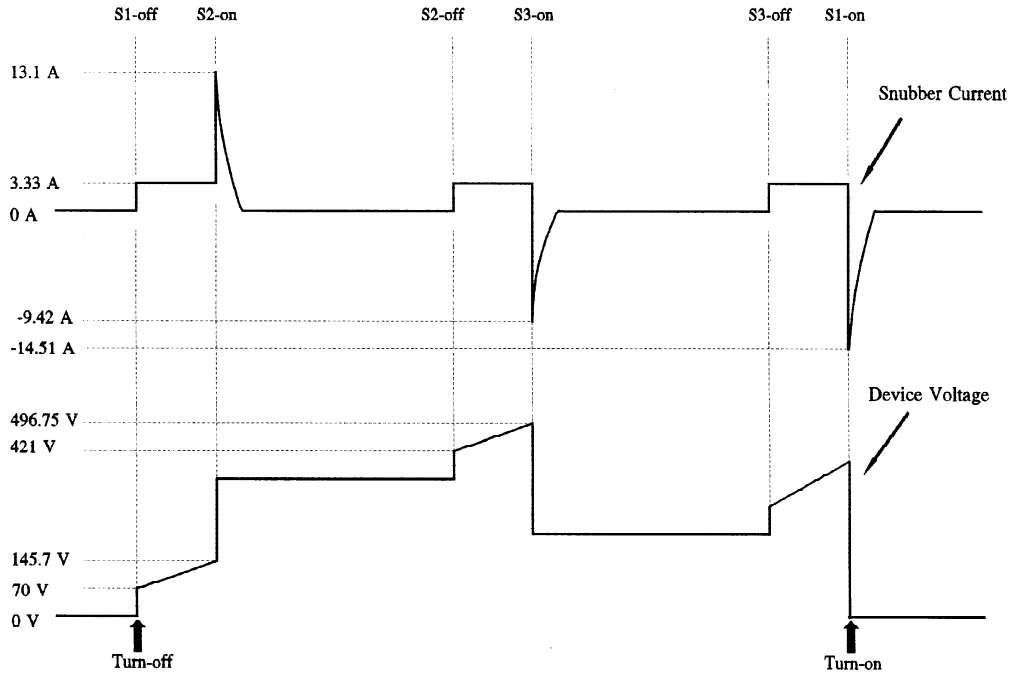

Fig. 4 Worst case waveforms of snubber current and device voltage for switch S_{Aa}

3. THE PSPICE MODELLING

The bidirectional switch with snubbers shown in Figure 5 has been considered for modelling 3-phase matrix converter by using PSPICE software package [10]. The parameters of the components used in the model have been provided by their manufacturer companies in order to get more realistic results [11]. Simulation conditions are taken same as those of the analysis. Figure 5 represents one of the matrix converter input phases and since the PSPICE model is the same for each input phase *A*, *B* and *C*, the programme is only listed say for input phase *A* as:

```
** The matrix converter model for input phase A
X1G11   100     110     210         310     CIGBT
R11     100     410     21 W
C11     410     510     0.022 mF
VX1     510     210     DC          0 V
D11     310     100     DMOD11
D12     310     210     DMOD11
.MODEL  DMOD11  DCIS=2.2E-15  BV=1200 V  TT=0  CJO=0
```

Two of *IRGBC2OU IGBTs* connected in anti-series shown in Figure 5 is represented in the programme list as *"CIGBT"* subcircuit and it is listed as

```
.SUBCKT   CIGBT          201   200   202   205
*TERMINALS               C     G     E     -
XIGBTI            201    200   205   IRGBC20U
XIGBT2            202    200   205   IRGBC20U
.ENDS     CIGBT
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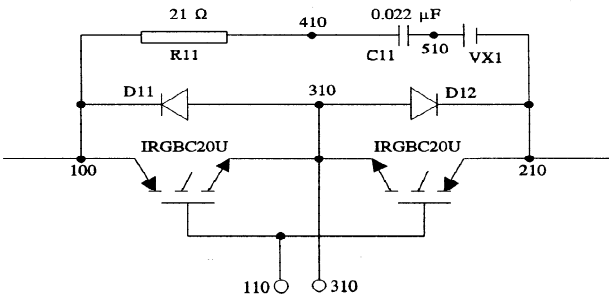

Fig. 5 The bidirectional switch with snubbers for PSPICE model

The PSPICE macro model of *IRGBC20U* labelled as *XIGBT* in the *"CIGBT"* subcircuit programme list has been maintained from the *IGBT's* manufacturer company. This N-Channel *IGBT* has the ratings of 600 V, 13 A, max. turn-off time of 375 ns and turn-on time of 34 ns. The same programme procedure has been followed for the other two input phases *B* and *C*. Thus, the complete PSPICE model of the matrix converter with snubbers has been obtained. The gate drive signal of the bidirectional switches in the model is a square-wave pulse with 50% duty cycle and ±18 V amplitude. A delay of 500 ns is also introduced between these drive signals of the complementary bidirectional switches to avoid a short circuit of the input lines.

3.1 Testing the model and simulation results

In order to examine the effectiveness of the model, tests were performed for the same conditions as those in the analysis. The test conditions were such that the instantaneous three-phase supply voltages *A*, *B* and *C* in the matrix converter model were 193 V, -158 V and -36 V, respectively. The external load resistance *R-L* was set so that the maximum steady-state current was 10 A.

Figure 6 and Figure 7 show the PSPICE simulation results for the snubber current and device voltage of S_1 bidirectional switch during turn-on and turn-off, respectively. The turn-on simulation results in Figure 6 correspond to the interval just starting before the point marked as "Turn-on" in the analysis results shown in Figure 4. Similarly, the results in Figure 7 correspond to the related part of the analysis results which start from the point marked as "Turn-off' and last for a while. As can be seen from the simulation and analysis results, the simulated results of the PSPICE matrix converter model are nearly identical to the results obtained in the analysis. However, the sharp edges in the analysis results do not appear in the corresponding simulation results. This is because the *IGBTs* and other devices used in the PSPICE model are not taken as ideal and they almost represent their real model.

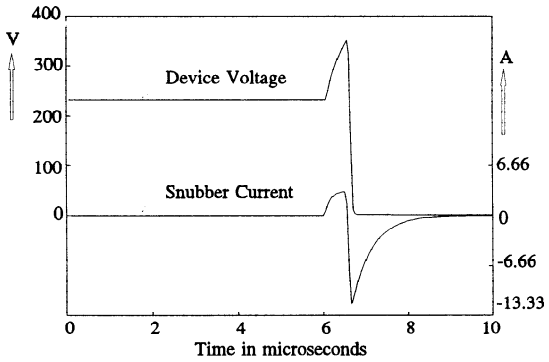

Fig. 6 Simulation results: Device voltage and snubber current at turn-on

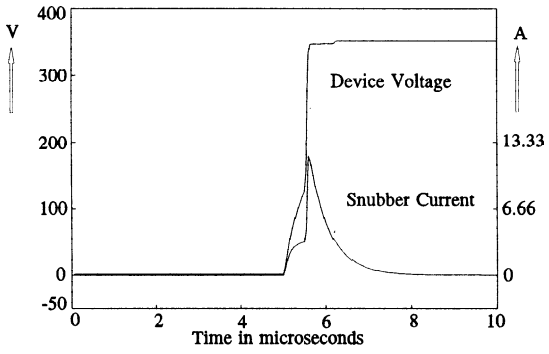

Fig. 7 Simulation results: Device voltage and snubber current at turn-off

4. EXPERIMENTAL WORK AND RESULTS

In this work, a 3-phase to 3-phase prototype matrix converter rated at 2.2 kW has been constructed. The bidirectional switches in the matrix converter power circuit have a simple *R-C* snubber circuit to limit the device voltage to an appropriate level during turn-off and provide the load current during the delay time. The values of *R-C* snubber elements have been determined by considering the analysis and PSPICE simulation results done in the previous section. The *R-C* snubber element values are specified in Appendix. In this converter, the total power loss in the snubbers is given by [7]:

$$P_{snub} = f_s\left[3I_0^2\left(Rt + \frac{t^2}{2C}\right) + \frac{27CV_L^2}{2}\right] \qquad (5)$$

where: f_s is the switching frequency, t is the dead time, V_L is the rms value of the input line voltage and I_0 is the rms output current.

As it can be seen from the Eq. (5), the snubber loss effectively changes with the dead time. That is, bigger value of the dead time results in higher snubber loss. On full load current (7.2 A), the total snubber loss is calculated as 40.8 W by using Eq. (5) and it was measured to be 43 W which is in good agreement. These losses are practically acceptable.

Unfortunately, it proved very difficult to obtain practical results for the snubber waveforms at full power due to interference between the measuring equipment and the control circuitry. For this reason, the previous analysis and PSPICE simulation were repeated for an output current of 4 A and the simulation results for this condition are given in Figures 8 and 9. Practical results for this condition were also taken as shown in Figures 10 and 11. As it can be seen from Figures 8-11, a very good correlation between the theoretical and measured results were obtained at 4 A suggesting that the analysis and simulation can be used with confidence to predict the device stresses at 10 A. The analysis and simulation results show that the design snubber parameters for a 500 ns delay are suitable to keep the device voltage and current stresses below the device ratings. Therefore, the snubber parameters, *R* and *C* used in the analysis and simulation have been also used in the prototype converter with confidence.

5. CONCLUSIONS

In this paper, a simple snubber circuit has been presented to be used in a matrix converter. First, the snubber parameters have been estimated by considering the device voltage and current ratings and the delay time introduced between the bidirectional switches for safe commutation. The analysis of the matrix converter for one output phase has been done by using the estimated snubber parameters. It has been

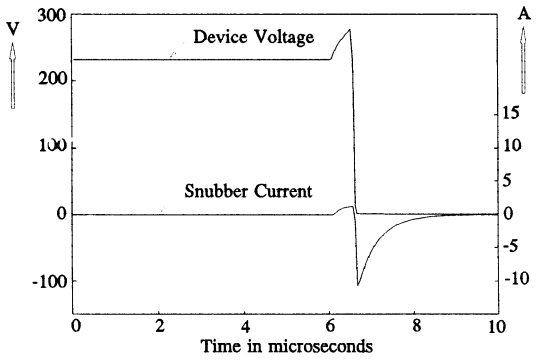

Fig. 8 Simulation results: Device voltage and snubber current at turn-on

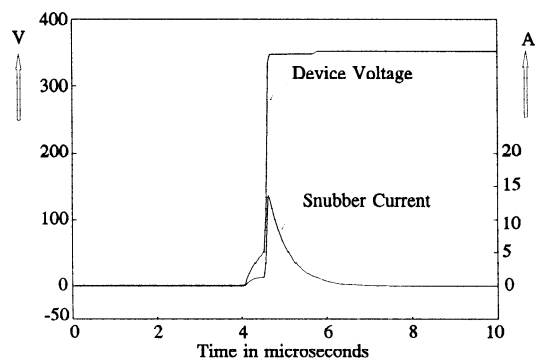

Fig. 9 Simulation results: Device voltage and snubber current at turn-off

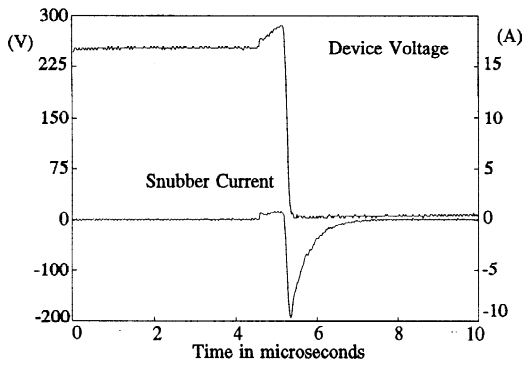

Fig. 10 Experimental results: Device voltage and snubber current at turn-on

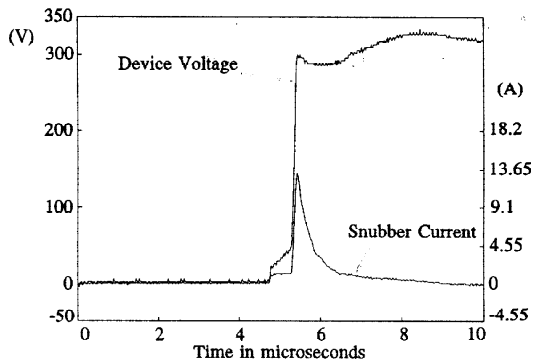

Fig. 11 Experimental results: Device voltage and snubber current at turn-off

seen from the analysis results that the device voltage and current values have remained below its maximum allowable ratings. To confirm the analysis results the model of the matrix converter including snubbers has been obtained using PSPICE software package. The simulation results obtained from the model are similar to their corresponding analysis results. As a result, various snubber values at different operating conditions may be used in the simulation to obtain optimum snubber parameters to keep the device voltage and current stresses just below the device ratings resulting in lower snubber losses. A 2.2 kW matrix converter power circuit has been constructed by considering the analysis and simulation results. Practical device voltage and snubber circuit waveforms obtained from the prototype converter have been compared to those of the simulation results and it has been shown that the theoretical and experimental results confirm each other.

It has been demonstrated that by designing appropriate snubber parameters, a simple snubber circuit provides both device protection and continuous load current during the delay time introduced for safe commutation. Hence, this snubber circuit keeps the power circuit simple as well as its control.

APPENDIX

Ratings of the snubber parameters:

R = 21 W, 4 W, C = 0.022 mF, 1000 V

Specification of IRGBC2OU:

$I_C = 13\ A$ at $T_C = 25\ °C$, $V_{CE} = 600\ V$

Turn-on delay time is 22 ns and Turn-on rise time is 12 ns.

Turn-off delay time is 95 ns (max) and Turn-off fall time is 280 ns (max).

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MODELIRANJE VRŠNE SNAGE I PROJEKTIRANJE STRUJNOG KRUGA S PRIGUŠNIM ELEMENTOM ZA MATRI^NI PRETVARA^

SA@ETAK

U matri~nim pretvara~ima jedna od osnovnih strategija jest mrtvo vrijeme prespajanja struje. Premda je primjena ove strategije prespajanja jednostavna i lagana, projektiranje parametara prigušivanja postaje va`nim za kontroliranje vršnih napona kroz prekida~e, radi otvorenog strujnog kruga okretanja motora tokom mrtvog vremena. Ovaj rad se bavi projektiranjem jednostavnog strujnog kruga s prigušnim elementom za matri~ni pretvara~. Slo`eniji strujni krugovi pretvara~a, kao i njegov rad, ote`avaju projektiranje strujnog kruga s prigušnim elementom ~ak i kod jednostavnog ure|aja za prigušivanje. Strujni krug matri~nog pretvara~a koji primjenjuje strategiju mrtvog vremena napravljen je od 9 dvosmjernih prekida~a, a svaki prekida~ treba imati prigušiva~ zbog odsustva putova slobodnog hoda. U ovom radu jedan R - C isklju~eni strujni krug prespojen na svaki dvosmjerni prekida~ koristi se za ograni~enje napona ure|aja na primjerenu razinu. Analizira se ure|aj za prigušivanje, a modeliranje vršne snage P matri~nog pretvara~a, uklju~uju}i i prigušiva~e, napravljeni su za razli~ite radne uvjete. Jedan matri~ni pretvara~ od 2.2 kW snage strujnog kruga, koji koristi IGBT ure|aje, konstruiran je vode}i ra~una o analizi i rezultatima simulacije. Prikazani su rezultati eksperimenata kako bi se potvrdili teorijski rezultati, te korigirao rad sustava.

***Klju~ne rije~i**: PSPICE, strujni krug, matri~ni pretvara~.*