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A partly isolated three-port converters with an improved power flow for integrating PV and energy storage into a DC bus

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ABSTRACT

This study proposes an integrated design of isolated three-port high-gain DC-DC converters to link PV (photovoltaic) and batteries for a standalone system. Three switches are required to process power between inputs and outputs while maintaining minimal circulating current flow between ports and permitting bidirectional power flow at the battery port. Furthermore, owing to the leakage inductance of the transformers, ZVS (zero-voltage switching) of all the switches may be done using a mutual active clamp circuit throughout the whole operating range. As a result, the converter has fewer components and can still operate in all power conversion modes. Because the bulk of renewable energy sources have a low voltage level, the converter maintains a high voltage gain. An effective and reasonably priced converter is the outcome of these qualities. Using MATLAB simulation, the suggested converter's detailed operating principles, characteristics, design concerns and control method are examined. In order to confirm the viability and efficacy of the suggested solution, an experimental prototype is constructed and tested.

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KEYWORDS
PV (photovoltaic); ZVS (zero-voltage switching); DISO (double-input-single-output); SISO (single-input-single-output); SIDO (single-input-double-output)

1. Introduction

Renewable energy sources (RES) including solar panels, fuel cells and wind turbines have attracted ongoing interest due to the world's increasing energy crisis, the depletion of its resources and greenhouse gas reduction initiatives [1,2]. However, depending on the temperature and weather, RES are irregular and unreliable due to these and other environmental conditions. Batteries and other energy storage components are necessary to provide a stable power supply and to balance the gap between RES and load. In order to handle sources, storages and loads while also simplifying the overall management system, a wide variety of TPCs (three-port converters) have been proposed as replacements to multiple standalone two-port converters [3].

Isolated PV systems are increasingly being used as DG (distributed generator) in recent years. To get around the intermittent nature of PV systems supplying isolated loads, ESS (Energy Storage Systems) must be used in combination with PV modules. For standalone PV systems, batteries are a common ESS used to balance collected PV output with load requirements. Two separate DC-DC converters or ITPCs (integrated TPCs) are utilized to handle the various operating voltage levels of the PV module, battery and load. The key benefits of TPCs over standalone DC-DC converters are their compactness, lower component count and less weight. There are three types of topologies for TPCs: non-isolated [4], partially-isolated [5] and fully-isolated [6].

In most situations of ITPCs are shown in Figure 1, consist of several full/half-bridge converters and rectifiers, and all three ports are isolated from one another using one or two transformers [7–10]. As a result, managing power among the ports is simple. When power is exchanged between these two ports, the third port becomes inactive, resulting in non-operational components. The use of full-scale high-frequency transformers to improve voltage gain increases the weight, size and magnetic losses of an ITPC. As a result, these parameters frequently have to be traded off. ITPCs can easily sustain soft-switching, although they often have an excessive amount of semiconductors. The converter in includes fifteen switches and six diodes, to give you an example. Maximum efficiency in this converter is 85%, and gentle switching was unable to significantly increase efficiency. Voltage-fed ports are used in [8–12], when redundant filters are required for applications involving renewable energy.

On the other hand, there is no port isolation in NITPCs (Non-Isolated TPCs) [13–15], block diagram shown in Figure 2. The fundamental benefit of NITPC is that practically every component is used in every operational mode [12,13]. In, two NITPCs were launched. These converters use the fewest switches and

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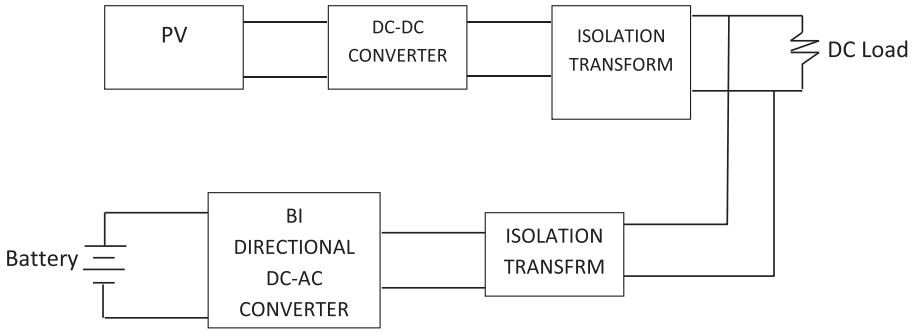


Figure 1. Block diagram of fully-isolated three-port converter.

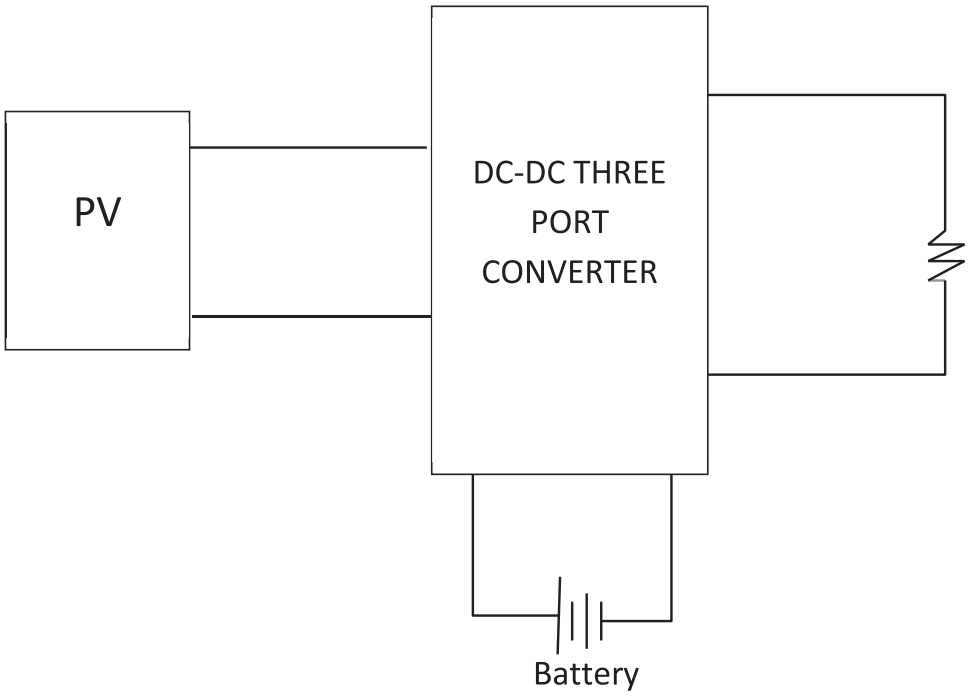


Figure 2. Block diagram of non-isolated three-port converter.

diodes overall. They no longer have soft-switching, and their voltage gain is minimal. Except for, NITPCs typically have minimal voltage gains. Only has two current-fed ports, making it the NITPC that is most suited for applications using renewable energy.

PITPCs (Partially-Isolated TPCs) block diagram is shown in Figure 3, a partial scale transformer is used to isolate the main output port from the input PV and Battery ports [16,17], also soft-switching of PITPC is achieved using partial state transformer leakage inductance [17]. Although a transformer has been used, PITPCs typically have limited voltage gains [16]. Despite the fact that there are several semiconductors, none of the cited references have current-fed terminals.

PV and battery port are non-isolated ports which is not required to handle a high voltage ration because the selected battery and PV has low voltage difference. But the PV and battery to DC load is isolated port which can handle the high voltage gain to obtain high voltage output. Yes, electrical isolation is crucial for the HESS application because security is so important. From a topological perspective, PITPCs may be adaptable enough to warrant the benefits of both isolated and non-isolated (such as good component sharing and few semiconductors) TPCs, including gentle switching and high voltage gain. As a result, PITPCs is suggested to handle the majority of the features listed above. For a stand-alone renewable power system application, as illustrated in Figure 18, a unique partly-isolated three-port DC–DC converter developed from a half-bridge converter is proposed in [18]. By allowing bias DC current in the transformer to cause power to flow between the input port and the bidirectional port, the proposed converter uses one of the two input-dividing capacitors as the bidirectional port. The voltage of each of the three ports can be independently adjusted because the secondary side of the transformer has two switches for synchronous regulation. According to [18], it is possible to derive various other converters by substituting the synchronous regulation in the converter with a post-regulation. The lower component count and comparatively straightforward configurations of all the

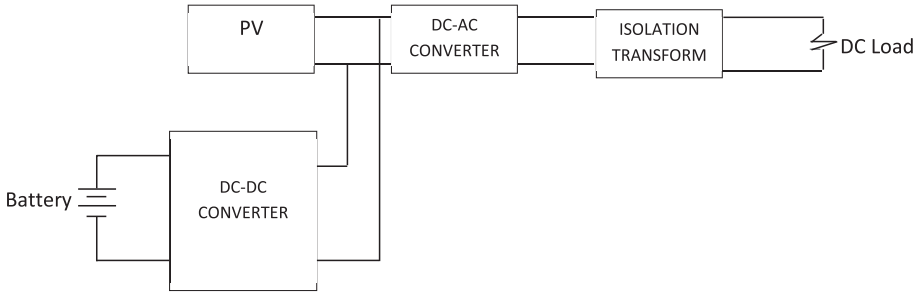


Figure 3. Block diagram of partly-isolated three-port converter.

converters that were produced are advantages. These converters have a reasonably high efficiency because there is just one step of power transfer between any two of the three ports. With the help of system-level power management, this converter has been integrated and modularized to create a DC distribution power system. Partially-isolated three-port DC–DC converters can also be obtained using the conventional full-bridge converter. Using a three-port DC–DC converter, the two switching legs of a conventional full-bridge converter are divided into two separate switching cells that can be linked to two distinct sources.

In, the TPC was derived from the integration of a bidirectional PWM converter, between the input and the battery, and a Series Resonant Converter (SRC) that transfers the power to the output. The major contribution of this proposal is utilizing the transformer's magnetizing inductance as a filter inductor for the PWM converter and the leakage inductance as a resonant inductor for the SRC, which means only single magnetic component is used in the TPC. Alternatively, the TPC was differently derived since the isolated port was the PV instead of the load as in general. The PV port is considered as a boost stage with a continuous current achieved by adding a fourth winding of the transformer to the input works as a magnetic switch. Unlike the aforementioned half-bridge TPCs, the battery is connected to the load via a boost converter since these two ports are non-isolated, which improves the power conversion efficiency between them; yet, the complexity of this TPC increases the volume and cost of it.

A partially isolated three-port converter that was proposed by the PITPCs for use in hybrid energy applications is introduced as shown in Figure 4. Two boost circuits form the converter's primary input port and a bidirectional battery port. As a result, both are current-fed, making converters more suitable for applications utilizing RES. A mutual active clamp circuit is also beneficial to boost circuits. The circuit, which employs a minimal number of semiconductors, permits gradual switching in combination with transformer leakage inductance. Two boost circuits are utilized to offer two current-fed ports. The converter proposed in this study has a high voltage gain, a high effectiveness and shares virtually all components in all modes of operation without the usage of two boost circuits. Compared to the PITPCs that are now in use, the number of semiconductors is substantially lower, although they all still use soft switching.

The structure of this essay is as follows. All operating modes are given in Section 2, along with a discussion of the converter's component-sharing capabilities. Control loop is detailed in Section 3. Section 4 shows the simulation result from examinations of dynamics. Section 5 presents the experimental findings.

2. Operational principles of the proposed PITPCs

The proposed PITPCs is depicted in Figure 5 and encompasses three port PV, battery and load (V_{pv}, S_1, S_2, S_3, D_1 and V_{bat}). S_4 and C_1 operate for power conversions as mutual active clamp circuits for increase in voltage gains and isolating output ports only on transformers. L_k is the transformer's leakage inductance. D_2 and C_{out} produce a rectifier at the output. Additionally, RL is used to model loads.

The following provides an explanation of the operating principles of the proposed PITPCs in the DISO (Double-input-single-output), SISO (Single-input-single-output) and SIDO (Single-input-double-output) modes. In DISO mode, the main input and the battery port supply the load with the necessary power. When in SISO mode, the load receives power from the input port while the battery is inactive. The battery is charged while operating in SIDO mode and serves as an output. Figure 6 shows that The Flow Chart of proposed PITPCs topology.

(1) SISO modes of operations

Mode 0:

As seen in Figure 7(a), switch S_2 is turned on while switches S_{Aux}, S_3 and S_1 are off. Reverse bias exists in D_O output rectifiers. In "normal" flyback operations, magnetizing inductances are linearly charged when charging is on.

Mode 1:

Switch S_2 is switched off, as seen in Figure 7(a). The magnetizing currents are equivalent to the current flowing through resonant inductors, charges Cr. Due

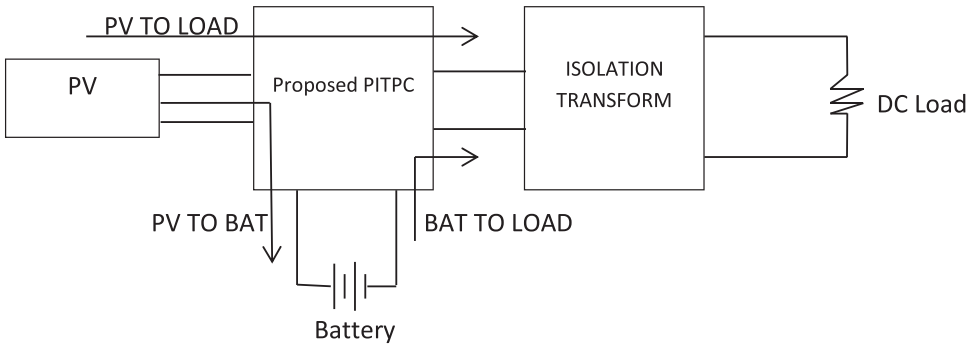


Figure 4. Block diagram of proposed partly-isolated three-port converter.

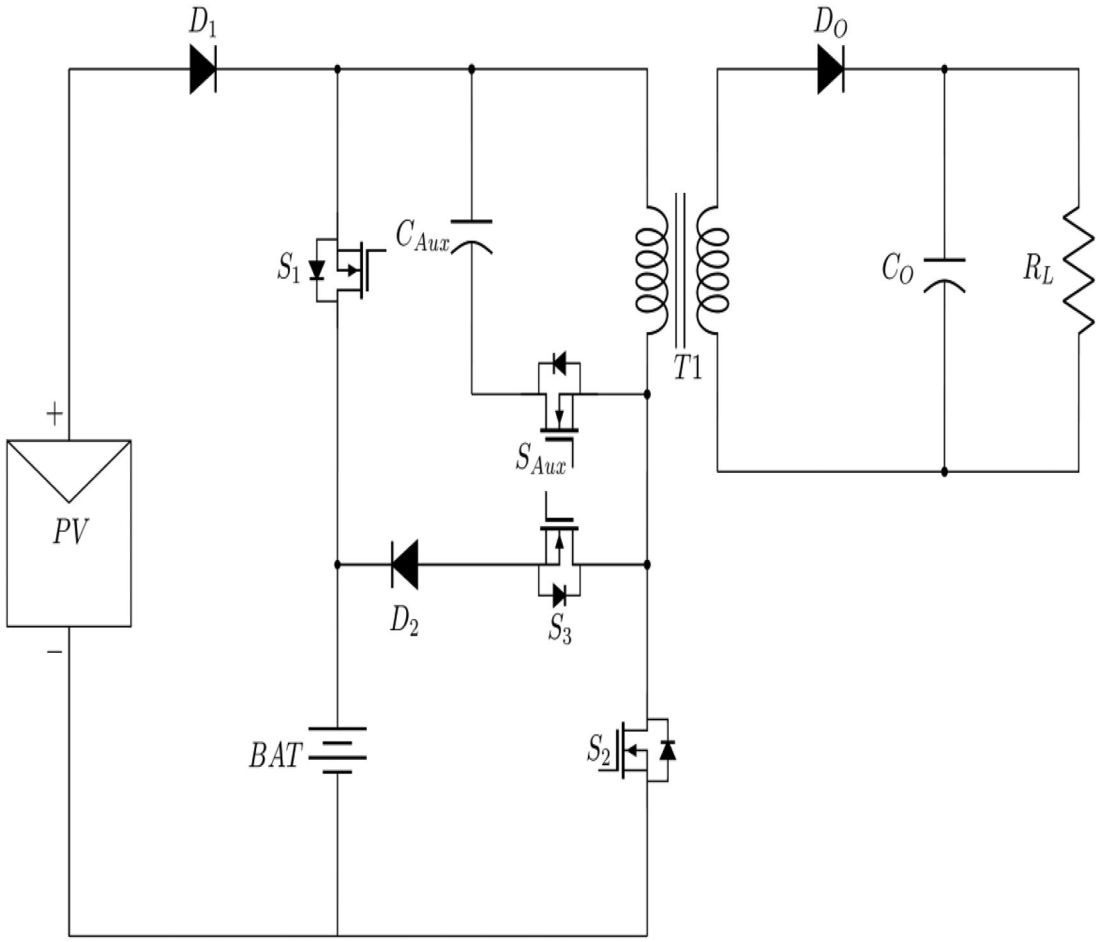


Figure 5. The proposed PITPCs topology.

to short charge times, charging behaviors are approximately linear.

Mode 2:

When the battery switch, S_1 and the auxiliary switch, S_{Aux}, are both off, as illustrated in Figure 7(a), Cr is charged to the point where the anti-parallel diode of S_{Aux} begins to conduct. In order to create a voltage divider between the two inductances, the clamp capacitor sets the voltage between the transformer's magnetizing inductance and the resonant inductor L_r to V_{CAux} (N^*V_O), where V_{CAux} is the clamp voltage, N is the turns ratio and V_O is the output voltage. Total magnetizing currents are routed through diodes to charge clamp capacitors since C_{Aux} is significantly greater than resonant capacitor Cr. As a result, according to the voltage divider action, the voltage visible across the magnetizing inductance, V_{pri}, lowers as V_{CAux} value grow, $V_{pri} = -V_C\left(\frac{L_m}{L_r} + L_m\right)$.

When S_2 is off and S_{Aux}, S_3 & S_1, are also off, Cr gets charged till auxiliary switch's anti-parallel diode starts conducting. Clamp capacitors define voltages across resonant inductors L_r and transformer magnetizing inductances to $V_{CAux}(\approx N^*V_O)$, forming voltage dividers between two inductances, where V_{CAux} represents clamp voltages, N implies turn ratios and V_O stands for output voltages.

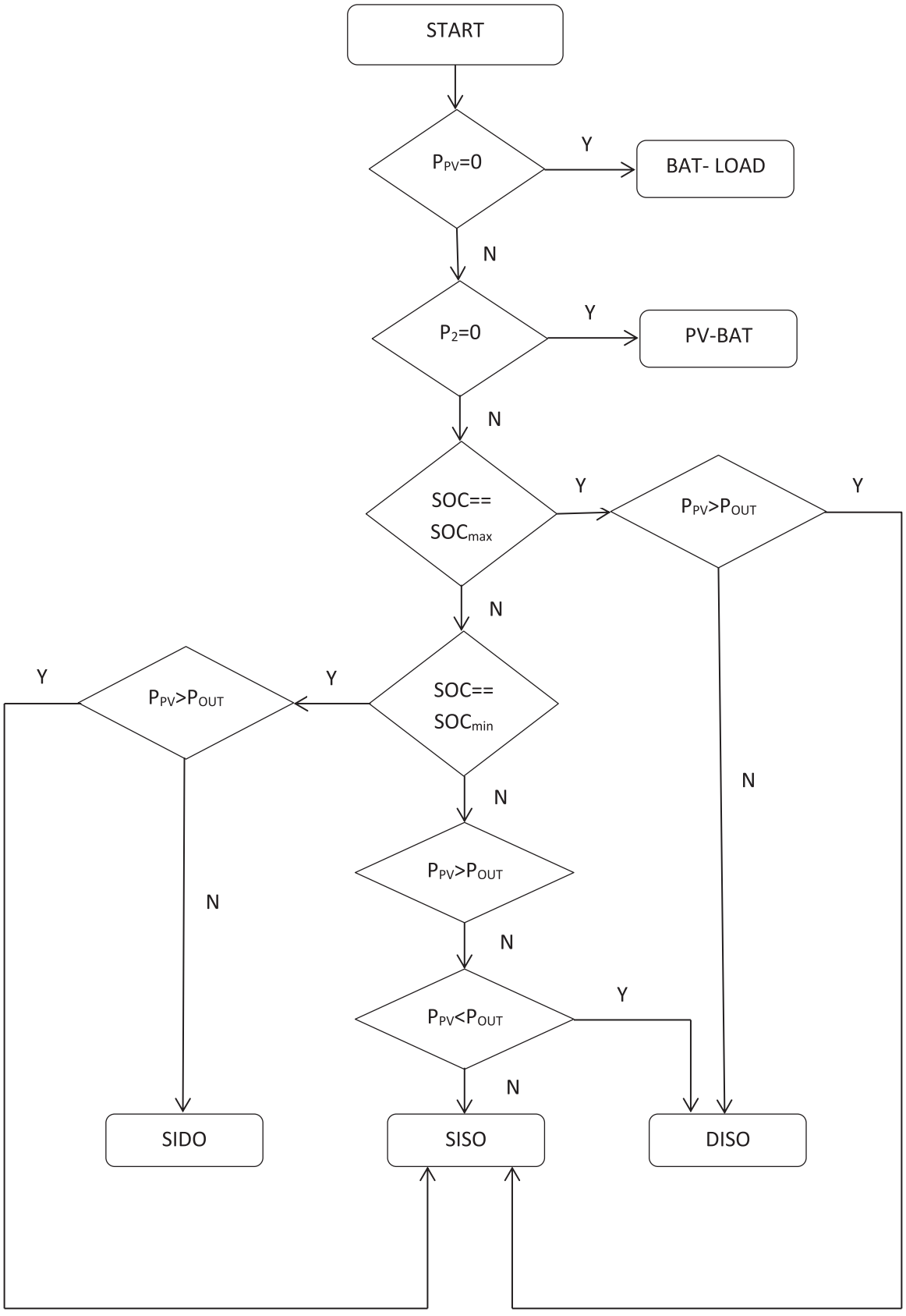


Figure 6. Flow chart of proposed PITPCs topology.

Mode 3:

Figure 7(b) illustrates how the primary voltage V_{pri} has fallen to a level where the secondary transformer voltage is adequate to forward bias D1. The output capacitance then clamps the transformer primary voltage to around N^*V_O, causing L_r and C_{Aux} begin to resonant. The device must be turned on before the clamp capacitor current I_{Aux} switches direction in order for S_{Aux} to reach ZVS.

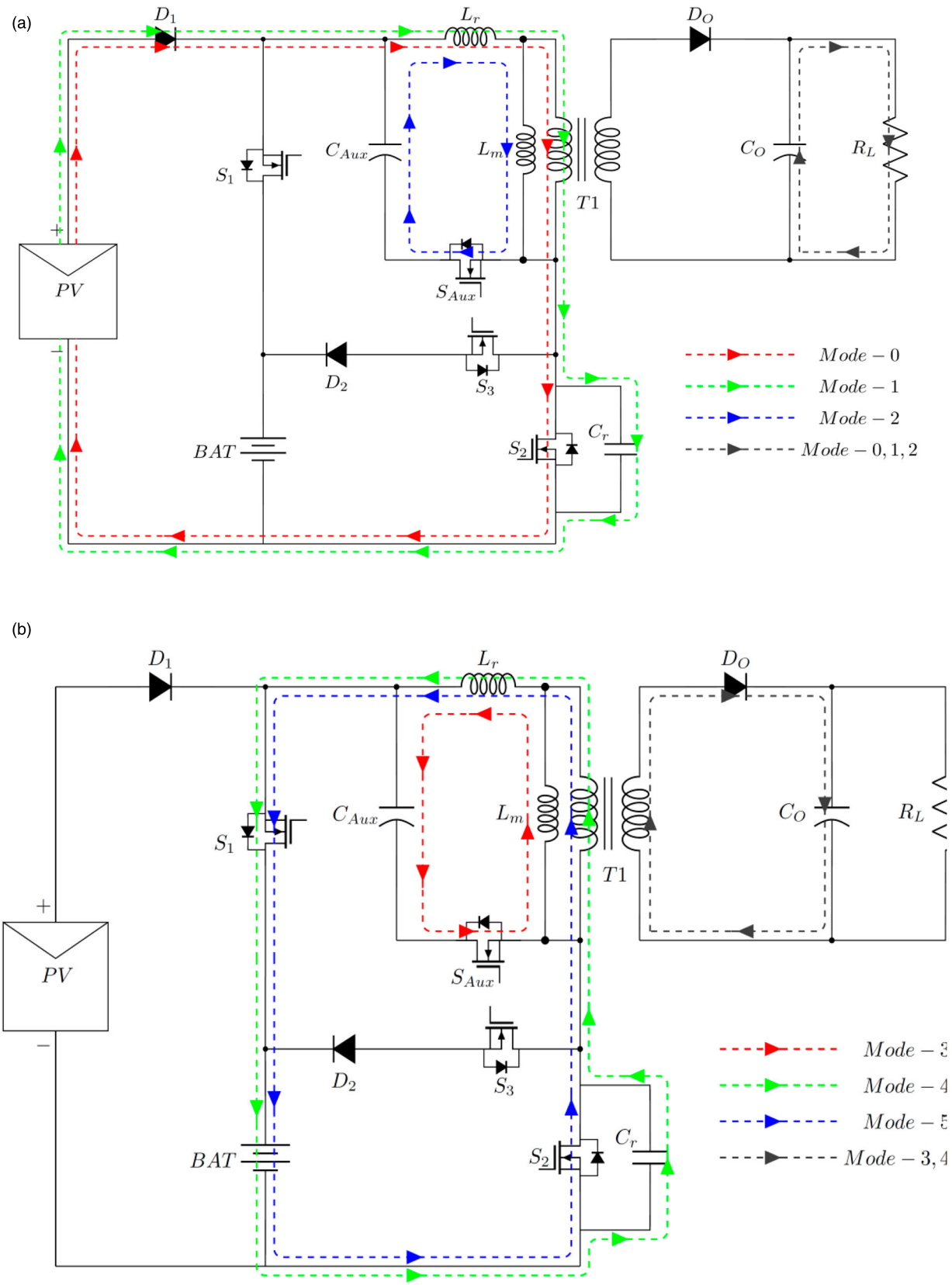


Figure 7. (a) Mode 0, Mode 1, Mode 2 of SISO. (b) Mode 3, Mode 4, Mode 5 of SISO.

Mode 4:

As seen in Figure 7(b), the auxiliary switch, S_{Aux}, is turned off, thus disconnecting C_{Aux} from the circuit. Between the MOSFET parasitic capacitances and the resonant inductor, a new resonant network is created. As C_r is depleted, the transformer primary voltage stays clamped at NV_O.

Mode 5:

As demonstrated in Figure 7(b), if L_r has more energy than C_r has, C_r will discharge to a sufficient

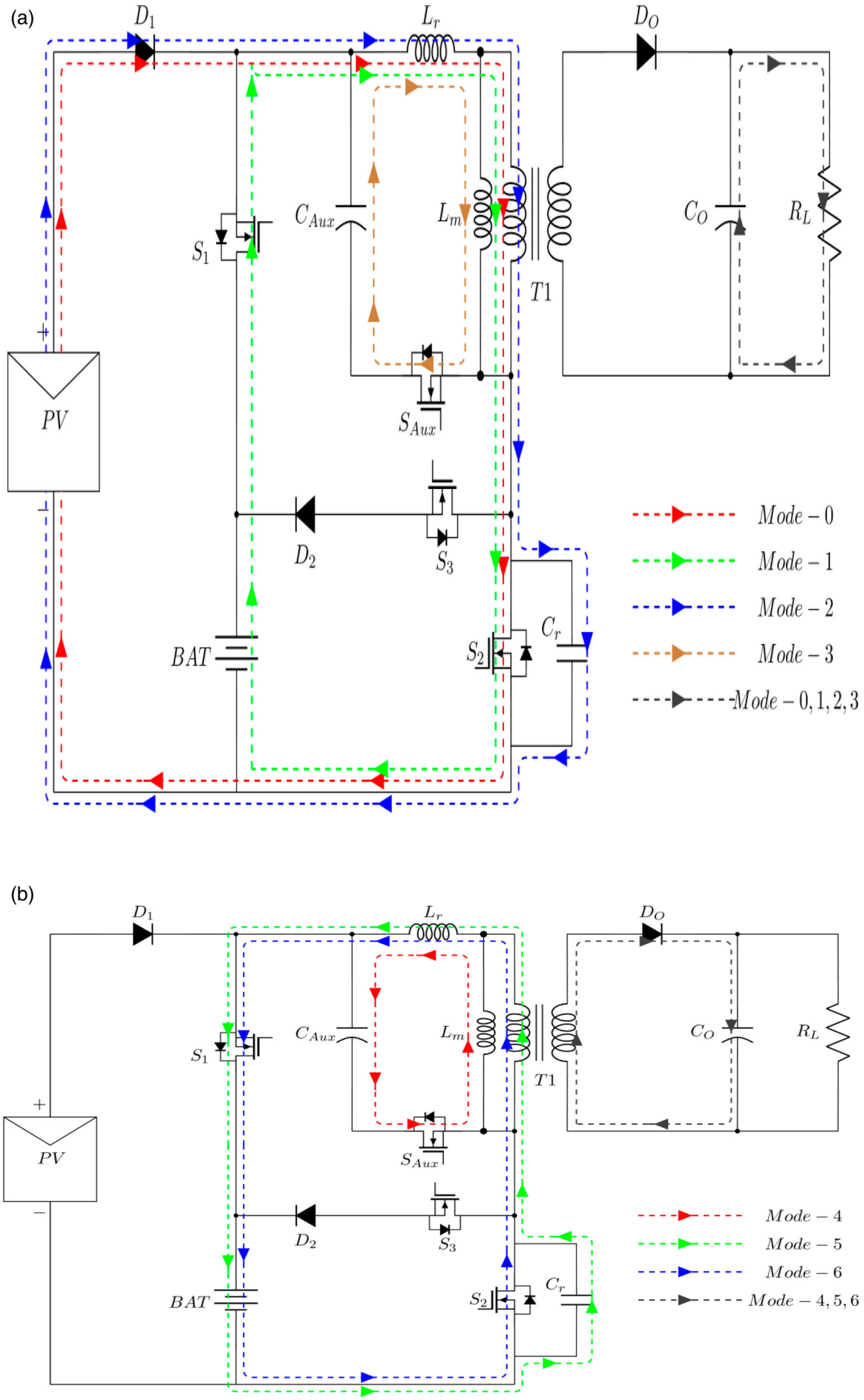


Figure 8. (a) Mode 0, Mode 1, Mode 2, Mode 3 of DISO. (b) Mode 4, Mode 5, Mode 6 of DISO.

degree to allow S_2's body diode to begin conducting. Voltages across resonant inductors get clamped at $V_{\text{Bat}} + NV_O$.

(2) DISO operational modes

Mode 0:

As shown in Figure 8(a) switch S_2 is put on while switches, S_{Aux}, S_3 & S_1, are put off. Output rectifiers, D_O, is biased reversely. In "normal" flyback operating mode, magnetizing inductances charge linearly from PV inputs.

Mode 1:

As seen in Figure 8(a). Switches, S_{Aux} and S_2, S_1 are off with reverse bias in D_O output rectifiers. In "normal" flyback operating modes, magnetizing inductance get charged linearly from battery inputs. Batteries are discharged in this mode as they have higher voltage potentials than PV potentials as soon as Switch S_1 is turned on.

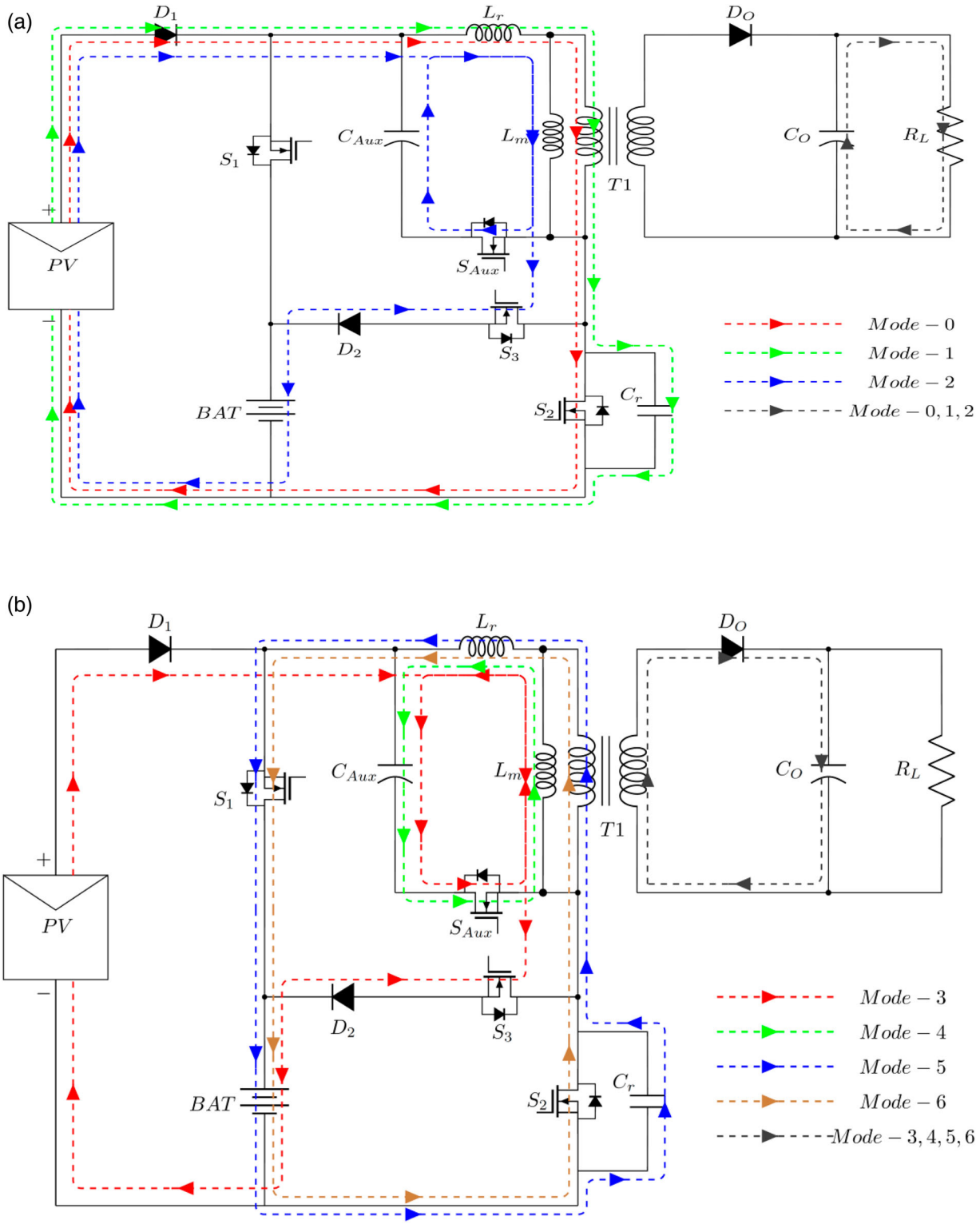


Figure 9. (a) Mode 0, Mode 1, Mode 2 of SIDO. (b) Mode 3, Mode 4, Mode 5, Mode 6 of SIDO.

Mode 2:

As shown in Figure 8(a). Switch S_2 is put off and Cr charged by magnetizing currents which are also equal to currents passing through resonant inductors. Charging times are brief resulting in approximately linear charge characteristics.

Mode 3:

As shown in Figure 8(a) switch S_2 is turned off and the auxiliary switch and battery switch, $S_{\text{Aux}}, S_3 \& S_1$, is also off,, Cr gets charged to points where anti-parallel diodes of S_{Aux} begin to conduct. In order to create voltage dividers between two inductances, clamp capacitors set voltages across resonant inductors L_r and the transformer magnetizing inductances to $V_{\text{CAux}}(\approx N^* V_O)$, where V_{CAux} represents clamp voltages, N refers to turn ratios and V_O stands for output voltages. Nearly all of the magnetizing currents are routed through diodes to charge clamp capacitors since C_{Aux} values are significantly greater than resonant capacitors Cr. This results in voltage divisions and visible voltages across magnetizing inductances, V_{pri}, decreases as V_{CAux} increases, $V_{\text{pri}} = -V_C \left(\frac{L_m}{L_r} + L_m\right)$.

Mode 4:

As shown in Figure 8(b), primary voltages V_{pri} get reduced to points where secondary transformer voltages are enough to forward biases D_1. Transformer primary voltages are then clamped by output capacitances to approximate to $N^* V_O$. L_r and C_{Aux} begin resonating and for S_{Aux} to achieve ZVS, devices need to be turned on before clamp capacitor currents I_{Aux} reverse directions.

Mode 5:

Auxiliary switch, S_{Aux}, is put off Figure 8(b) for eliminating C_{Aux} from the circuit effectively. New resonant networks are created between MOSFET parasitic capacitances and resonant inductors. As C_r values get depleted, transformer's primary voltages stay clamped at NV_O.

Mode 6:

Assuming energies stored in L_r are greater C_r energies as shown in Figure 8(b), C_r is discharged for conductance from S_2's body diode. Voltages across resonant inductors get clamped at $V_{\text{Bat}} + NV_O$.

(1) SIDO operational modes

Mode 0:

As displayed in Figure 9(a), switch S_2 is put on while switches S_{Aux}, S_3 & S_1, are in off state. Output rectifiers, D_O, are reversely biased and Magnetizing inductances get linearly charged in "normal" flyback operations.

Mode 1:

Switch S_2 is switched off, as seen in Figure 9(a). Magnetizing currents equivalent to the currents flowing through resonant inductors, charge Cr. Due to short charge times, charging behaviors are roughly linear.

Mode 2:

As shown in Figure 9(a) switch S_3 is turned ON and the auxiliary switch and battery switch, S_{Aux}, S_2 & S_1, is also off, Cr get charged till anti-parallel diodes of S_{Aux} begin to conduct. In order to create voltage dividers between two inductances, clamp capacitors set voltages across resonant inductors L_r and transformer magnetizing inductances to $V_{\text{CAux}}(\approx N^* V_O)$,, where V_{CAux} refers to clamp voltages, N implies turn ratios and V_O represents output voltages. Nearly all of the magnetizing currents are routed through diodes to charge clamp capacitors and batteries, since C_{Aux} and battery charges are significantly bigger than resonant capacitors Cr. This results in voltages V_{pri} across magnetizing inductances to drop as V_{CAux} rises, $V_{\text{pri}} = -(V_C + V\_\text{bat}) \left(\frac{L_m}{L_r} + L_m\right)$.

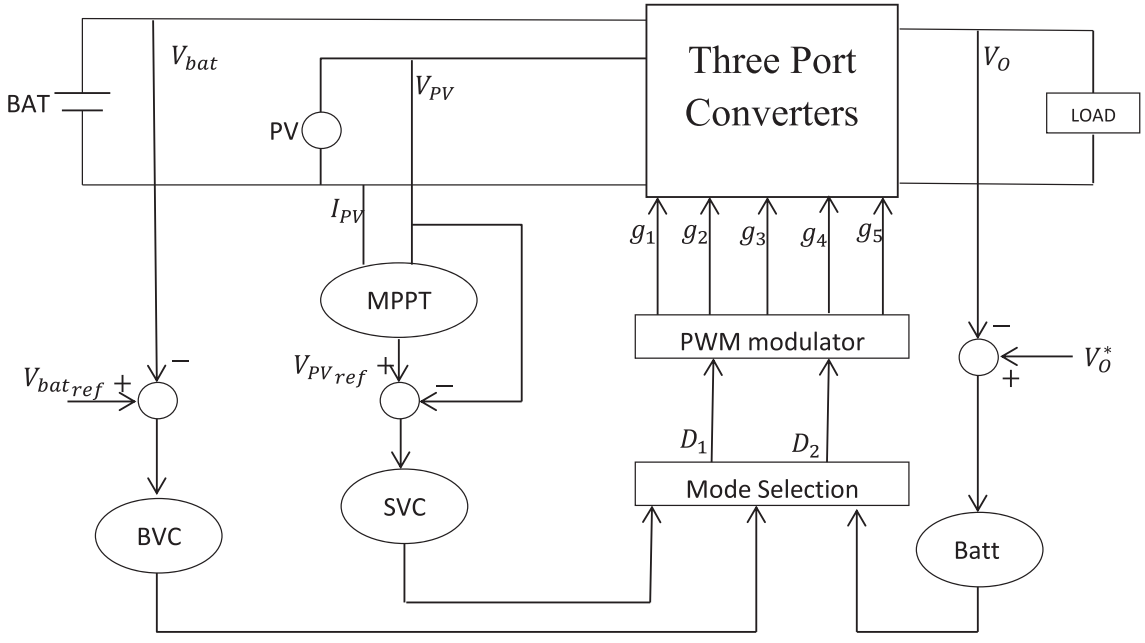


Figure 10. Control scheme of the proposed three-port converter.

Cr is charged until S_{Aux} anti-parallel diodes begin to conduct. In order to create voltage divisions between two inductances, (where), clamp capacitors fix voltages between transformer's magnetizing inductances and resonant inductors L_r. Nearly all of the magnetizing currents are routed through diodes to charge clamp capacitors and batteries as they are considerably larger than resonant capacitors Cr. This results in voltage divisions and visible voltage visible across magnetizing inductances, V_{pri} reduces when V_{CAux} values grow.

Table 1. Input-output specifications.

	Value
PV panel design specification	
Short circuit currents at reference conditions Isc	8.42 A
Open circuit voltages at reference conditions Voc	32.8 V
MPP voltages at reference conditions Vmp	25.25 V
MPP currents at reference conditions Imp	7.92 A
Irradiances at standard test conditions (STC)	1000 W/m^2
Cell temperatures at standard test conditions	25 _C
Maximum powers @ STC	200 W
No of parallel panels	2 No's
Battery specification	
Nominal voltage	36 V
Rated capacity	40 Ah
Cut-off voltage	27 V
Full charge voltage	41.9 V
Nominal discharging current	17.39 A

Mode 3:

As shown in Figure 9(b), switch S_3 is turned ON the diode D_2 is forward base. The secondary windings are connected to outputs, and main mutual inductances L_m are discharged to batteries and when batteries are charged, mutual inductors ($L_{m)}$ and PV systems work in tandem to operate as boost converters and accelerate the charging process.

Mode 4:

As shown in Figure 9(b), primary voltage V_{pri} has reduced to a point where secondary transformer voltages are enough to forward biases D1. Transformer's

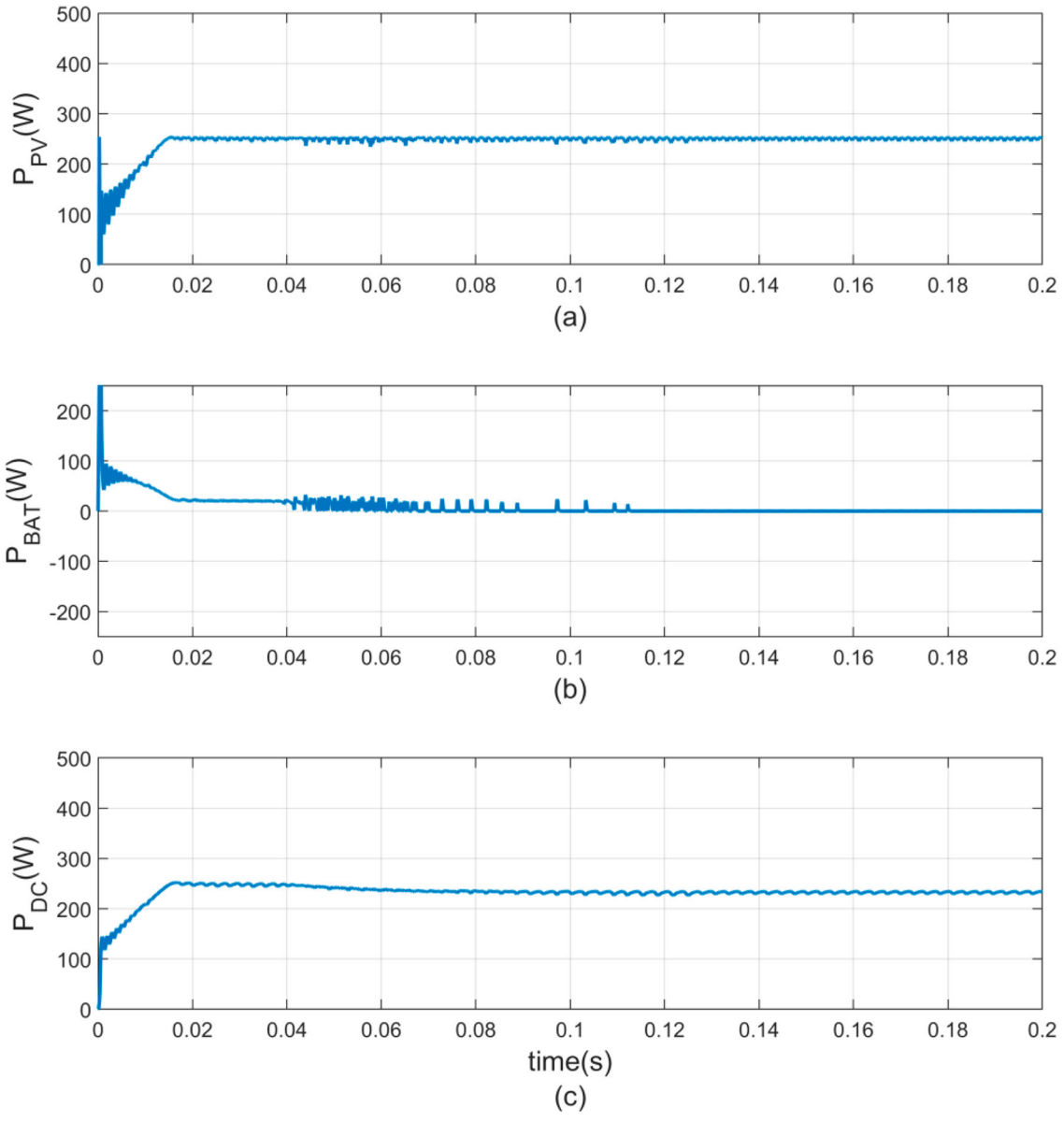


Figure 11. Power waveform of proposed PITPCs at SISO domain.

primary voltages are then clamped by output capacitances approximately to N^*V_O. L_r and C_{Aux} begins to resonate. For S_{Aux} to achieve ZVS, devices need to be turned on before clamp capacitor currents I_{Aux} reverse their directions.

Mode 5:

S_{Aux}, is turned off as shown in Figure 9(b) for eliminating C_{Aux}, effectively from circuits. New resonant networks are generated between resonant inductors and MOSFET parasitic capacitances. The transformer's primary voltages stay clamped at NV_O as C_r is being discharged.

Mode 6:

Assuming the energy stored in L_r is greater than the energy stored in C_r, as shown in Figure 9(b) C_r will be sufficiently discharged to allow S_2's body diode to start conducting. The voltage across the resonant inductor becomes clamped at $V_{\text{Bat}} + NV_O$.

3. Modeling and control strategy

As mentioned in Section II, the available solar power and battery charging states influence the converter's working modes. In order to manage the input and output port voltages, different state variables are required to operate the converter in each mode. The suggested converter has three control loops: OVC (output voltage controls), SVC (solar voltage controls) and BVC (battery voltage controls). Control system is displayed in Figure 10. OVC is a straightforward voltage regulation loop. For smooth mode transitions, both SVC and BVC loops use same control variables, d2. SVC is used to implement the MPPT algorithm and control the voltage of PV ports. The battery voltage regulation loops, or BVC, guards against overcharging. It should be noted that SVC is typically used to run the PV port. BVC would thus not be functional during typical operation. Between the SVC and BVC, only one control loop is

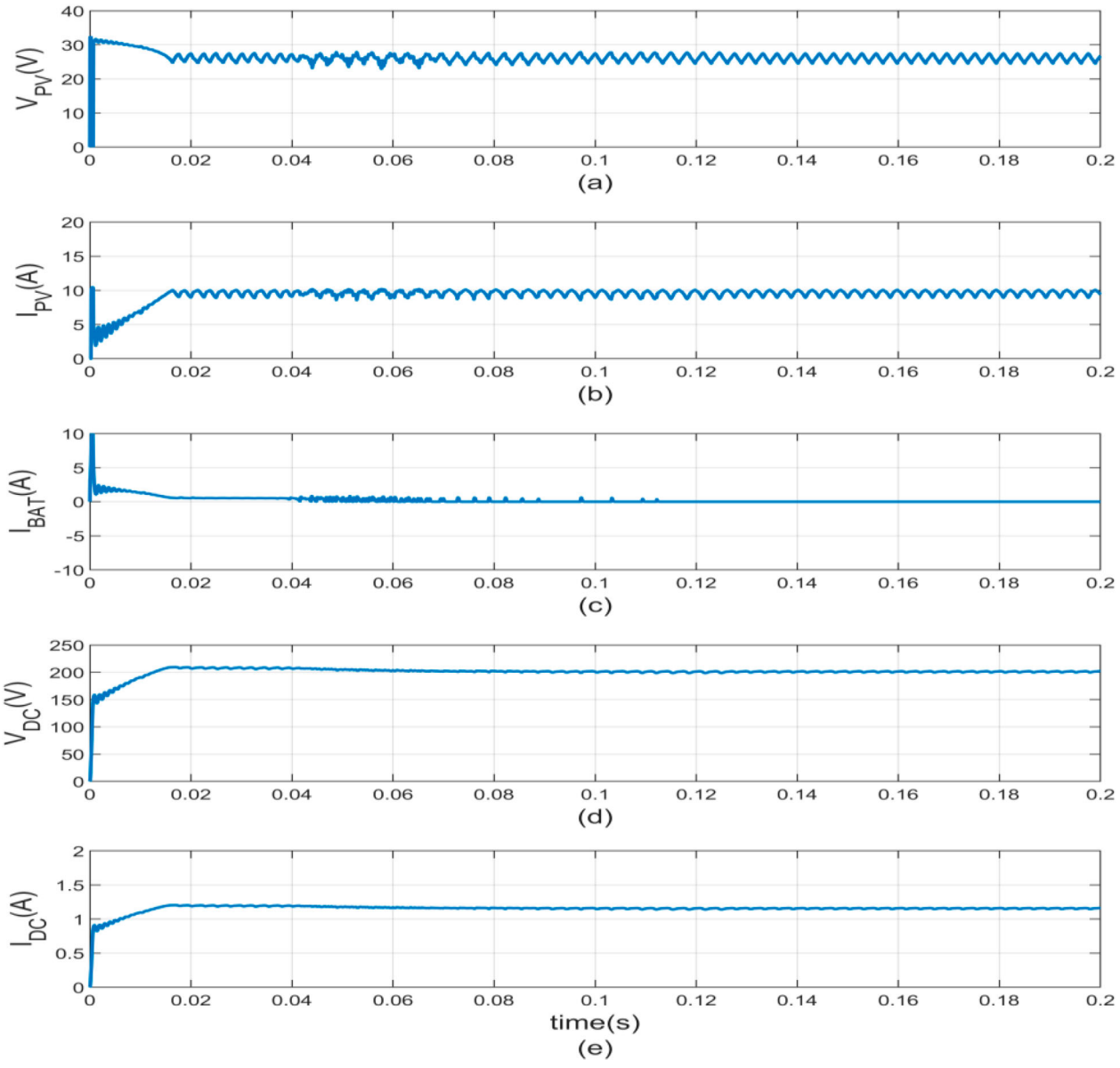


Figure 12. Input and output port waveform of proposed PITPCs at SISO domain.

executed. Additionally, SVC will be instantly turned off as BVC starts to take control of d2 in order to prevent the MPPT algorithm's noise problem. Cross-coupled control loops are a vital element of multiport converters since they are a high-order system. The controllers for a multiport converter will be tough to design. A decoupling network for extracting separate transfer functions in such a system has been described by simulating the system dynamics in a matrix format.

For power electronics converters, the small-signal modeling approach is frequently utilized. A matrix-form model will be highly beneficial to perform closed-loop control and analyse system dynamics for a three-port converter with two input ports. Two sets of small-signal models will be generated since the proposed three-port converter has two operational modes. While the control variables are the same across all models, the state variables vary slightly. To enable distinct controller design for each model, the decoupling network is necessary.

4. Simulation results

MATLAB/Simulink environments using simpower-system Toolbox were used in simulations for evaluating proposed PITPCs Converter performances. Table 1 shows specifications of converter inputs and outputs used in simulations.

(1) SISO domain simulation results

Assume at standard test condition the solar panel receives medium irradiation the solar generation power 232.5 W is sufficient to supply the load of 230 W and 2.5 W not sufficient to charge the battery; Figure 11. clearly shows the proposed converter functions in SISO. Thus the medium power extracted from the solar panel is clearly observed using PV Voltage, PV current, battery current and battery voltage domain distribution is shown in Figure 12. Figure 13 shows the Switch current for S2, PV current, battery current, primary fly back transformer current and clamping capacitor current

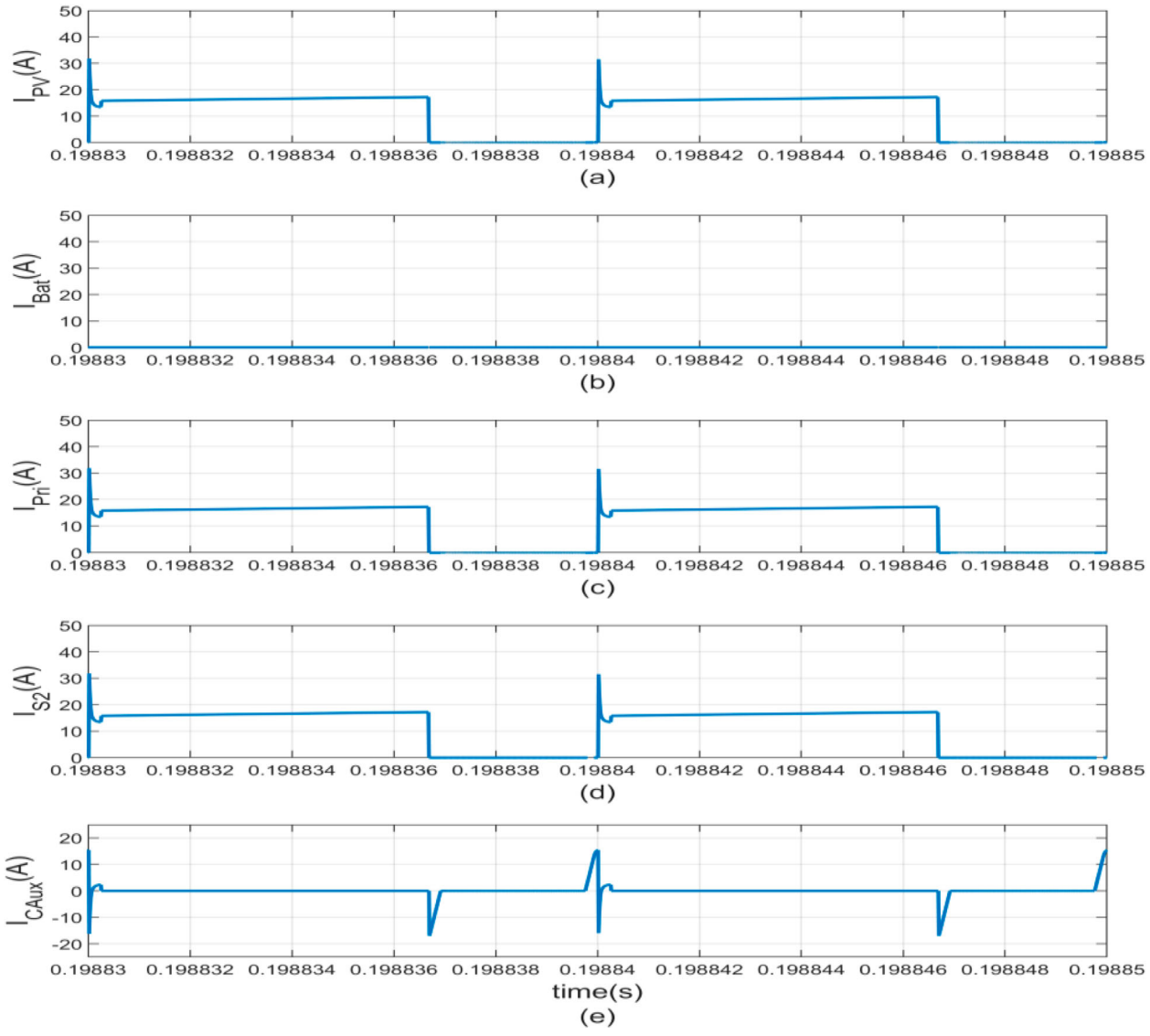


Figure 13. Switch mode waveform of proposed PITPCs at SISO domain.

which shows the proposed converter is operating at soft switching condition means that in this mode the only operated in this mode.

(2) DISO domain simulation results

Assume at standard test condition the solar panel receives low irradiation; The power produced from the PV is 150 W which is much lower than the load power of 230 W so the battery should supply the load demand of 80 W is clearly shown in Figure 14, Thus the low power extracted from the solar panel is clearly observed using PV Voltage, PV current, battery current and battery voltage domain distribution is shown in Figure 15. Figure 16 shows the Switch current for S2, PV current, battery current, primary fly back transformer current and clamping capacitor current.

(3) SIDO domain simulation results

Assuming at standard test condition the solar panel receives maximum irradiation, in Figure 17, the solar generating power of 383 W is adequate to provide the load at 230 W and charge the battery at 150 W vividly demonstrates the intended converter functionalities in Solar domains, the proposed TPC operates in SD, the corresponding PV voltage, PV current, Battery Current, control DC voltage of 200 V and DC current is shown in Figure 18. Thus the maximum power extracted from the solar panel is clearly observed. Figure 19 shows the Switch current for S2, PV current, battery current, primary fly back transformer current and clamping capacitor current.

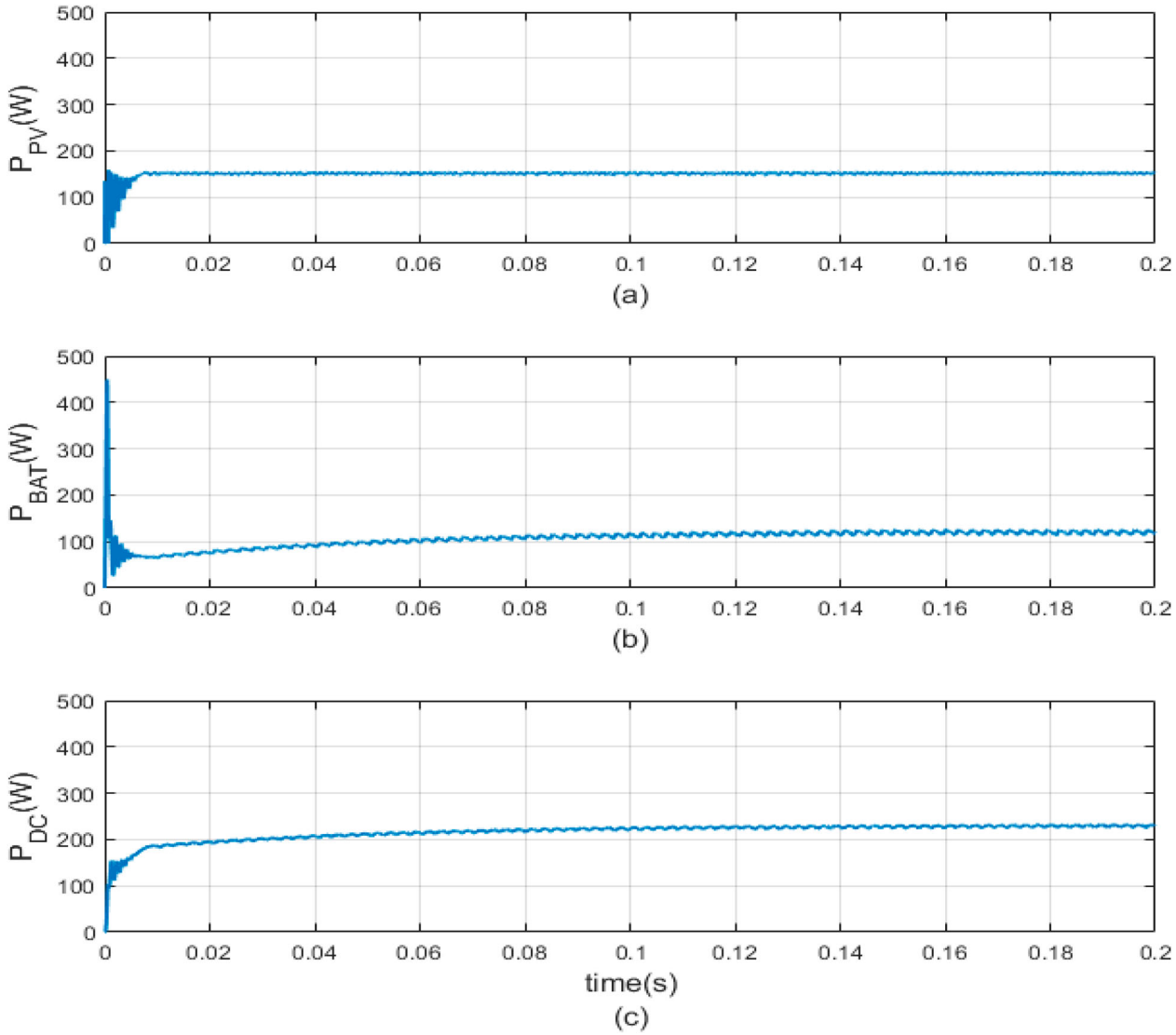


Figure 14. Power waveform of proposed PITPCs at DISO domain.

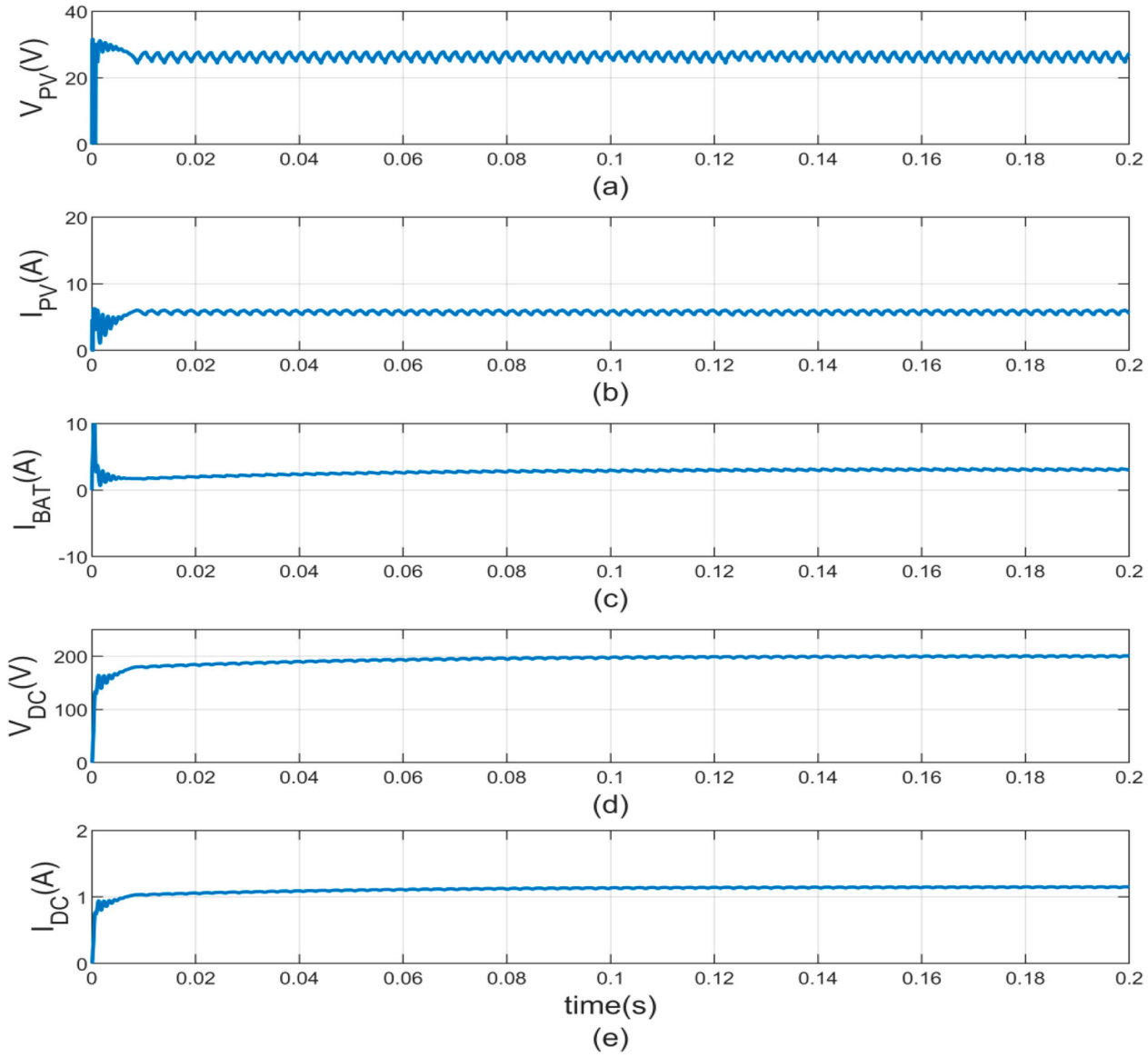


Figure 15. Input and output port waveform of proposed PITPCs at DISO domain.

5. Experimental verification

According to the domain distribution, high solar irradiation shows that the proposed converter operates in SIDO, low solar irradiation indicates that it operates in SISO, and night time (when there is little to no solar irradiation) implies that it operates in DISO. The converter in each of these three domains operates based on solar radiation; as a result, the load voltage and modes may be automatically modified in accordance with the power circumstances of each port. The outcomes of the respective experiments in these three areas are analysed in more detail below. Table 2 states that, Experimental specifications.

5.1. SIDO domains

The solar generation power is sufficient to supply the load and to charge the battery; Figure 20. Clearly shows the proposed converter functions in ESS Charging Domain. The PV delivers a power of 372.32 W the corresponding PV voltage is $V_{PV} = 18.4$ V, PV current is $I_{PV} = 20.23$ shown Figure 20(a). The load current and load voltage is maintained at 200.55 W, 200 V and 1.01 A. The remaining power of 159.9 W is efficiently stored in battery the corresponding battery voltage is $V_{BAT} = 12.12$ V, battery current is $I_{BAT} = -13.19$ A shown Figure 20(b).

5.2. SISO domains

Solar power generations are sufficient for loads, but insufficient to charge batteries; Figure 21. Clearly shows proposed converter functions of SISO. PV delivers a power of 238.68 W with corresponding PV voltages as $V_{PV} = 18.1$ V and PV current of $I_{PV} = 13.18$ as shown Figure 21(a). 200.55 W, 200 V and 1.01 A are the constant load current and voltage. The battery effectively stores the remaining 34.1 W of power; the appropriate

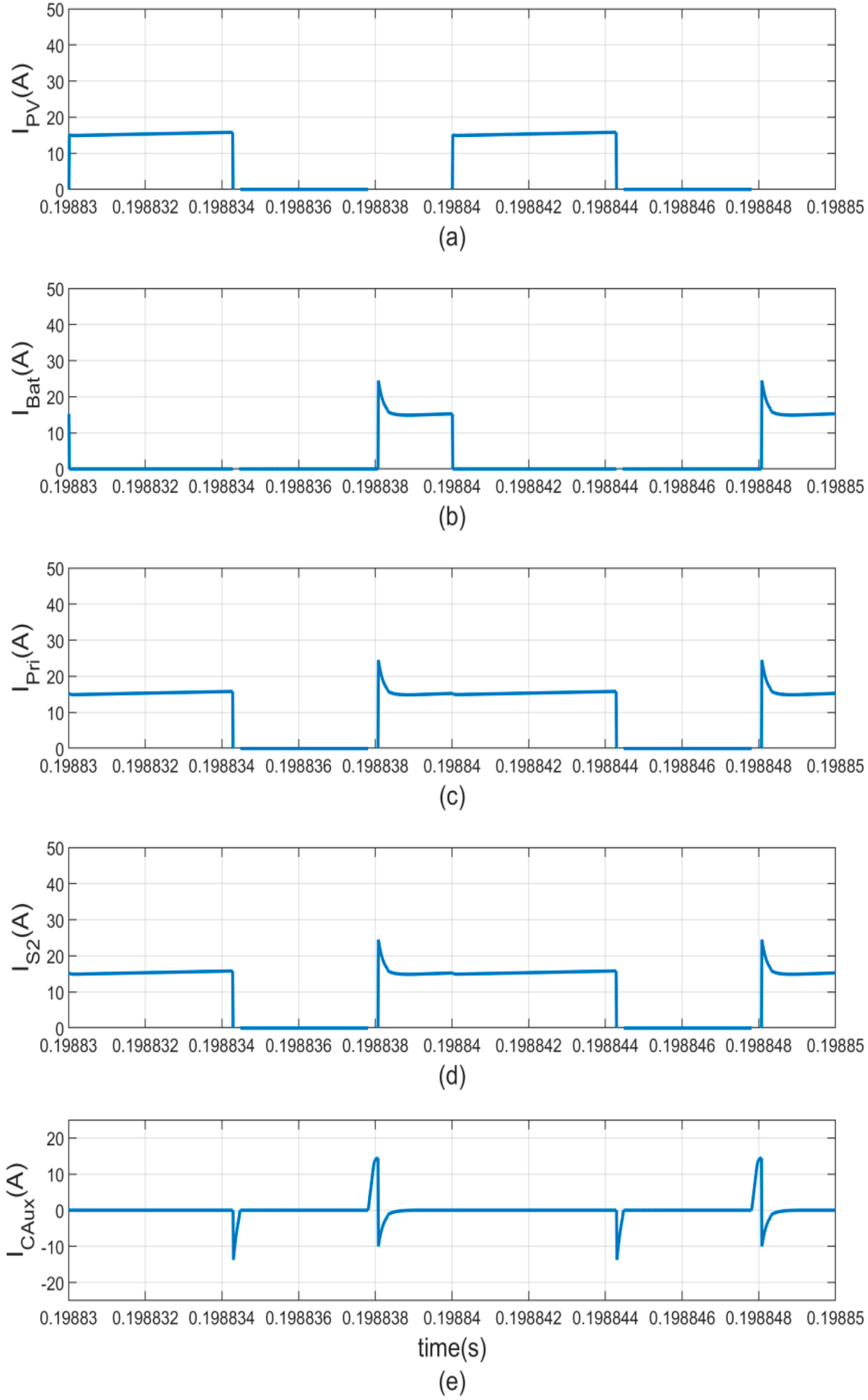


Figure 16. Switch mode waveform of proposed PITPCs at DISO domain.

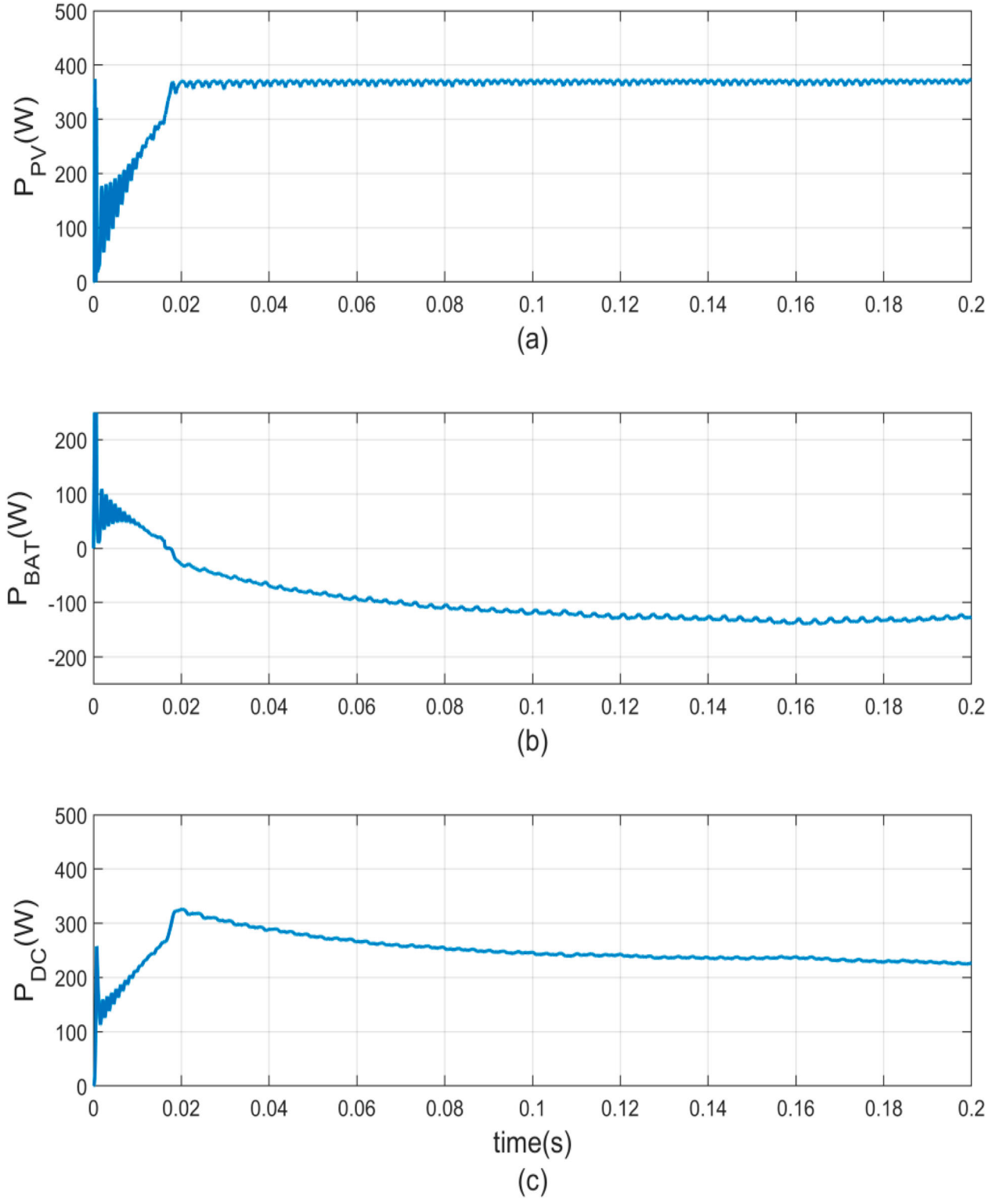


Figure 17. Power waveform of proposed PITPCs at SIDO domain.

battery voltage is $V_{BAT} = 12.08$ V, battery current is $I_{BAT} = -2.89$ A shown Figure 21(b).

5.3. DISO domains

The power from solar is not sufficient to support load demand, so battery should supply the load power demand; Figure 22. Clearly shows the proposed converter functions in DISO Domain. The PV delivers a power of 20.698 W the corresponding PV voltage is $V_{PV} = 17.56$ V, PV current is $I_{PV} = 1.17$ A shown Figure 22(a). The load current and load voltage is maintained at 200.55 W, 200 V and 1.01 A. The remaining power of 188.7 W is efficiently discharge from battery the corresponding battery voltage is $V_{BAT} = 11.8$ V, battery current is $I_{BAT} = 15.99$ A shown Figure 22(b).

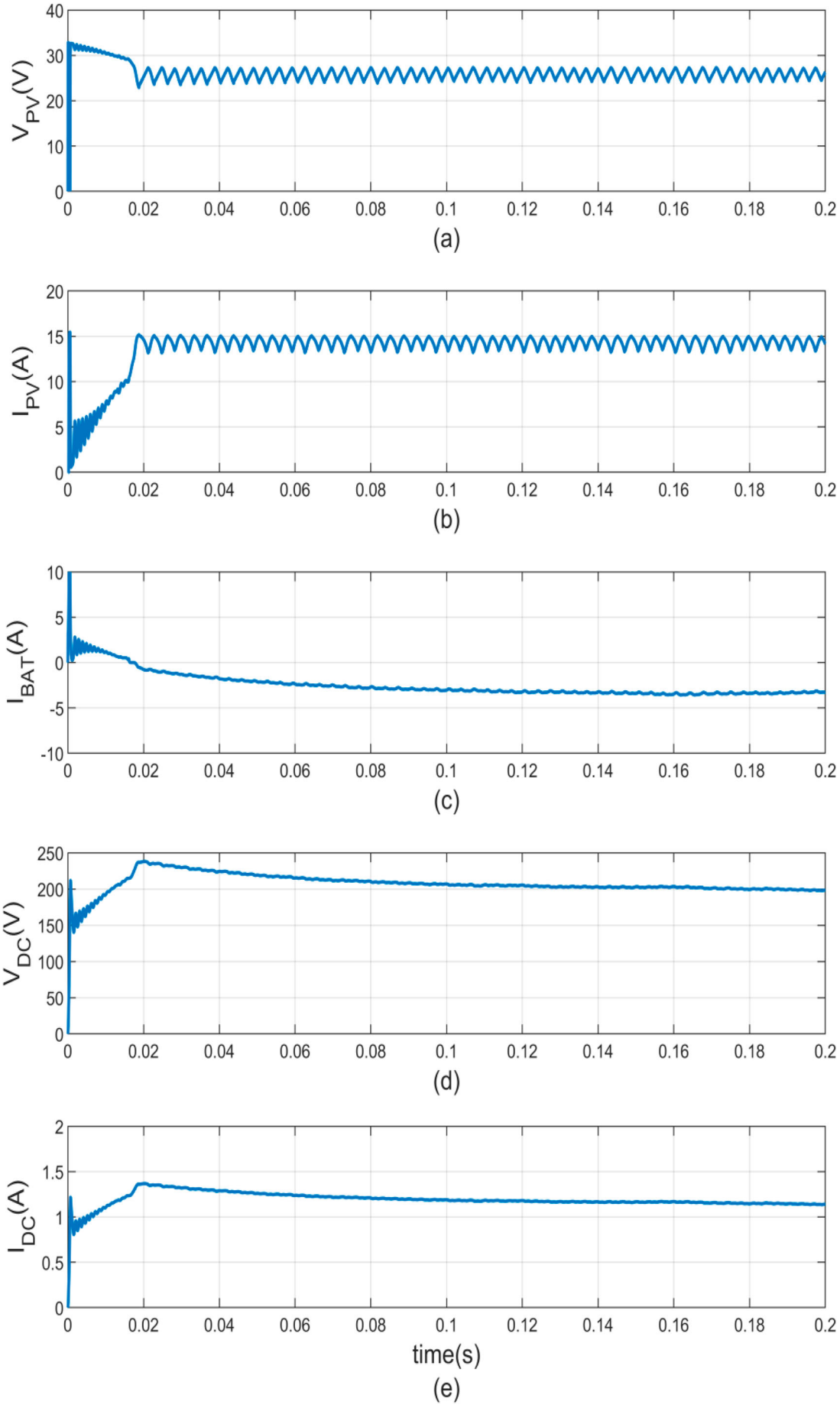


Figure 18. Input and output port waveform of proposed PITPCs at SIDO domain.

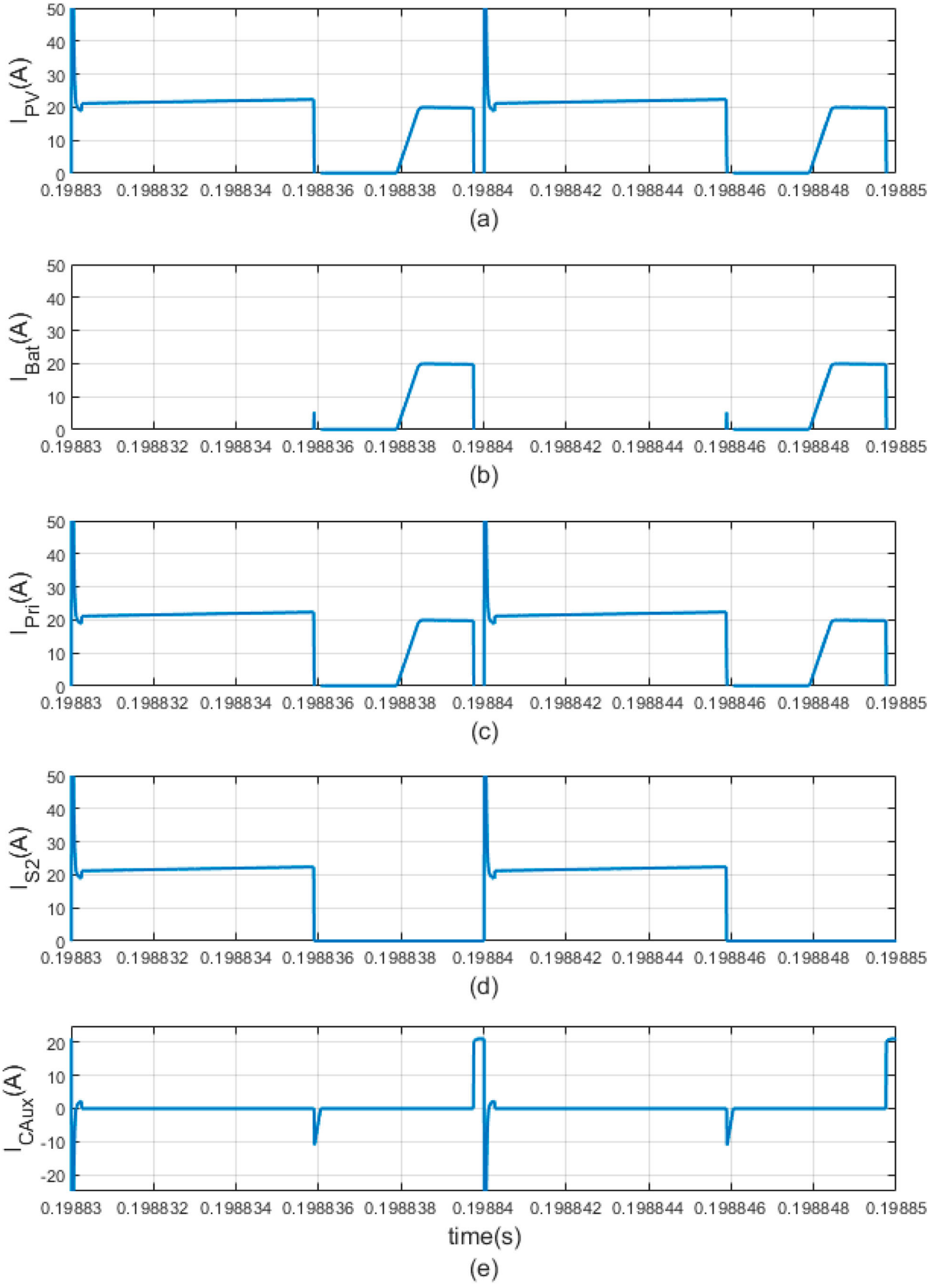


Figure 19. Switch mode waveform of proposed PITPCs at SIDO domain.

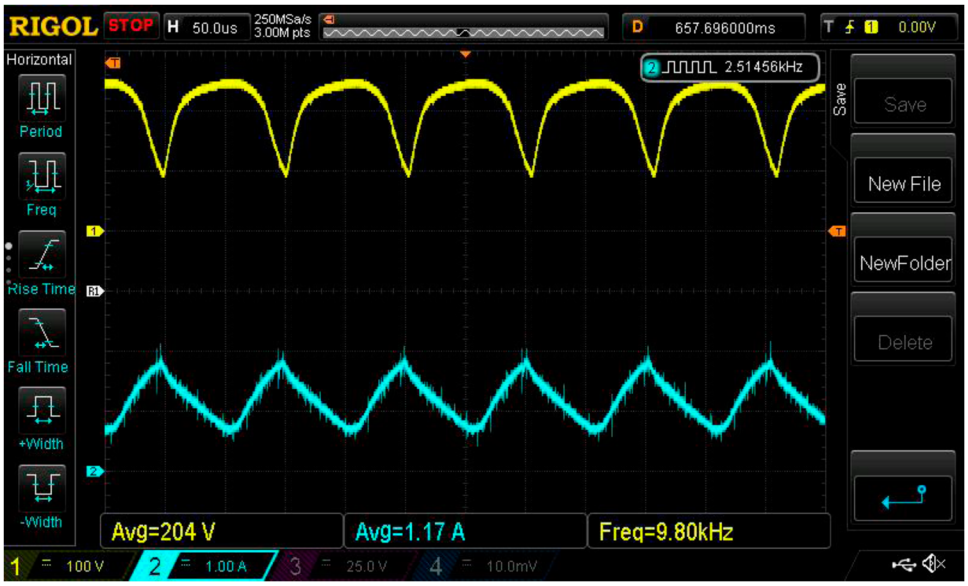
Table 2. Experimental specifications.

Parameters	Values
180 W PV panel design specification	
Short circuit currents at referenced conditions Isc	6.1 A
Open circuit voltages at referenced conditions Voc	23.32 V
MPP voltages at referenced conditions Vmp	18 V
MPP currents at referenced conditions Imp	5.56 A
Irradiances at standard test conditions (STC)	1000 W/m^2
Cell temperatures at standard test conditions	25 _C
Maximum power @ STC	100 W
Input-output specification	
No. of series panel	4 No's
Input power (10 180 W panel connected in series configuration)	400 W
Load power	200 W
Load voltage	100 V
Battery specification	
Rated voltage	12 V
Rated current	14 Ah'

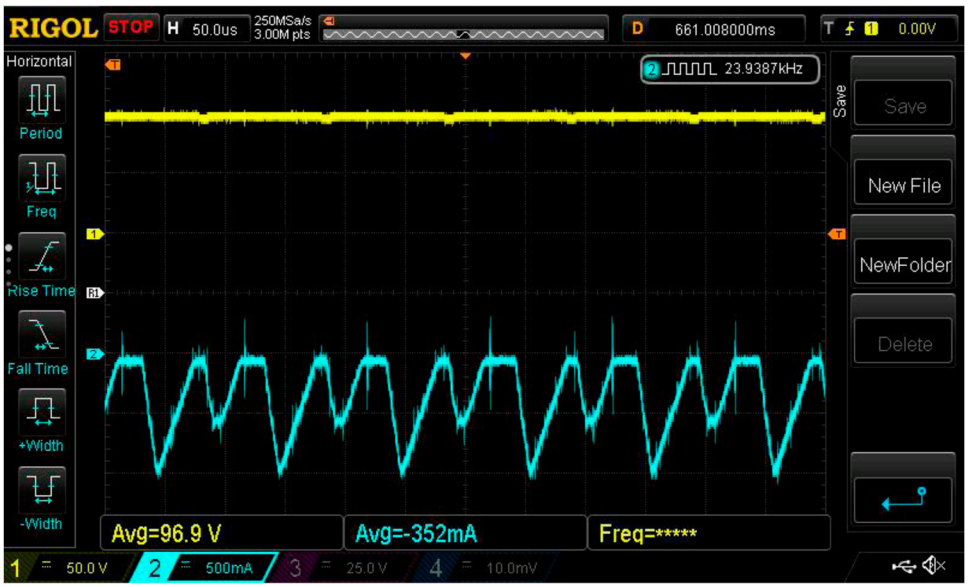
(a)

(b)

Figure 20. Experimental wave form of PV and battery in SIDO domain.



(a)



(b)

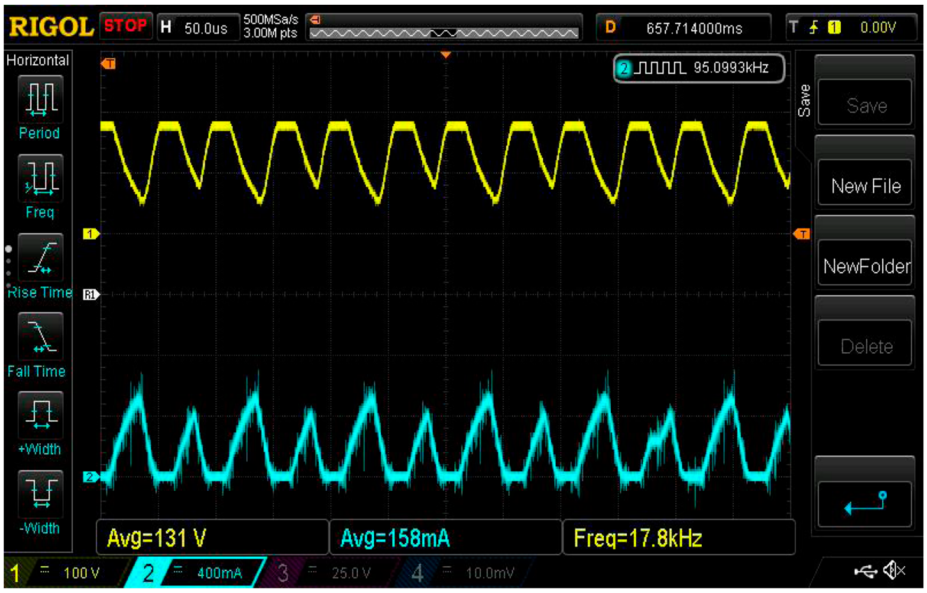
Figure 21. Experimental wave form of PV and Battery in SISO domain.

6. Conclusion

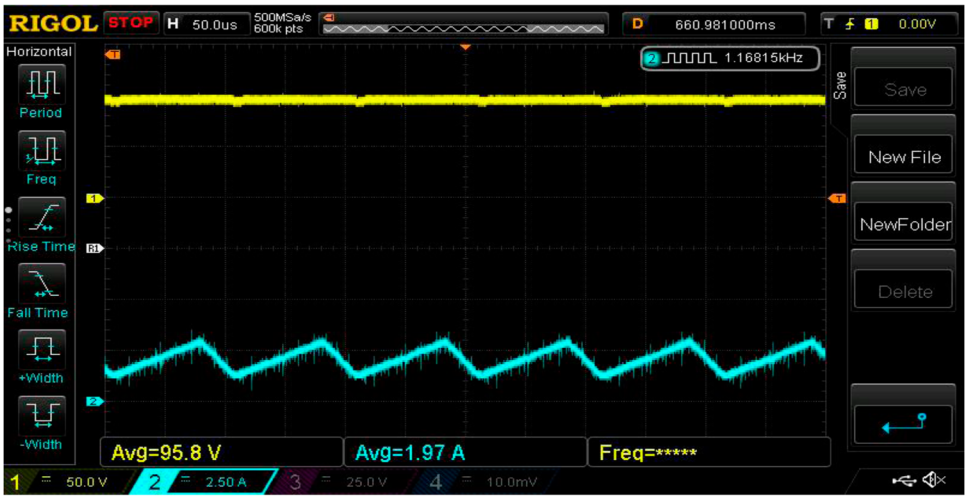
In order to utilize the three port converters more efficiently in hybrid energy systems, three possible power flow modes for proposed PITPC, including SIDO, DISO and SISO, are illustrated. The proposed PITPC has utilized one transformer for isolated DC bus and battery (bidirectional port) power flow. Consequently, reduces the cost and size of the converter. The leakage inductances of the transformers are exploited to make the semiconductors operate with soft switching. The semiconductors soft switching are preserved in all modes, which has led the converter to have good efficiency. Simulation results demonstrate precise MPPT and tight load voltage regulation for all three power flow is verified in proposed integrated PV-battery system. Moreover, experimental results are presented to validate the analyses of the proposed PITPC-based integrated PV-battery system under different modes during battery charging and discharging operations. Furthermore, capabilities of the proposed system to keep the load voltage under different disturbances are exhibited. The experimental of proposed PITPC verifies the SIDO efficiency is 96.8%, SISO efficiency is 98.3% and DISO efficiency is 95.7%.

Disclosure statement

No potential conflict of interest was reported by the author(s).



(a)



(b)

Figure 22. Experimental wave form of PV and battery in ESS discharging domain.

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