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Original scientific paper

IoT based Performance Improvement of Single Instruction Multiple Data (SIMD) Processor Array for Wireless Sensor Networks Application

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Abstract: The advent of the Internet of Things (IoT) has brought about the need for more sophisticated and low-cost resource devices compared to traditional embedded systems. These IoT devices, which are often deployed in wireless sensor networks, must operate within strict power constraints. To meet these requirements and to harness the potential of IoT, power consumption planning strategies have evolved, necessitating the integration of new capabilities, including machine learning. In this research, the focus is on migrating machine learning applications onto Field Programmable Gate Arrays (FPGAs) for IoT edge devices, specifically targeting wireless sensor network applications. FPGAs offer flexibility and parallel processing capabilities, making them well-suited for IoT applications where machine learning is increasingly important. A critical component in this work is the development of a Single Instruction Multiple Data (SIMD) processor array, optimized for FPGA implementation. SIMD architectures allow for parallel processing of data, which is essential for efficient machine learning tasks. The research also includes the design and implementation of a multiplier-accumulator (MAC) unit within the SIMD processor array, and an innovative approach is employed using the Dual Field Vedic multiplier. Notably, the researchers opt for the Vedic multiplier design over traditional Booth's method due to its advantages in terms of reducing latency and hardware complexity. The Vedic multiplier, which draws inspiration from ancient Indian mathematics, offers potential performance gains in this context. The research methodology involves creating a high-performance SIMD processor array using FPGA technology and programming it using the Verilog hardware description language. Through FPGA experimentation and analysis, the researchers gather data on various performance metrics. These include area overhead, time delay details, and power consumption parameters.The primary goal of this research is to demonstrate the advantages of the Vedic multiplier in the context of the SIMD system, highlighting its potential to enhance the efficiency and effectiveness of machine learning applications on FPGA-based IoT edge devices. By comparing the results obtained with the Vedic multiplier to those of conventional dual-field multipliers, the research aims to provide valuable insights into the feasibility and benefits of this approach for wireless sensor networks and other IoT applications.

Keywords: dual field vedic multiplier; field programmable gate array multiplier-accumulator; internet of things; single instruction multiple date

1 INTRODUCTION

The Internet of Things (IoT) represents a paradigm where connected devices are harnessed to enhance consumers' quality of life by leveraging the data generated by these devices. The proliferation of IoT devices has been on a steady rise. In 2018, there were already an estimated 7 billion IoT devices, and this number is projected to surge to approximately 21.5 billion by 2025. IoT serves as a prime example of how cloud computing capabilities have been deployed in data centers to manage the data generated by these devices. However, challenges arise due to network inactivity and the limitations of cloud-based processing capacity, leading researchers to advocate for a paradigm shift. This shift involves embracing the concept of "fog computing," which leverages devices closer to the data source for local data processing. This alteration in data processing approaches necessitates a transformation in machine learning algorithms. Embedded machine learning plays a pivotal role in enabling IoT end-devices, often constrained by limited resources, to acquire the capability to learn and adapt. Even basic machine learning algorithms, which are designed to be resource-efficient in terms of memory and power consumption, present challenges when applied to embedded systems. These algorithms can serve a multitude of purposes, including the detection of anomalous network activity and the identification of IoT botnets, among other applications. Many IoT devices interact with both other devices and humans, particularly in scenarios where quick actions are imperative. Therefore, reducing response latency and power consumption overhead in IoT end-devices is a priority. To address this issue, this paper recommends the incorporation of a reconfigurable Multiply-Accumulate (MAC) unit in Single Instruction Multiple Data (SIMD) processors. The MAC unit in the SIMD processor is meticulously designed using a Dual Field Vedic Multiplier, which contributes to the efficiency and performance of IoT devices, particularly in resource-constrained programmable scenarios, such as those found in medical applications. In energy-constrained IoT environments, FPGAs can be integrated with energy harvesting mechanisms to power IoT devices. This synergy between FPGAs and energy-efficient machine learning algorithms is crucial for long-term, autonomous IoT deployments. In recent years, the integration of machine learning applications into the Internet of Things (IoT) landscape has become a focal point of research and development. This integration is driven by the need to process and analyze data at the edge, closer to the data source, rather than relying solely on centralized cloud computing. Field Programmable Gate Arrays (FPGAs) have emerged as a key enabler for deploying machine learning models in IoT edge devices, particularly in wireless sensor network applications. FPGAs are semiconductor devices that can be programmed to perform specific tasks, making them highly adaptable for a wide range of applications.

2 LITERATURE REVIEW

In this section, let's discuss existing Multiply-Accumulate (MAC) units designed for real-valued and complex-valued operations. In real-valued operations, a single MAC unit is employed to carry out both multiplication and accumulation, requiring just a single instruction for execution [6, 7]. This results in an efficient and streamlined process. However, when it comes to complex-valued MAC operations, multiple instructions are often necessary, utilizing the same MAC unit for various steps in the computation. To address the challenges in complex-valued MAC operations, some Very Large Instruction Set Digital Signal Processor (VLIS-DSP) designs have been developed, which significantly improve the speed of complex-valued MAC operations [8-10]. These designs optimize performance by parallelizing the operations, effectively handling multiple genuine complex-valued MAC tasks with a single instruction. This approach capitalizes on data parallelism to boost overall execution efficiency. Nonetheless, complex-valued MAC operations in certain scenarios still require the execution of multiple consecutive instructions. In specific contexts, complex-valued MAC hardware can be designed to support both complex-valued and real-valued operations [11]. In such cases, a single instruction can efficiently process complex-valued MAC tasks. Some of these hardware designs have also been adapted for butterfly operations to accelerate Fast Fourier Transform (FFT) calculations [12]. In their research, the scientists have developed a Digital Signal Processor (DSP) that consists of an array of identical data paths [13]. Each of these data paths is equipped with its own MAC unit, which can be independently controlled. These MAC units typically operate with operands of 16-bit bit width. For single double-precision MAC operations, more than one cycle is typically required. Additionally, a DSP core with a dual MAC architecture is employed in certain applications, particularly in the calculation of digital filters [14-16]. This architecture involves one MAC unit receiving delayed input from another MAC unit, and both MAC units repeatedly process the word subdivisions. This architecture proves to be highly efficient for algorithms that involve multiple MAC operations with the same operands, thus saving on computational resources. Various studies have explored the utilization of reconfigurable computing for speeding up embedded applications, particularly in FPGA-based reconfigurable computing [17]. Due to its inherent parallelism, reconfiguration is commonly used in image processing and IoT hardware. In some research, dynamic reconfiguration with plugins and on-chip programmability for structured connectivity are discussed [18]. These approaches can significantly enhance the performance of IoT and video processing, especially when incorporating a general-purpose CPU and ISA extensions. Additionally, the studies have explored in-order and out-of-order processors with ISA extensions, yielding substantial reductions in total execution time [19, 20]. To overcome these limitations in Single Instruction Multiple Data (SIMD) processors, the researchers in this work propose the reconfiguration of the MAC unit using the Dual Field Vedic Multiplier. This innovative approach is aimed at enhancing the overall performance of SIMD processors in IoT and similar applications. Overall, the literature suggests that FPGAs hold significant promise for enhancing the capabilities of IoT edge devices, particularly in the context of machine learning applications. This integration offers the potential to transform various industries, from healthcare and smart cities to industrial automation and environmental monitoring, by enabling more intelligent and responsive IoT systems.

3 PROPOSED METHOD - VEDIC MULTIPLIER

In this research we aim to create a 16-bit multiplier by integrating a 2 × 2 multiplier, a 4 × 4 multiplier, an 8 × 8 multiplier, and a 16 × 16 Vedic Multiplier into the system. Each of these multipliers serves a specific function, as described below. Additionally, the utilization of two distinct fields, namely binary and prime fields, is essential for SIMD processors. The Urdhva-Tiryagbhyam Sutra is depicted as a 2 × 2 bit hardware representation in Fig. 1. This ancient mathematical concept, known as the "Urdhva-Tiryagbhyam Sutra" or the "Vertically and Crosswise Algorithm," has been effectively harnessed to develop a digital multiplier architecture in this context. This method efficiently handles the multiplication of two two-bit numbers, denoted as A and B, with values $a1a0$ and $b1b0$, respectively. The 2 × 2 Vedic multiplier module is constructed using four 2-input AND gates and two half adders. This module is a fundamental building block for the larger multipliers in the system, such as the 4 × 4 and 8 × 8 multipliers, which employ similar principles of adding and subtracting partial products.The utilization of these multipliers in the system allows for the efficient multiplication of 16-bit values, further extending the capabilities of the processor.

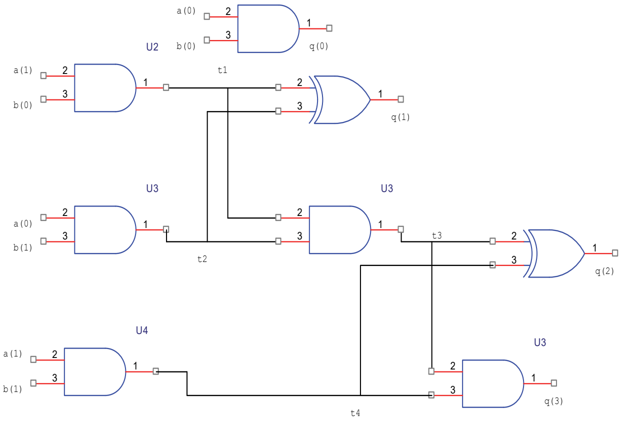

Figure 1 The architecture of the 2 × 2 Vedic multiplier

The development of a 4 × 4 Vedic multiplier is displayed in Fig. 2. This figure has four 2 × 2 multiplier and three adder. As an outcome, in this figure, $a0$ to $a3$ and $b0$ to $b3$ address a four-digit inputs. The Least Significant Bit (LSB) of the two data sources ($a0$, $a1$ and $b0$, $b1$) is at first passed to the contribution of the 2 × 2 multiplier to play out the multiply operation.

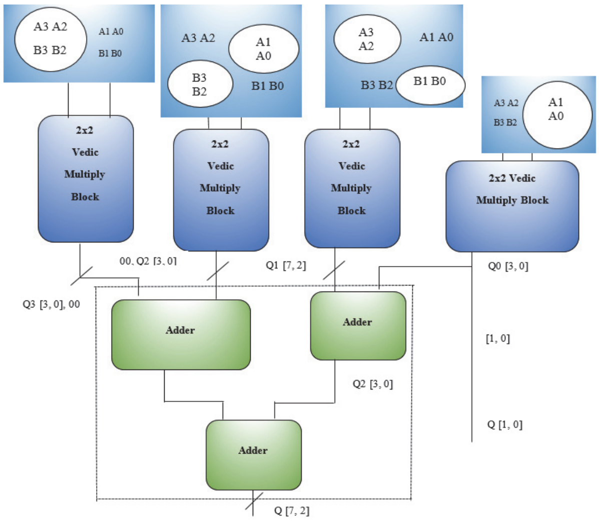

Figure 2 The architecture of the 4 × 4 Vedic multiplier

In the second step, the 2 × 2 multiplier operation is applied to $a2$, $a3$, and $b0$, $b1$ values, in the third stage, to $a0$, $a1$ and $b2$, $b3$ values, and in the fourth stage, to $a2$, $a3$, and $b2$, $b3$ values. The last two-stage multiplier's value was preserved in one adder, while the initial two-stage multiplier's value was saved in another. The outputs of the two adders are fed into the input of the final adder. Finally, 8-bit values are provided in the design's output.

Four 4 × 4 Vedic multipliers employing the UrdhvaTiryagbhyam sutra were used to create the 8-bit multiplier. An adder adds the output of these 4-bit Vedic multipliers. In this multiplier, one 8-bit adder and two 12-bit adders are used. Fig. 3 depicts the proposed 8 × 8 multiplier's block diagram.

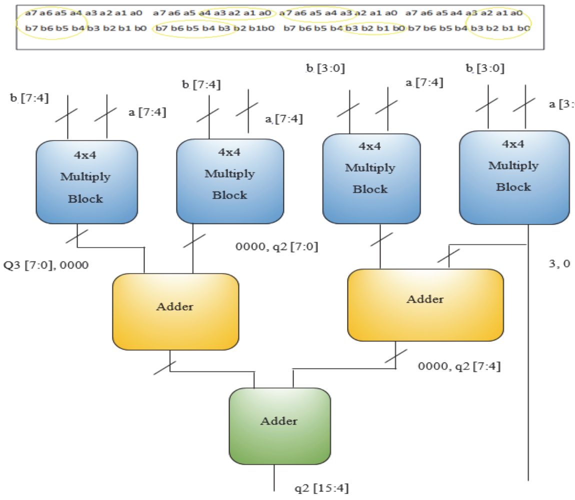

Figure 3 The architecture of 8 × 8 Vedic Multiplier

The 16 × 6 Vedic multiplier illustrated in Fig. 4 is built using the "UrdhvaTiryagbhyam" Sutra. Four 8 × 8 Vedic multiplier modules, one 16 bit binary parallel adder, and two 24 bit binary parallel adder stages make up the 16 × 6 Vedic multiplier design. To build the final 32-bit result (q_{31} - q_8) & ($q7$ - $q0$), the suggested architecture employs 16-bit and 24-bit Binary Parallel Adder modules. The $q7$ - $q0$ (8-bits) output of the right-hand most (4-th) 8 × 8 multiplier module represents the least significant 8-bits of the 16-bit output.

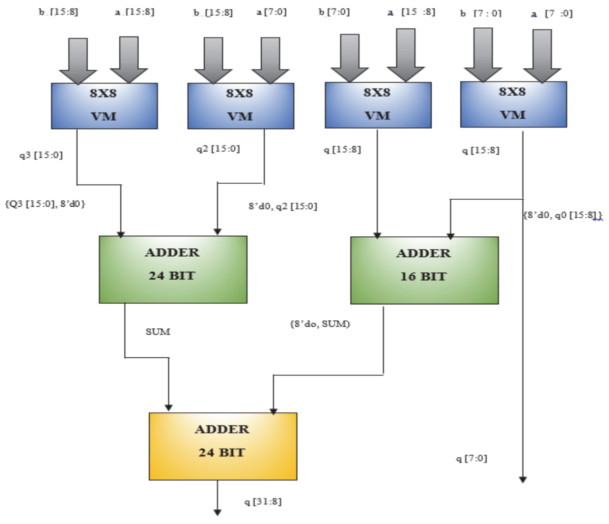

Figure 4 16 × 16 Vedic multiplier

The 16-bit Binary Parallel Adder takes two 16-bit inputs and adds them together (one of $q1$ and another of $q0$ concatenated with eight zeros in front). Then the multiplied output from 1-st ($q3$) and 2-nd ($q2$) 8 × 8 multiplier block is provided as input to 24-bit BPA (making concatenation of 0's as required). Then, the sum part extracted from a 16-bit & 24-bit BPA is provided as input to another 24-bit BPA, which provides the sum as $q31$ - $q8$ (24-bit). Finally, the carry bits are omitted while taking the final product. The suggested 32bit Vedic multiplier is depicted in Fig. 5 as a block diagram.

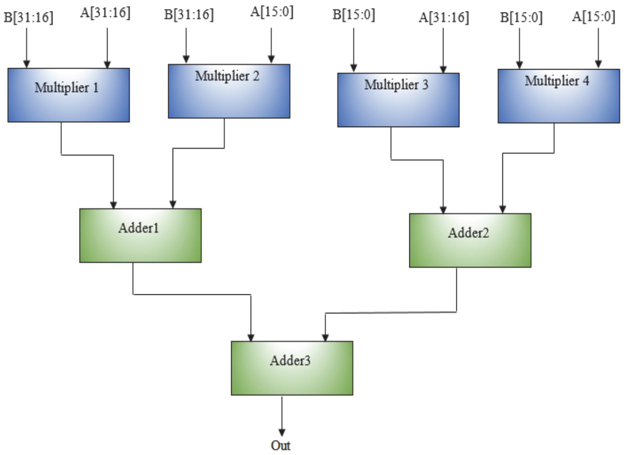

Figure 5 Block Diagram of 32 × 32 Vedic multiplier

Fig. 6 and 7 show the architecture of 32 bit and 48 bit adder.

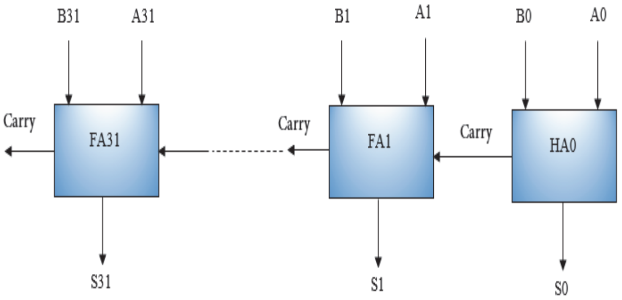

Figure 6 The architecture of 32-bit adder

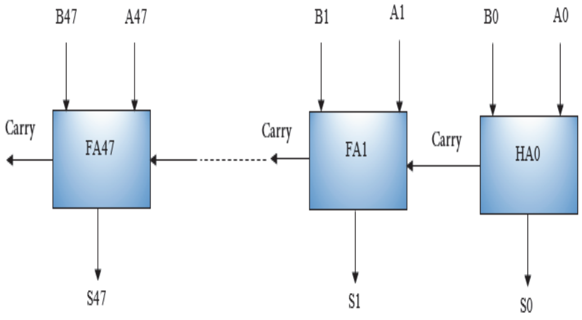

Figure 7 The architecture of 48-bit Adder

As evident from the line diagram, the Urdhva-tiryakbyham sutra effectively handles both the vertical and horizontal aspects. Consequently, a computation is performed based on the line graph depicted in Fig. 8.

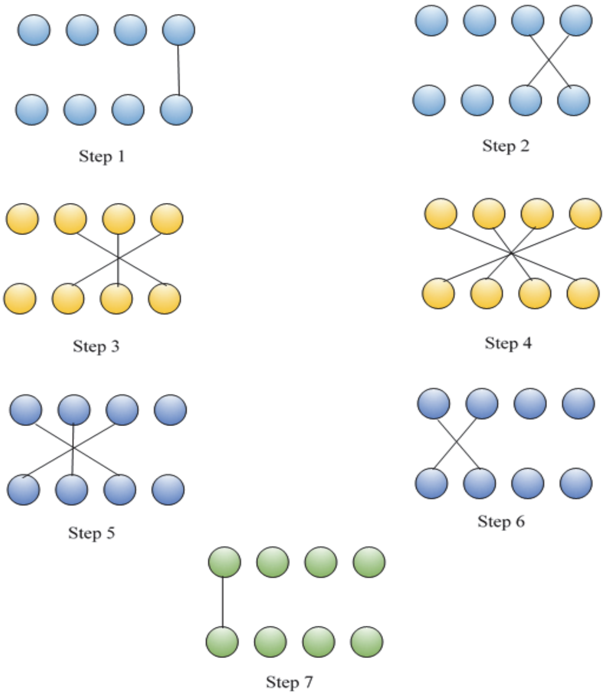

Figure 8 Line diagram Representation of Urdhva-tiryakbyham sutra

In this section, an example of the pin mentioned in above diagram is shown. Bitl = "l0ll" and Bit2 = "1101" are the two 4-bit values represented in the pin diagram.

4 RESULTS AND DISCUSSION

This section offers an in-depth analysis of the performance and simulation results of a SIMD processor, which is built upon a 32 × 32 Vedic multiplier architecture. The 32-bit Vedic multiplier was developed using Verilog and was subjected to simulation using the Xilinx ISE 14.7 software platform. The accompanying figures and tables present a comprehensive view of the simulation outcomes and performance assessments. Fig. 8 provides an RTL schematic diagram illustrating the structure of the proposed 32-bit Vedic Multiplier, featuring four 32 × 32 Vedic multipliers, two 48-bit adders, and one 32-bit adder.

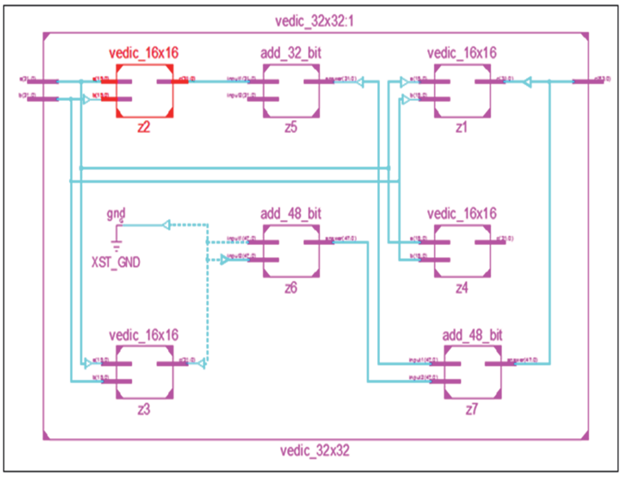

Figure 9 RTL Schematic Diagram for Vedic multiplier

Tab. 1 shows the percentage reduction in hardware area overhead, power consumption, and time delay for various approaches that lowered percentages of area, power, delay, APP, and ADP for recommended methodology.

Table 1 Reduction (%) for the different methods.

Techniques	Overhead Reduction / %	Power Reduction / %	Delay Reduction / %
DMM-OCLA	14.78	10.15	13.38
DMM-OCBA	19.41	11.43	19.50
DMM-LCSLA	34.72	41.60	27.25
DVM-LCSLA	42.77	71.09	28.61

Tab. 2 presents the performance comparison of different implementation devices for various methods to analyzing performance limitations.

Table 2 Performance analysis for various methods

Target FPGA	Circuit	LUT	Flip-flop	Slice	Number of DSP	Frequency / MHz
Virtex6 xc6vcx240t	DMM-CSA	119981/150720	85/109984	86/301440	768/768	20.42
	DMM-OCLA	98526/150720	88/109984	81/301440	736/768	25.55
	DMM-OCBA	90235/150720	78/109984	75/301440	699/768	25.62
	DMM-LCSLA	82256/150720	65/109984	70/301440	781/768	30.55
	DVM-LCSLA	79594/150720	58/73608	72/301440	656/768	39.64
Virtex7 xc7vx550t	DMM-CSA	98217/346400	73/99219	76/692800	3580/2880	37.64
	DMM-OCLA	95625/346400	69/99219	70/692800	3454/2880	20.21
	DMM-OCBA	88254/346400	65/99219	68/692800	3125/2880	26.15
	DMM-LCSLA	81546/346400	61/99219	63/692800	2968/2880	30.32
	DVM-LCSLA	77054/346400	50/692800	50/692800	2784/2880	38.22
Virtex7 xc7vx485t	DMM-CSA	98462/303600	45/99465	58/607200	3500/2800	34.66
	DMM-OCLA	95235/303600	54/99465	56/607200	3312/2800	25.12
	DMM-OCBA	91254/303600	56/99465	51/607200	3125/2800	28.65
	DMM-LCSLA	86325/303600	51/99465	50/607200	2935/2800	31.75
	DVM-LCSLA	84726/303600	45/99465	48/607200	2705/2800	38.42

DVM is a decent multiplier among those four multipliers, we have determined. Hardware Area overhead Reduction (42.77%), Power Reduction (71.09%), and time delay (28.61%) have been decreased in the proposed DVM-LCSLA technology. In that table, LUT, number of DSP, and Frequency have been analyzed for different target devices, namely Virtex 6 and Virtex 7. For FPGA analysis also, the DVM-LCSLA method gave better results than other multiplier techniques.This table shows that the DVM-LCSLA approach reduces the LUT, flip-flop, and slice sizes while increasing the operating frequency. The area in SIMD architecture has been minimized as a result of the reduction of certain parameters.

5 CONCLUSION

This work presents an efficient design for reconfigurable Single Instruction Multiple Data (SIMD) processors tailored for IoT wireless sensor network applications, particularly focusing on patient monitoring. The design incorporates the use of a Dual Field Vedic Multiplier, which enhances computational efficiency. The research delves into the impact of SIMD size and the utilization of varied instruction sets on potential performance improvements. Within this work, various challenges affecting SIMD optimization for IoT applications are thoroughly explored, and comprehensive solutions are provided for different architectural scenarios. Many IoT application designs currently feature specific SIMD instructions, and while such strategies can yield substantial performance improvements, they might not be equally effective for other application domains. In this paper, the authors identify a set of generic SIMD instructions that have a transformative effect on the performance of IoT-based health monitoring applications. The proposed SIMD processor design, especially when integrated with a reconfigurable Arithmetic Logic Unit (ALU), reimagines the modifier framework for the multiplier structure. The possibilities demonstrated in this research highlight a decrease in delays and power consumption through innovative design choices. These findings underscore the effectiveness of reconfigurable processor methodologies, particularly when applied to IoT-based Wireless Sensor Network applications. The potential benefits of these reconfigurable SIMD processors can significantly enhance the capabilities and performance of IoT devices designed for healthcare and patient monitoring, contributing to more efficient and responsive systems.

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