Taylor & Francis
Taylor & Francis Group

Automatika

Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: (Print) (Online) Journal homepage: www.tandfonline.com/journals/taut20

An analytical design and analysis of a high gain switched inductor voltage multiplier cell power converter

K. Jayanthi & J. Gnanavadivel

To cite this article: K. Jayanthi & J. Gnanavadivel (2024) An analytical design and analysis of a high gain switched inductor voltage multiplier cell power converter, Automatika, 65:3, 1100-1112, DOI: 10.1080/00051144.2024.2343957

To link to this article: https://doi.org/10.1080/00051144.2024.2343957

Published online: 22 Apr 2024.

AUTOMATIKA
2024, VOL. 65, NO. 3, 1100–1112
https://doi.org/10.1080/00051144.2024.2343957

An analytical design and analysis of a high gain switched inductor voltage multiplier cell power converter

K. Jayanthi and J. Gnanavadivel

Department of Electrical and Electronics Engineering, Mepco Schlenk Engineering College, Sivakasi, Tamil Nadu, India

ABSTRACT

The proposed modified higher gain boost converter employs switched Inductor and multiplier cell-based voltage boosting techniques, as the paper represents. This converter is modelled to enhance the static gain and efficiency. As the designed topology has an incessant source current at its input side, it is ideal for solar PV applications. With a power capacity of 100 W, the proposed topology is designed to work on 24 V source input and 200 V load/output voltage. The load voltage is maintained by a PI controller, which achieves the highest efficiency of 92% under rated load conditions. The converter's transient performance with the controller is investigated under various situations, including supply voltage variation, reference voltage variation, and load power variation. Finally, the designed converter's experimental model is created to evaluate the simulated and conceptual results.

ARTICLE HISTORY
Received 6 October 2022
Accepted 10 April 2024

KEYWORDS
High gain converter; PI converter; voltage boosting techniques

1. Introduction

The usage of non-conventional energy sources is growing daily owing to the adverse effects of conventional energy sources. Hence renewable energy is used in the production of electricity. Renewable energy such as solar photovoltaic is used popularly. It can supply in the range of 10 KW, but the issue is that it produces low output voltage. Hence, a boost converter improves the voltage to higher levels. The issue with boost converters is that they have less voltage gain and higher switching stress [1]. Over the years, research has resulted in many circuit designs that can be applied to microgrids that utilize boost converters. As a result, high-gain DC–DC boost converters were required.

Boost converter structures based on impedance networks are developed using one switch with identical capacitors and Inductors [2]. The interleaved converter topologies are employed to reduce the switching stress. The floating interleaved boost converter possesses two modules linked in a cascaded manner at the output and parallel at the source side to produce a less voltage gain with reduced switching loss [3]. The converters presented in Refs [4–6] have a multiplier cell with the boost converter to generate a high static voltage gain. When the multiplier cell is used with a classic step-up converter, the load side voltage is twice that of the classical step-up converter without an increase in the switching voltage. Switch conduction losses are reduced by lowering the drain–source voltage [4]. When the multiplier cell works as a clamping circuit for regeneration, it reduces the problem of EMI generation. When the multiplier cell is combined with the step-up converter, it gives more static gain and less duty cycle [5]. The controlled inverter, which is used instead of a single transistor, reverses the multiplier input current to reduce the power loss by the capacitors. In this circuit, the capacitance of the voltage multiplier cell capacitors is also reduced [6]. Many research have been done to introduce the non-isolated DC–DC power converter topologies. Boosting of input voltage is done by switched Inductor. The concept of capacitor charging in parallel and getting discharged in series is reported in Ref. [7]. This converter has three switches and is operated by two duty ratio. The gain is achieved with a duty ratio of 0.8 to 1; however, getting such a gain is difficult [8].

A capacitor-diode network employed in the non-isolated converters improves the output voltage. The converter has two switches controlled by a single gating signal [9]. For further increase in gain, several boost and quadratic converters are used [10]. Operating the power switch with a duty ratio greater than 0.7 improves the static gain of the converter [11]. A voltage doubler circuit employed in the non-isolated converter topology doubles the output voltage, thereby improving the voltage gain [12]. High-gain extendable power converters structures are presented in Refs [13,14] and use two or more semi-conductor switches to augment the

CONTACT K. Jayanthi kjayanthi@mepcoeng.ac.in Department of Electrical and Electronics Engineering, Mepco Schlenk Engineering College, Sivakasi, Tamil Nadu 626005, India

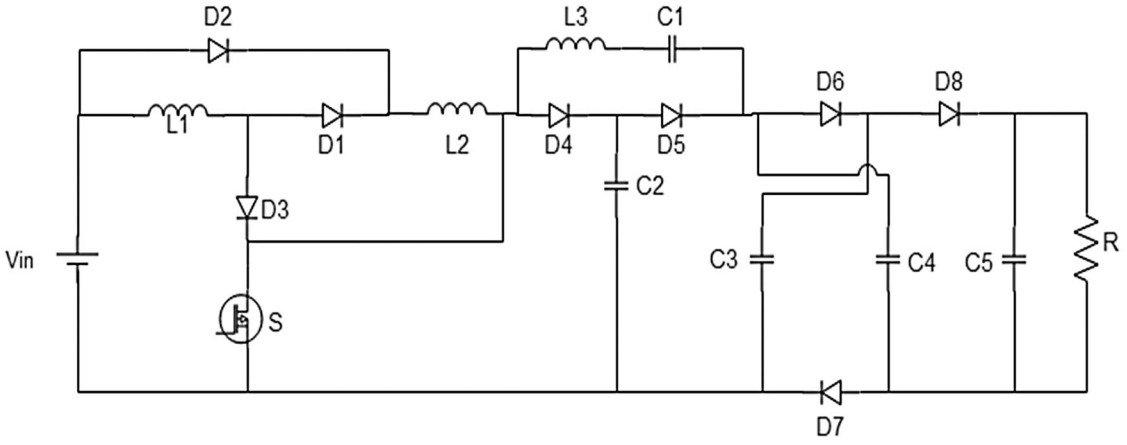


Figure 1. Topology of proposed SI-VMHG converter.

voltage gain. In extended stages, the component count increases, but voltage gain is not changed as much. DC–DC step-up power converters with high voltage gain are employed in real-time situations such as UPS, lamp ballasts, traction and medical applications [15,16]. The significant limitations of isolated DC–DC converters are transformer core saturation and low efficiency [17,18]. The switched capacitor is used with a step-up converter to give more gain in voltage. The continuous input current is obtained without maintaining a high-duty cycle [19]. The converter is designed to supply two different voltage levels, one for low-level loads and the other for high-level loads, which are very suitable for DC micro-grid applications [20].

There is great demand for DC–DC power converters having improved voltage gain with innovative characteristics. This work presents a new lofty step-up DC–DC converter topology that includes a switched inductor, multiplier cell, and only one switch. In addition, the voltage boosting techniques enhanced output voltage with less switching stress, thereby increasing efficiency.

2. Proposed switched inductor–voltage multiplier cell high gain (SI-VMHG) converter topology

The proposed SI-VMHG converter model is designed by integrating the voltage boosting cells such as the switched Inductor and multiplier to augment the voltage gain. The SI-VMHG converter uses a single power switch S, six power diodes D_1 to D_6, high frequency operated inductors L_3, L_2, L_1 and capacitors C_1 to C_5. The resistive load is considered for analysis purposes. The pictorial representation of the SI-VMHG topology is exposed in Figure 1. The SI-VMHG converter is designed by taking into consideration of the subsequent hypothesis. The power switches and power diodes are expected to be ideal; output capacitance has a significant value to get ripple-free output voltage.

3. Operating modes of proposed SI-VMHG converter

Depending on the gating pulse, the proposed model operates in five ways. The switching characteristics of the SI-VMHG model can be found in Figure 2.

Mode 1: For the time range $[t_0–t_1]$, the power semiconductor switch S is turned ON. The D_2, D_3, and D_5 power diodes are biased in the forward direction and D_1, D_4, D_6, D_7, and D_8 diodes are biased in the reverse direction. The L_1 and L_2 inductors are charged with the source voltage V_{in}. The inductor L_3 and capacitor C_1 get charged due to capacitor voltage C_2. The capacitor C_5 supplies the energy to the load resistor R. The current direction during mode 1 is pictured in Figure 3. The voltage across the L_1, L_2 and L_3 inductors are found using KVL is portrayed in 3 and are expressed in Equations (1)–(4).

$$U_{L1} = U_{in} \tag{1}$$

$$U_{L2} = U_{in} \tag{2}$$

$$U_{L3} = U_{C1} - U_{C2} \tag{3}$$

$$U_{C5} = U_0 \tag{4}$$

Mode 2: Power switch S is in ON position during time $[t_1–t_2]$. The D_2, D_3, and D_8 power diodes are in a conducting state, and D_1, D_4, D_5, D_6, and D_7 diodes are in a non-conducting state. The L_1 and L_2 inductors get charged to the V_{in}. The capacitors C_3 and C_4 release its energy, whereas the capacitor C_1 gets charged. The capacitor C_5 supplies the power to the load and is displayed in Figure 4. Using Kirchhoff's Voltage Law, the voltage across the L_1, L_2 and L_3 inductors are found and given in Equations (5)–(7).

$$U_{L1} = U_{in} \tag{5}$$

$$U_{L2} = U_{in} \tag{6}$$

$$U_{C3} - U_{C5} + U_{C4} - U_{C1} + U_{L3} = 0 \tag{7}$$

Mode 3: The power semiconductor switch S is in the ON position between time interval $[t_2–t_3]$. The D_2 and

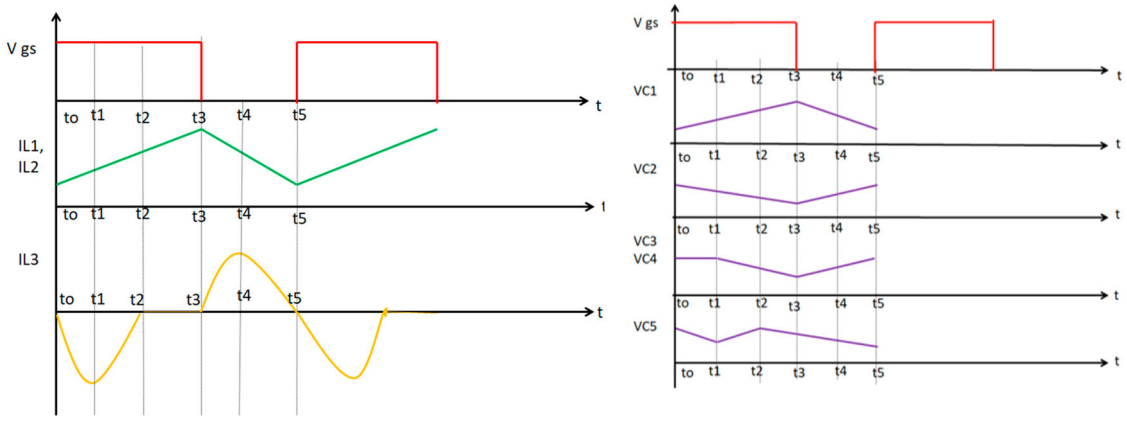


Figure 2. Switching waveform of proposed SI-VMHG converter.

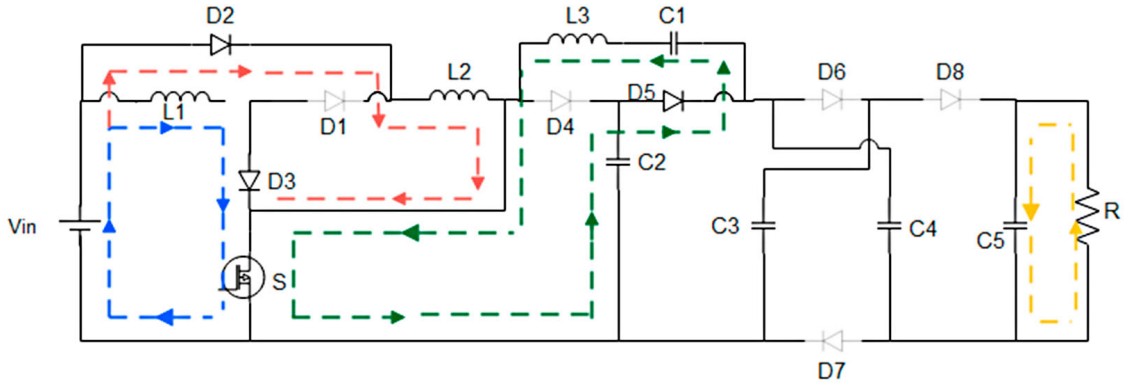


Figure 3. Mode 1 operation.

D_3 diodes are in conduction mode, and the remaining power diodes are in OFF condition. The L_1 and L_2 inductors continuously store its energy while the capacitor C_5 discharges its charge to the resistor R. The flow of the current path direction is presented in Figure 5. The L_1 and L_2 inductor voltage expressions are specified in Equations (8)–(11) after applying the KVL.

$$U_{L1} = U_{in} \tag{8}$$

$$U_{L2} = U_{in} \tag{9}$$

$$U_{L3} = 0 \tag{10}$$

$$U_{C5} = U_0 \tag{11}$$

Mode 4: During the period $[t_3–t_4]$, the semiconductor switch S is in turned OFF position. The D_1, D_4, D_6, and D_7 power diodes are forward-biased, and D_2, D_3, D_5, and D_8 the diodes are reverse-biased. The capacitor C_2 is charged by discharging the L_1 and L_2 inductors. Similarly, the L_3 inductor, C_2, C_3 and C_4 capacitors are charging due to capacitor C_1. The current flow in the circuit is depicted in Figure 6. The capacitor C_5 discharges its stored energy through R. The voltage across the passive elements is given in Equations (12)–(16).

$$U_{in} - U_{L2} - U_{C2} = U_{L1} \tag{12}$$

$$U_{L2} = U_{in} - U_{L2} - U_{L3} + U_{C1} - U_{C4} \tag{13}$$

$$U_{L3} = U_{in} - U_{L1} - U_{L2} + U_{C1} - U_{C3} \tag{14}$$

$$U_{C3} = U_{C4} \tag{15}$$

$$U_{C5} = U_0 \tag{16}$$

Mode 5: For the duration of $[t_4–t_5]$, the semiconductor switch S is in turned OFF position. The D_1, D_4, D_6, and D_7 power diodes are forward-biased, and D_2, D_3, D_5, and D_8 the power diodes are reverse-biased. Now, L_1 and L_2 inductors are discharged, and L_3 inductor is discharged in a positive direction. The C_2, C3, and C_4 capacitors start to charge, and C_1 and C_5 capacitors start to discharge. The direction of the current path is displayed in Figure 7, and the voltage expressions are given in Equations (17)–(20).

$$U_{in} - U_{L2} - U_{C2} = U_{L1} \tag{17}$$

$$U_{L2} = U_{in} - U_{L2} - U_{L3} + U_{C1} - U_{C4} \tag{18}$$

$$U_{C3} = U_{C4} \tag{19}$$

$$U_{C5} = U_0 \tag{20}$$

The static gain expression of the suggested SI-VMHG converter is determined using Equation (21) and stated in Equation (22) using the volt-sec balancing method.

$$\int_{t0}^{t1} U_{L1} dt^{I} + \int_{t1}^{t2} U_{L1} dt^{II} + \int_{t2}^{t3} U_{L1} dt^{III} + \int_{t3}^{t4} U_{L1} dt^{IV} + \int_{t4}^{t5} U_{L1} dt^{V} = 0 \tag{21}$$

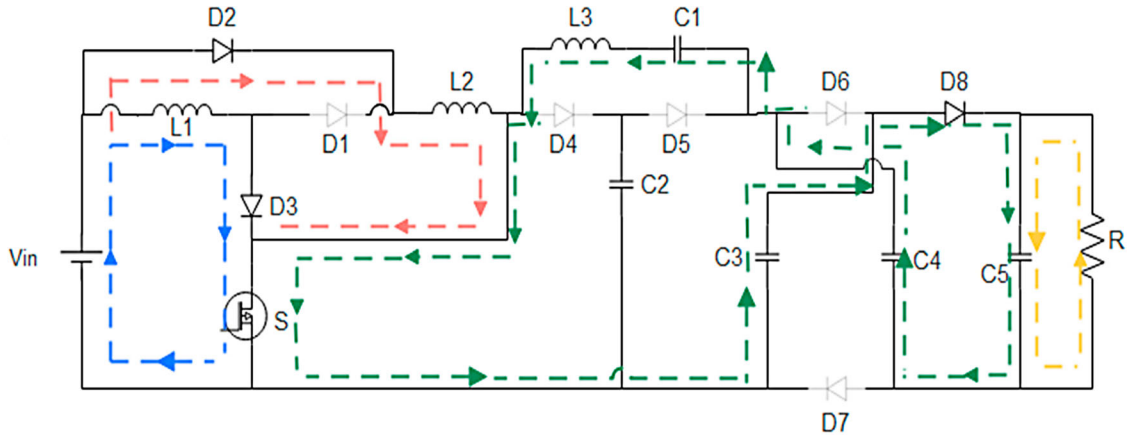


Figure 4. Mode 2 operation.

where I, II, III, IV, and V are operating modes

$$\frac{U_0}{U_{\text{in}}} = \frac{3(1+D)}{1-D} \tag{22}$$

4. Designing of inductor and selection of capacitor

4.1. Design of inductor

The inductors L_1 and L_2 ripple current during the turn-on period of the switch is computed as

$$\Delta i_{L1} = \Delta i_{L2} = \frac{U_{\text{in}}}{L1} d T_s \tag{23}$$

The derived Inductors L_1 and L_2 values are based on source voltage (V_{in}), duty ratio (d), switching frequency (f_s) and inductor ripple current (ΔI_L), the inductor values are given as per equation given in (23)

$$L_1 = L_2 = \frac{V_{\text{in}} d}{f_s \Delta i_{L1}} \tag{24}$$

The average currents through the inductors L_1 and L_2 are expressed as

$$I_{L1} = I_{L2} = \frac{2I_0}{(1-d)} \tag{25}$$

The inductor L_3 value depends on the capacitor voltage and is designed by using Equation (24)

$$L_3 = \left(\frac{U_{C3} - U_{C1}}{di}\right) dt \tag{26}$$

4.2. Capacitor selection

The energy stored in the input inductors during mode 5 is transferred to the multiplier capacitor C_2 through diode D_4. The current variations in the diode D_4 are reduced linearly because the capacitor C_2 voltage decreases and maintains constant voltage applied to the resonant inductor. The capacitors C_3 and C_4 get charged in mode 5 where the power switch S is in turn-off condition. The energy stored in the capacitors is expressed as

$$Q_{C3} = C_3 \Delta U_{C3} = \frac{I_{L1}}{2} d T_s \tag{27}$$

$$Q_{C4} = C_4 \Delta U_{C4} = \frac{I_{L1}}{2} d T_s \tag{28}$$

The final expression for the selection of capacitors is based on switching frequency (f_s), duty ratio (d), source voltage (U_{in}), output voltage (U_0) and ripple voltage (ΔU_c). The capacitor C_1–C_5 values are selected based on Equations (29)–(32).

$$C_1 = C_2 = \frac{V_0(1-d)}{R f_s \Delta U_{C1}} \tag{29}$$

$$C_3 = \frac{d V_0}{(1-d) R f_s \Delta U_{C3}} \tag{30}$$

$$C_4 = \frac{d V_0}{(1-d) R f_s \Delta U_{C4}} \tag{31}$$

$$C_5 = \frac{P_0}{f_s \Delta U_{C5}} \tag{32}$$

5. Power loss analysis

The power loss analysis of any converter topology is considered more important because the internal parasitic parameters are included. The internal parasitic resistance of inductor, capacitor and diode are considered for power calculations. The powers consumed by each of the components are computed as below. Let us consider the value of R_L is 10 mΩ.

Power Loss due to inductor: The power loss of the inductors L_1, L_2 and L_3 is derived and given in (33)

$$P_L = I_{L1}{}^2 R_L + I_{L2}{}^2 R_L + I_{L3}{}^2 R_L \tag{33}$$

The value of I_{L1}, I_{L2} and I_{L3} values are calculated using Equations (25) and the power loss is obtained as 1.65 W.

Power Loss due to Capacitors: The power loss of the capacitors is computed by using Equation (34). The

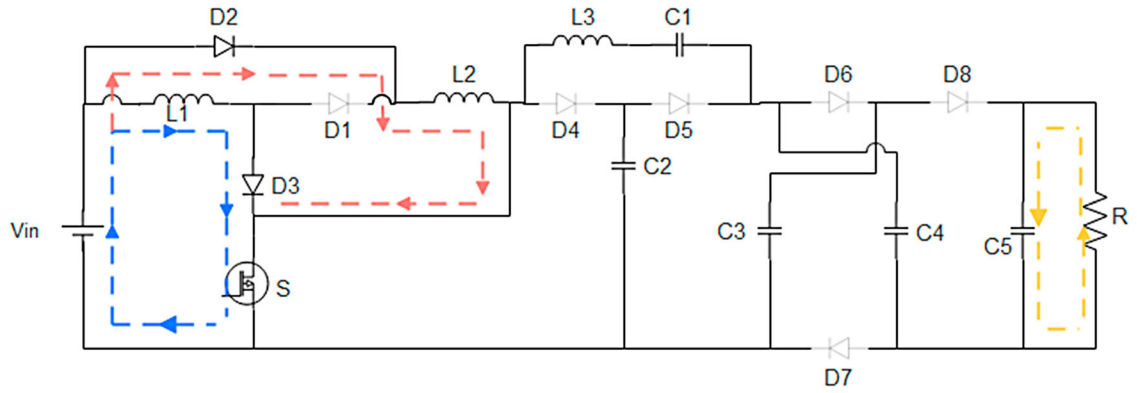


Figure 5. Mode 3 operation.

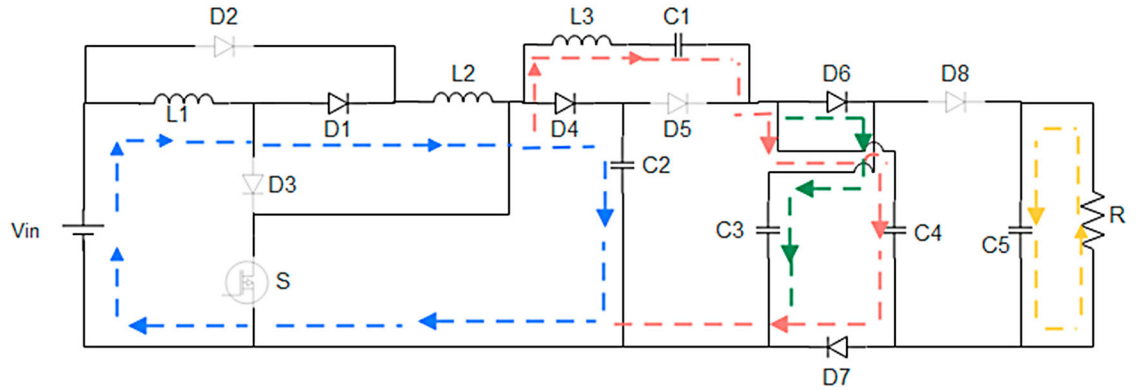


Figure 6. Mode 4 operation.

value of R_C is 10 mΩ.

$$P_C = I_{C1}{}^2R_C + I_{C2}{}^2R_C + I_{C3}{}^2R_C + I_{C4}{}^2R_C + I_{C5}{}^2R_C \quad (34)$$

The RMS current values of the capacitors I_{C3}, I_{C4} and I_{C5} are calculated using the following equations:

$$I_{C3} = I_{C4} = \frac{\sqrt{d}}{1-d} I_0 \quad (35)$$

$$I_{C5} = \frac{\sqrt{3d^2 + d}}{1-d} I_0 \quad (36)$$

The computed power loss of the capacitor is 2.18 W.

Power Loss Due to Diode: The power loss associated with the diodes D_1 to D_8 is given in (37). Let, R_D is 17.1 mΩ.

$$P_{D\_C} = I_{D1}{}^2R_D + I_{D2}{}^2R_D + I_{D3}{}^2R_D + I_{D4}{}^2R_D + I_{D5}{}^2R_D + I_{D6}{}^2R_D + I_{D7}{}^2R_D + I_{D8}{}^2R_D \quad (37)$$

$$P_{D\_C} = \frac{(7-d)I_0^2}{(1-d)^2} \quad (38)$$

Likewise, the forward voltage drop loss of the diode is given in Equation (39). Let, V_f is 0.74 V.

$$P_{D\_Vd} = I_{D1\_avg}{}^2V_F + I_{D2\_avg}{}^2V_F + I_{D3\_avg}{}^2V_F + I_{D4\_}avg^2V_F + I_{D5\_avg}{}^2V_F + I_{D6\_avg}{}^2V_F + I_{D7\_avg}{}^2V_F + I_{D8\_avg}{}^2V_F \quad (39)$$

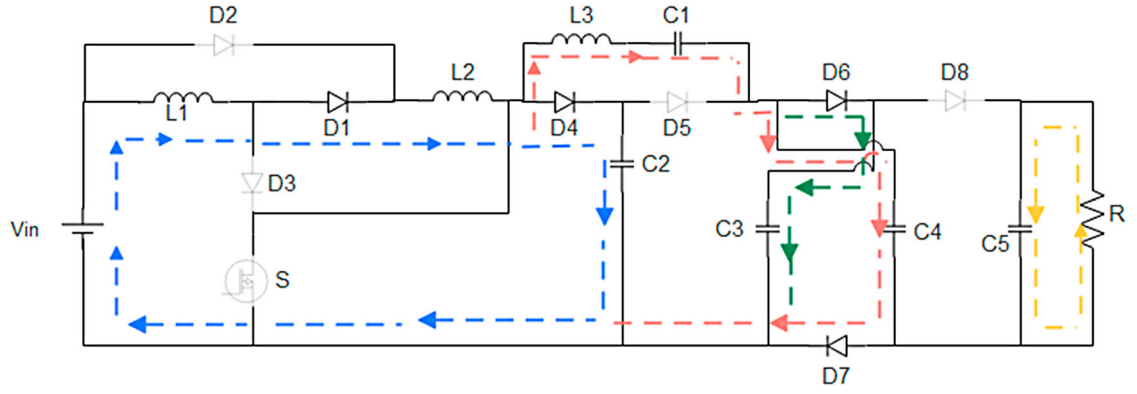


Figure 7. Mode 5 operation.

$$P_{D\_Vd} = \frac{(5-d)I_0}{(1-d)} \tag{40}$$

where $I_{D1\_avg} = 2I_0$; $I_{D2\_avg} = I_{D3\_avg} = 2dI_0/(1-d)$; $I_{D4\_avg} = I_{D5\_avg} = dI_0/(1-d)$; $I_{D6\_avg} = I_{D7\_avg} = I_{D8\_avg} = I_0$.

The computed power loss of the diode is found to be 3.69 W.

Power Loss Due to Switch: The power loss of the switch is due to switching loss and conduction loss. The power loss associated with the on-state resistance of the switch is given in (41). Let, R_s is 27 mΩ.

$$P_{S\_C} = I_{S\_RMS}{}^2 R_s \tag{41}$$

The switching loss associated with the switch is given in (42). Let, $t_{on} + t_{off}$ is 74.9 ns.

$$P_{S\_Sw} = \frac{1}{2} V_s I_s f_s (t_{on} + t_{off}) \tag{42}$$

where $I_{S\_RMS} = 16dI_0{}^2/(1-d)^2$.

The computed power loss of the switch is 2.35 W.

Thus, the total power loss of the proposed high gain converter is calculated by using the following equation:

$$P_{L\_T} = P_L + P_C + P_D + P_S = 9.87\ \text{W} \tag{43}$$

The efficiency of the proposed converter is expressed as

$$\text{Efficiency} = \frac{P_0}{P_{in}} = 91.02\% \tag{44}$$

6. Investigation of the proposed SI-VMHG converter with previously designed converter topologies

The static voltage gain, component count, stress in the semiconductor devices, and efficiency of the SI-VMHG converter parameters are compared with various existing converters are tabulated in Table 1. In comparison with the step-up converter, the SI-VMHG topology achieves a 77% increase in voltage gain. The static gain of the converters against the duty ratio is drawn and is shown in Figure 8. The diode switching stress of the SI-VMHG converter with the converter presented in Ref. [2] is equal, but it is 24% less when compared with the converter in Ref. [1]. The amount of switching components in the SI-VMHG converter is 50% lesser than the converter in Ref. [12]. The reduction of component counts leads to a reduction in the power density of the circuit. The simulated efficiency of the proposed SI-VMHG model under rated load conditions is 92%.

7. Results and discussions of simulation

The proposed converter topology is created in MATLAB using the Matlab Simulink tool. It is designed to operate with a 24 V source voltage, a 200 V load voltage, and a 100 W load power. Based on Equations (23)–(28),

Table 1. Analysis of the SI-VMHG converter topology with previously designed converters.

Parameter	Boost	[1]	[2]	[12]	Proposed SI-VMHG converter
Static gain	$\frac{1}{1-d}$	$\frac{1+d}{1-d}$	$\frac{2(1+d)}{1-d}$	$\frac{1+3d}{1-d}$	$\frac{3(1+d)}{1-d}$
Switch count	1	2	1	2	1
Diode count	1	2	6	2	8
Capacitors count	1	4	3	3	5
Inductors count	1	6	2	3	3
Switching stress	V_0	$\frac{V_0}{1+d}$	$\frac{V_0}{2}$	$\frac{M}{1+3d}$	$\frac{V_0}{2}$
Diode stress	V_0	$\frac{V_0}{1+d}$	$\frac{V_0}{2}$	$\frac{2M}{1+3d}$	$\frac{V_0}{2}$
Efficiency	80%	89%	83%	89%	92%

Table 2. Simulated parameters of proposed SI-VMHG converter.

Parameters	Values
Source voltage	24–48 V
Output/load voltage	200 V
Output/load power	100 W
Switching frequency	20 kHz
Inductor	$L_1 = L_2 = 330$ μH, $L_3 = 1$ μH
Capacitor	$C_1 = C_2 = 100$ μF, $C_3 = C_4 = 10$ μF, $C_5 = 100$ μF

the values of the power circuit components such as inductors and capacitors are calculated and displayed in Table 2. The voltage at the converter's output varies for duty ratio, but the converter should maintain the same voltage of 200 V at the output side. The constant load voltage is achieved by using the PI controller. The controller parameters are regulated in such a way as to maintain the voltage at the output constant. The Z-N tuning methodology is adopted to obtain the proportional gain k_P and integral gain k_i values. The block diagram representation of PWM generation using the PI controller is shown in Figure 9. The closed-loop MATLAB simulation of the SI-VMHG converter is pictured in Figure 10. The simulated input and load voltage, current, and power graphical waveforms are shown in Figure 11. The controller maintains a steady voltage of 200 V in the load side of SI-VMHG converter for a voltage of 24 V. The simulated graphical representation of inductors and diodes voltage and current are pictured in Figures 12 and 13.

The performance of SI-VMHG converter is analyzed under different conditions, including voltage at the input, setpoint/reference voltage, and output/load power variations.

To investigate the controller's performance with the SI-VMHG converter topology, different voltage inputs are varied over a wide range of time intervals from 24 to 48 V. The input voltage of 24 V is initially considered at time $t = 0$ s. The output/load voltage and the load power are regulated to 200 V and 100 W, respectively. A voltage variation of 24–34 V occurred at $t = 0.4$ s. The change in input voltage tends to enhance the output voltage and load power. The error signal is generated and fed into the controller unit for generating the gating signal to maintain the output voltage and load power. Similarly, the source voltage varies from 34 to 48 V

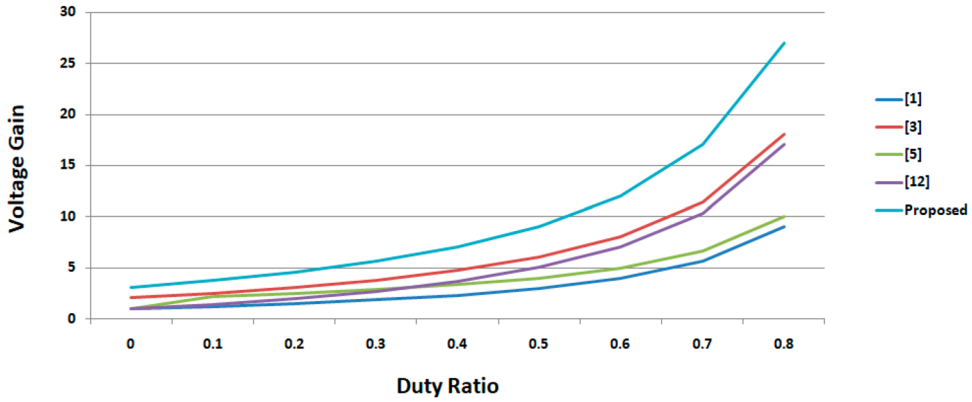


Figure 8. Voltage gain against duty ratio.

Table 3. Source voltage variations.

Voltage on source side (V)	Current on source side (A)	Power on source end (W)	voltage on load side (V)	Current on load side (A)	Power on load end (W)	Efficiency (%)
24	4.58	110	200	0.5	100	90
34	3.207	109	200	0.495	100	91.74
48	2.275	109.2	200	0.5	100	91.57

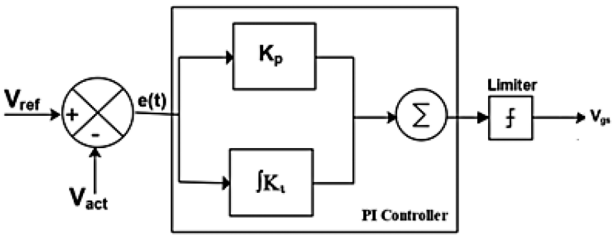


Figure 9. Generation of PWM signal using PI controller.

at $t = 0.7$s; the controller senses the change in output voltage and generates the gating signal for maintaining the voltage at an output of 200 V. The pictorial representation of the input voltage at different time durations is displayed in Figure 14, and the values are tabulated in Table 3.

The controllability of the controller can be studied by altering the setpoint/ reference voltage. On the source side of the converter, the voltage of 24 V is maintained. During time $t = 0$ s, the setpoint/reference voltage is made at 200 V, and the output voltage and load power are maintained at 200 V and 100 W, respectively. At time $t = 0.4$ s, the setpoint value is increased from 200 to 220 V; the controller senses the change in voltage and generates the required gating signal to maintain the reference voltage. Likewise, during time $t = 0.7$ s, the reference voltage decreases from 220 to 180 V. At that time, the controller generates the PWM signal to maintain the reference voltage. The controller took less than 0.02s to maintain the reference value, the load/output power and is presented in Figure 15. The changes in voltage, current, and power values related to the setpoint/reference values variations are tabulated in Table 4.

The proposed converter is again tested under different load powers at different durations to assess its working with the controller. During $t = 0$ s, the converter is operated at half the rated load power of 50 W. Power and voltage are maintained at the output. The load power is increased from 50 to 100 W during time $t = 0.5$ s. The controller estimates the change in load power variations, and an appropriate gating signal is applied to the power MOSFET to turn on. The change in load power variations at different time durations is shown in Figure 16, and the corresponding variations in voltage, current and power values at the source side and load end are tabulated in Table 5.

8. Experimental prototype model

A hardware prototype model of the SI-VMHG topology isdeveloped to check the simulation results. Prototype hardware is designed using a voltageof 20 and 240 V at input and output for power at the load of 100 W. The detailed hardware specification of the SI-VMHG topology is tabulated in Table 6. Figure 17 presents the experimental prototype model of the proposed SI-VMHG topology.

The gating pulse for the converter is obtained using a PIC 18F452 microcontroller. The power circuit and the gate driver circuit are presented in Figure 17. In order to obtain a load voltage of 100 V from a source voltage of 10 V, a duty ratio of 0.5 is needed. The load voltage of 86 V is obtained experimentally and is shown in Figure 18(a). Likewise, for a 200 V load voltage, input voltage of 20 V, the experimental output voltage of 199 V is obtained and pictured in Figure 18(b). The inductors (L_1, L_2 and L_3) current waveforms are obtained experimentally and displayed in Figure

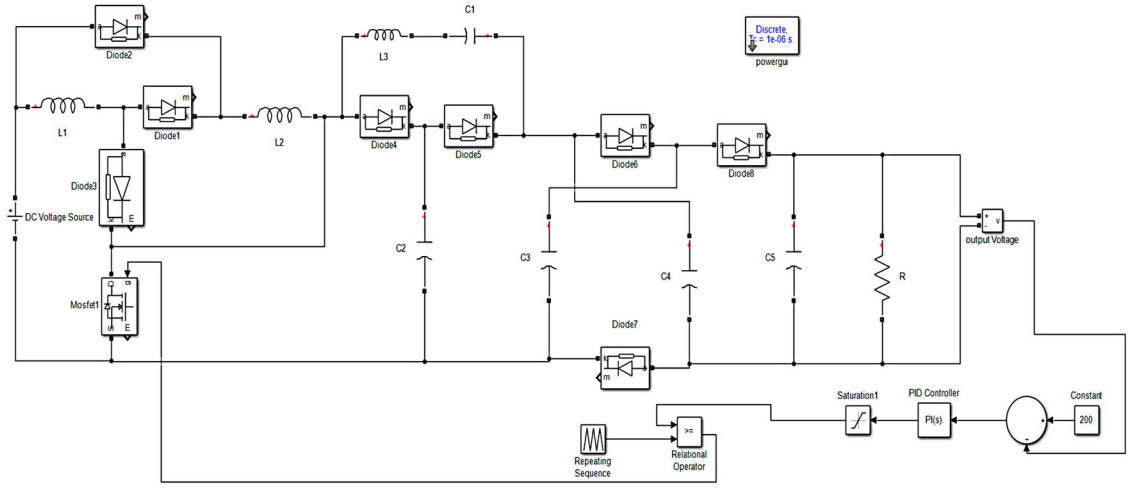


Figure 10. Closed-loop simulation diagram of proposed SI-VMHG converter.

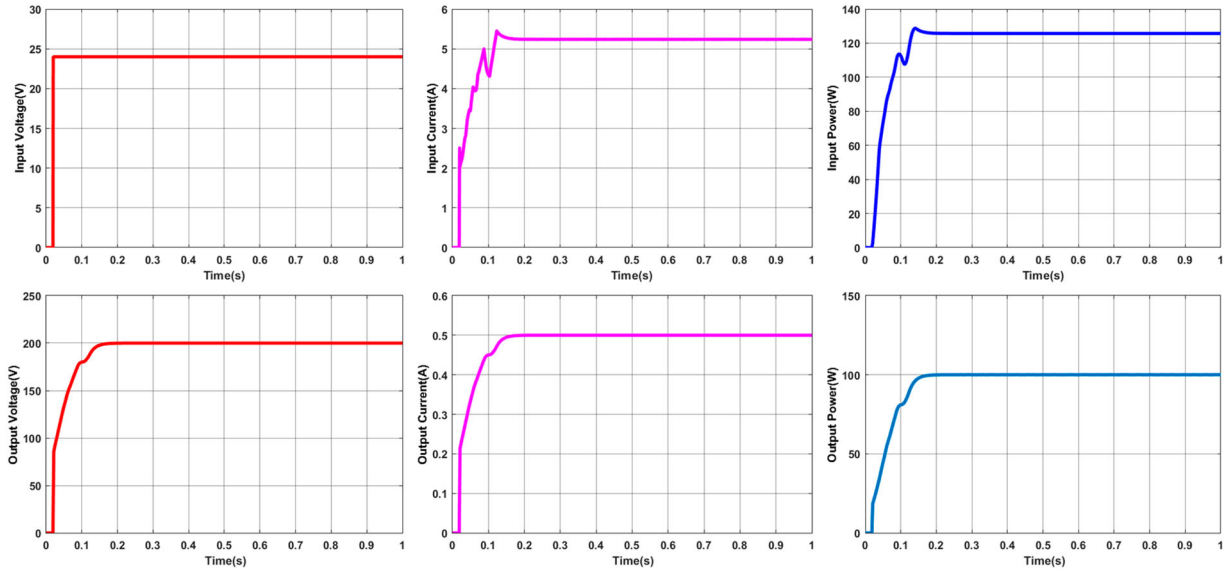


Figure 11. Closed-loop simulated waveforms of proposed SI-VMHG converter topology.

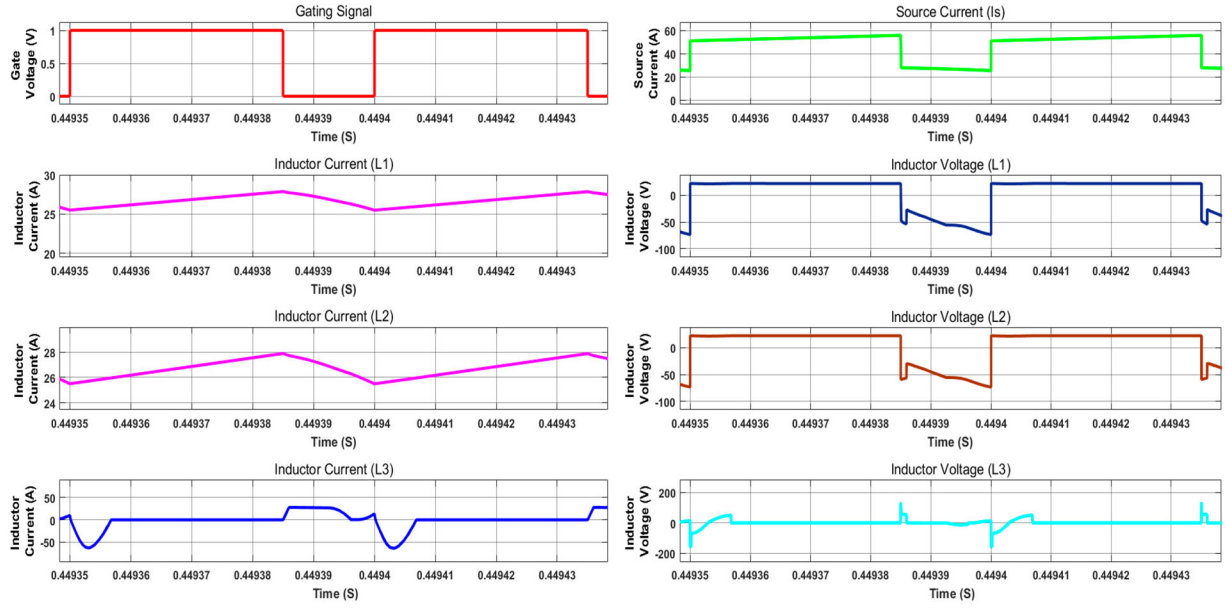


Figure 12. Closed-loop simulated current and voltage waveforms of inductors in proposed SI-VMHG converter.

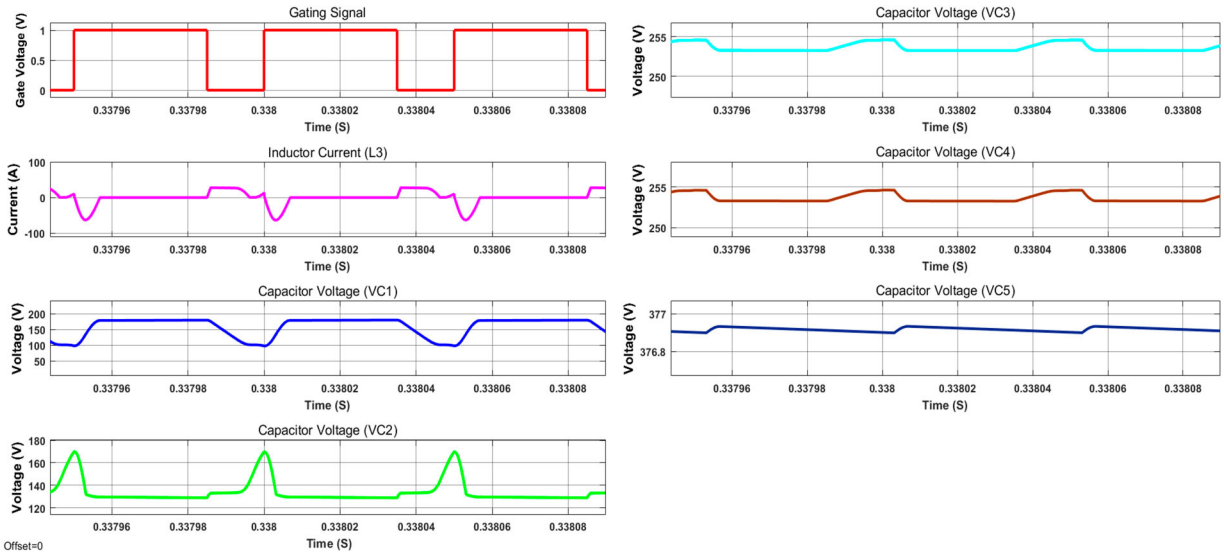


Figure 13. Closed-loop simulated waveforms of inductor current and capacitor voltage of proposed converter.

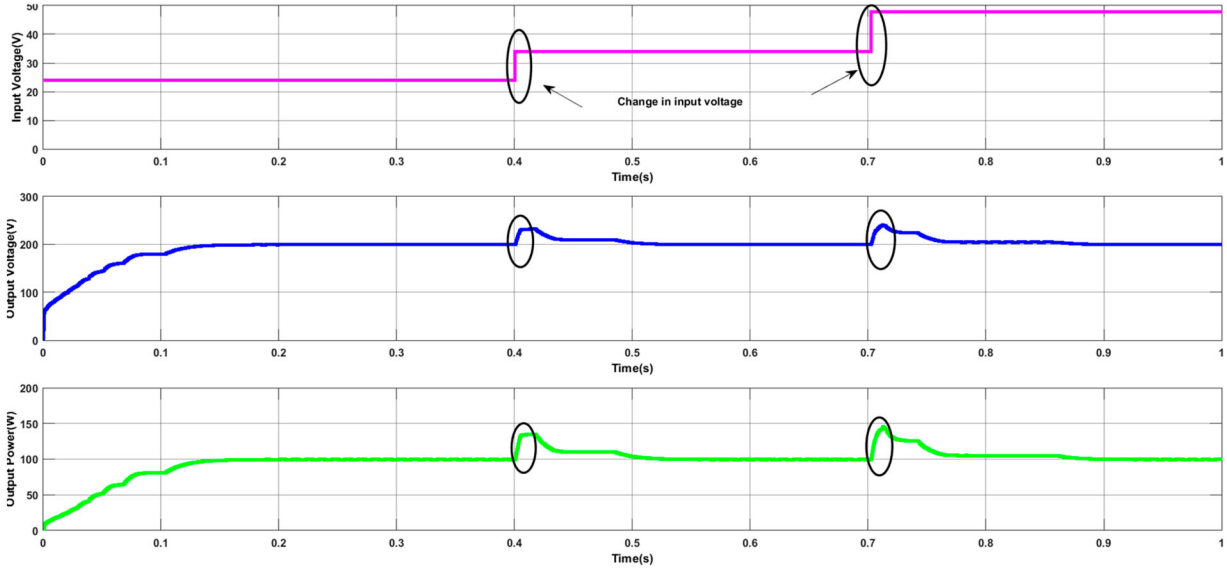


Figure 14. Performance analysis of proposed SI-VMHG converter under input voltage variation.

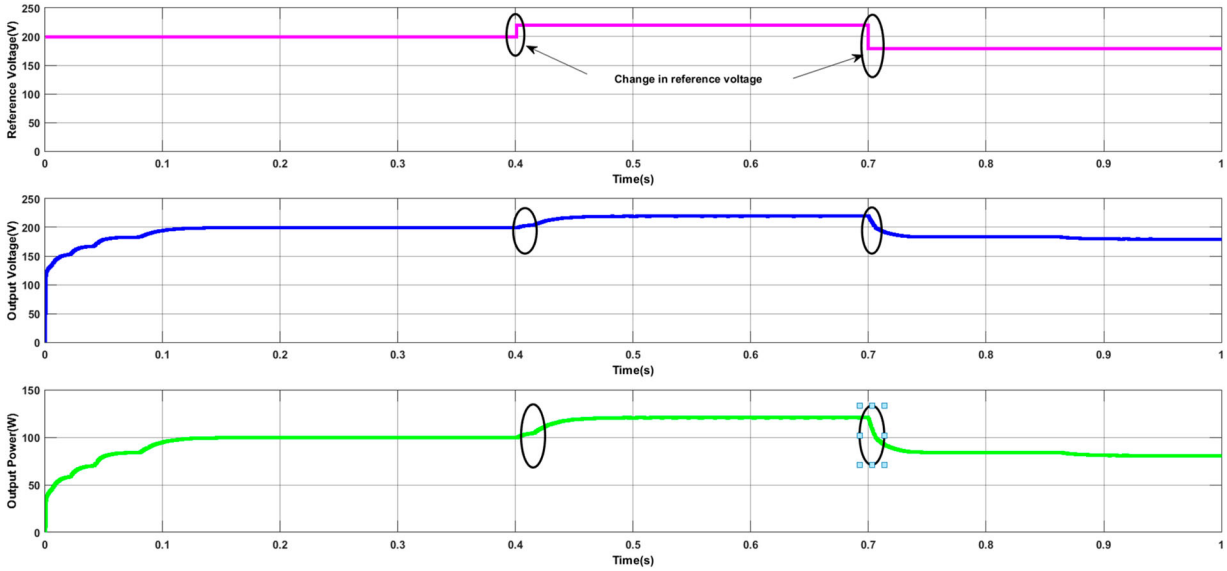


Figure 15. Performance analysis of proposed SI-VMHG converter under setpoint/reference voltage variation.

Table 4. Reference voltage variations.

Voltage on source side (V)	Current on source side (A)	Power on source end (W)	Reference voltage (V)	voltage on load side (V)	Current on load side (A)	Power on load end (W)	Efficiency (%)
24	5.5	132	220	220	0.55	121	91.66
	4.58	110	200	200	0.5	100	90
	3.644	87.46	180	180	0.446	79.55	90.95
	5.5	132	220	220	0.55	121	91.66

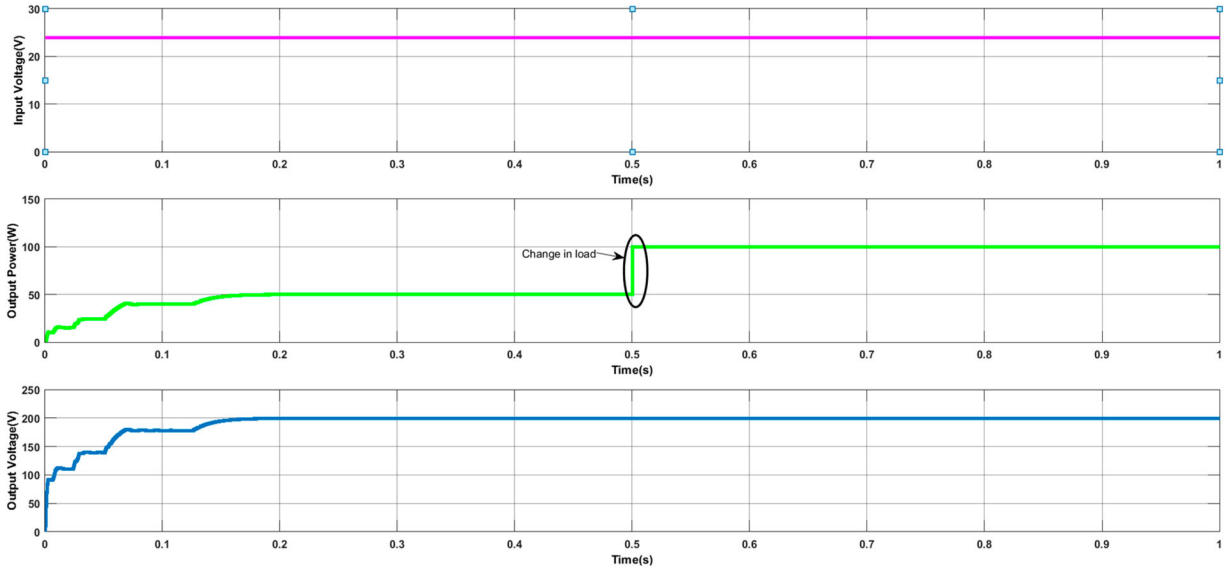


Figure 16. Performance analysis of the proposed converter under load power variations.

18(c,d) and are validated with the simulated waveforms. The diode voltage and current waveforms are found and are shown in Figure 18(e–k). Similarly, the voltage across the switch and current flows through the switch is pictured in Figure 18(l). In order to validate the controllers' performance, a step change in source voltage variation and load power variations are depicted in Figure 18(m,n).

9. Conclusion

The proposed SI-VMHG converter is based on a boost converter that uses switched inductors and voltage multipliers. The proposed topology maintains a continuous current at the source side, making power devices less susceptible to switching stress. The converter is modelled for the voltage rating of 24 V/200 V

Table 5. Load power variation.

Voltage on source side (V)	Current on source side (A)	Power on source end (W)	Current on load side (A)	Voltage on load side (V)	Power on load end (W)	Efficiency (%)
24	4.58	110	0.5	200	100	90
	2.763	66.3	0.252	200	50	76
	3.87	93	0.377	200	75	81.07
	4.58	110	0.5	200	100	90

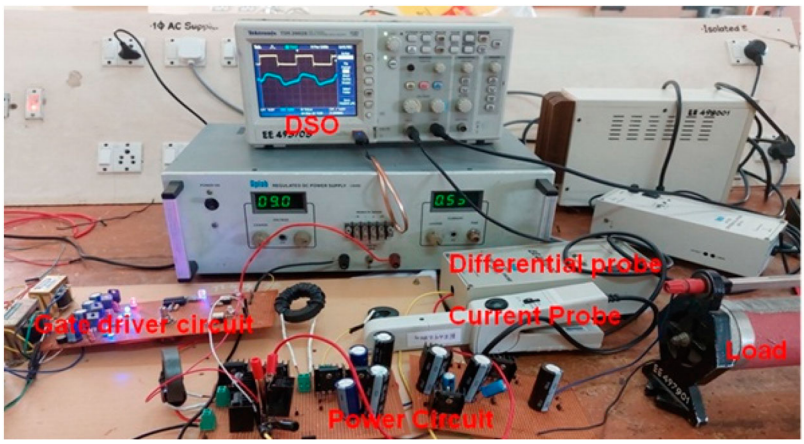
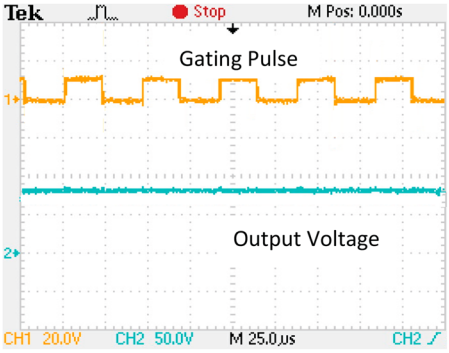
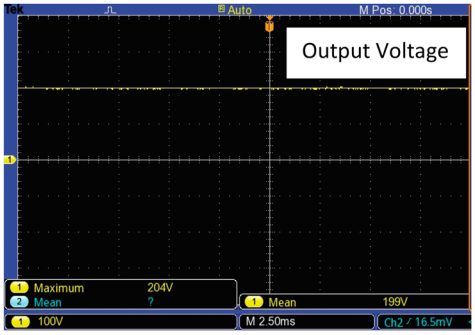


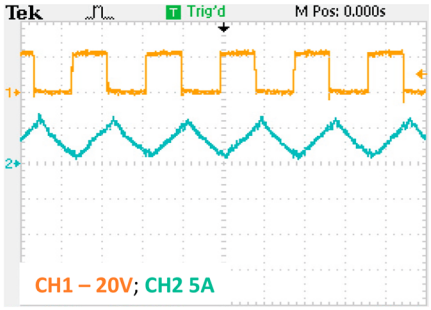
Figure 17. Hardware prototype model.



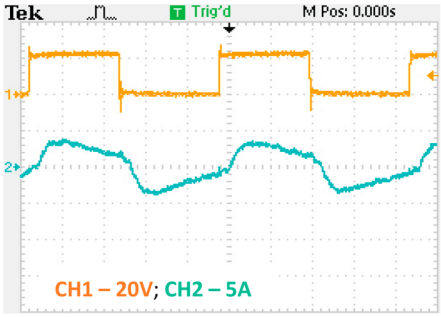
(a) Gating Pulse & Output Voltage Waveforms for the input voltage of 10V



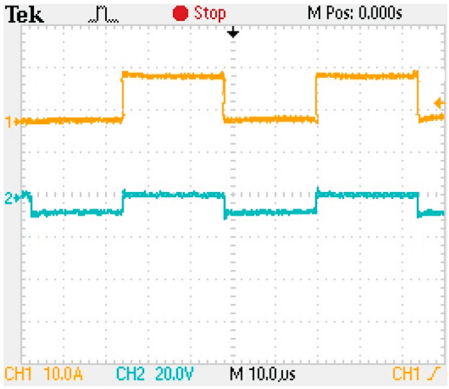
(b) Output Voltage Waveforms for the input voltage of 20 V



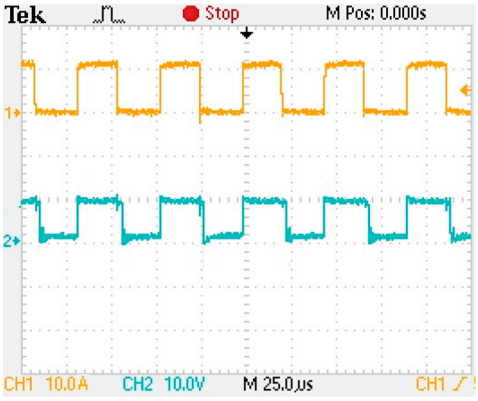
(c) Gating Pulse & Inductor (L_1 & L_2) current Waveforms



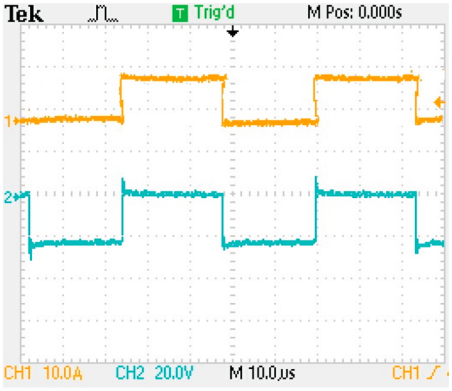
(d) Gating Pulse & Inductor (L_3) current Waveforms



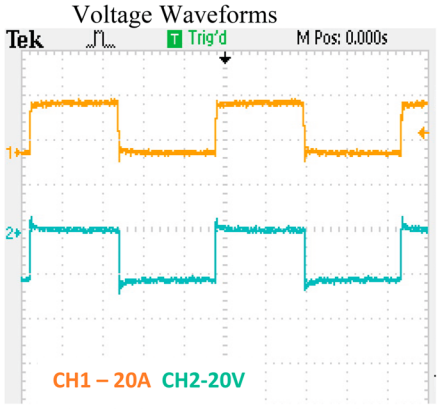
(e) Diode D1 Current & Voltage Waveforms



(f) Diode (D_2 & D_3) Current & Voltage Waveforms

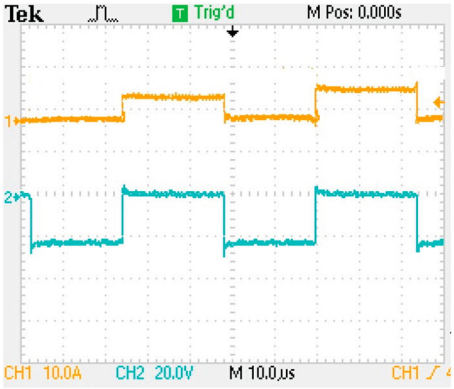


(g) Diode (D_4) Current & Voltage Waveforms

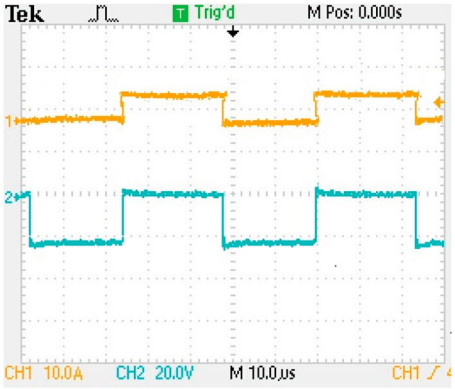


(h) Diode (D_5) Current & Voltage Waveforms

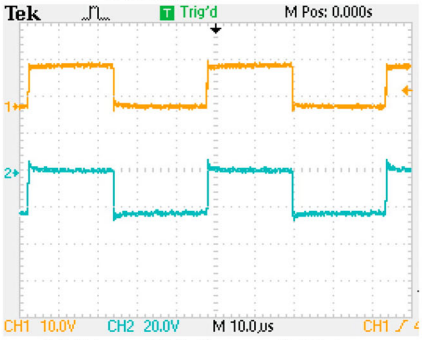
Figure 18. (a) Gating pulse and output voltage waveforms for the input voltage of 10 V; (b) output voltage waveforms for the input voltage of 20 V; (c) gating pulse and inductor (L_1 and L_2) current waveforms; (d) gating pulse and inductor (L_3) current waveforms; (e) Diode D1 current and voltage waveforms; (f) Diode (D_2 and D_3) current and voltage waveforms; (g) Diode (D_4) current and voltage waveforms; (h) Diode (D_5) current and voltage waveforms; (i) Diode (D_6) current and voltage waveforms; (j) gating pulse and diode (D_7) voltage waveforms; (k) diode (D_8) current and voltage waveforms; (l) switch current and voltage waveforms; (m) step response for input voltage variation waveforms; and (n) step response for load power variation waveforms.



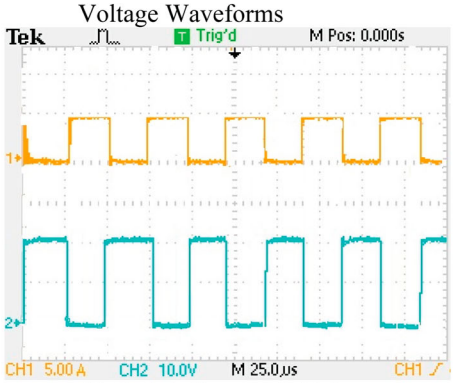
(i) Diode (D_6) Current & Voltage Waveforms



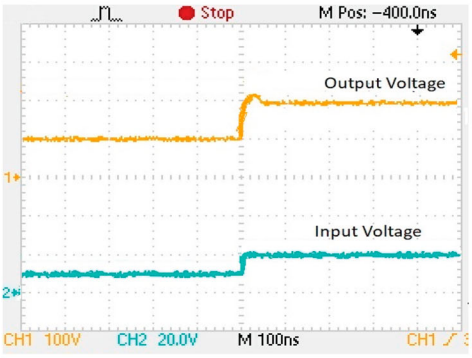
(j) Gating Pulse & Diode (D_7) Voltage Waveforms



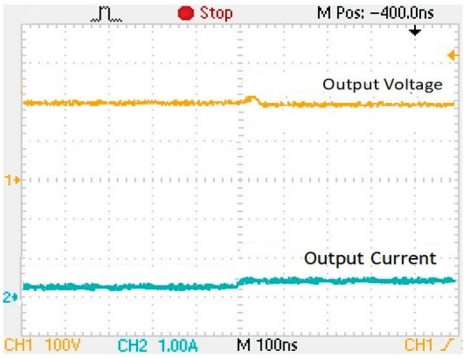
(k) Diode (D_8) Current & Voltage Waveforms



(l) Switch Current & Voltage Waveforms



(m) Step response for input Voltage variation Waveforms



(n) Step response for load power variation Waveforms

Figure 18. Continued.

Table 6. Hardware specifications for proposed SI-VMHG converter.

Parameters	Values
Source voltage (V_{in})	20 V
Load voltage (V_0)	200 V
Output power (P)	100 W
Switching frequency (f_s)	20 kHz
Inductor	$L_1 = L_2 = 330$ µH, $L_3 = 1$ µH
Capacitor	$C_1 = C_2 = 100$ µF, $C_3 = C_4 = 10$ µF, $C_5 = 100$ µF
Diode	MUR3060PT
Switch	IRFP9240

and power of 100 W. The operating modes and the converter component design values are designed. The proposed SI-VMHG converter simulation studies are performed using MATLAB Simulink tool. The performance behaviour of the SI-VMHG under open loop and closed loop simulations is also done. The PI controller is used to regulate the load voltage of SI-VMHG converter. In addition to that, analyses of the proposed SI-VMHG converter's performance under various conditions are also provided. Finally, the hardware prototype is modelled, and the experimental result certifies the simulated and theoretical values. From the analysis, it is inferred that the SI-VMHG converter model is compatible with solar PV applications.

Disclosure statement

No potential conflict of interest was reported by the author(s).

ORCID

K. Jayanthi http://orcid.org/0000-0002-8945-5401

References

[1] Li Q, Xu L, Ma R, et al. An improved floating interleaved boost converter with the zero-ripple input current for

fuel cell application. IEEE Trans Energy Convers. 2019 Dec;34(4):2168–2174. doi:10.1109/TEC.2019.2936416
[2] Shanthi T, Prabha SU, Sundaramoorthy K. Non-isolated n- stage high step-up DC-DC converter for low voltage DC source integration. IEEE Trans Energy Convers. 2021 Sep;36(3):1625–1630. doi:10.1109/TEC.2021.3050421
[3] Fusheng Z, Naayagi RT. Power converters for DC microgrids – modelling and simulation. IEEE innovative smart grid technologies –Asia (ISGT Asia); 2018 Jul. p. 994–997.
[4] Prudente M, Pfitscher LL, Gules R. A boost converter with voltage multiplier cells. IEEE; 2005 Apr. p. 2716–2721.
[5] Prudente M, Pfitscher LL, Emmendoerfer G, et al. Voltage multiplier cells applied to non-isolated DC-DC converters. IEEE Trans Power Electron. 2008 Mar;23(2):871–887. doi:10.1109/TPEL.2007.915762
[6] Berkovich Y, Axelrod B, Shoshani D, et al. DC-DC converter based on the bipolar boost converter and Dickson voltage multiplier. IEEE; 2018 May.
[7] Axelrod B, Berkovich Y. Switched-capacitor/ switched-inductor structures for getting transformerless hybrid DC-DC PWM converters. IEEE Trans Circuits Syst. 2008 Mar;55(2):687–694. doi:10.1109/TCSI.2008.916403
[8] Lakshmi M, Hemamalini S. Non isolated high gain DC-DC converter for DC microgrids. IEEE Trans Ind Electron. 2018 Feb;65(2):1205–1212. doi:10.1109/TIE.2017.2733463
[9] Yang L-S, Liang T-J. Transformerless DC-DC converters with high step-up voltage gain. IEEE Trans Ind Electron. 2009 Aug;56(8):3144–3151. doi:10.1109/TIE.2009.2022512
[10] Zhang Y, Liu H, Sumner M, et al. DC-DC boost converter with a wide input range and high voltage gain for fuel cell vehicles. IEEE Trans Power Electron. 2019 May;34(5):4100–4111. doi:10.1109/TPEL.2018.2858443
[11] Gu Y, Chen Y. High step-up DC-DC converter with active switched LC network for photovoltaic systems. IEEE Trans Energy Convers. 2019 Mar;34(1):321–329. doi:10.1109/TEC.2018.2876725
[12] Salvador MA, Lazzarin TB. High step-up DC-DC converter with active switched inductor and passive switched capacitor networks. IEEE Trans Ind Electron. 2018 Jul;65(7):5644–5654. doi:10.1109/TIE.2017.2782239
[13] Babaei E, Maheri HM, Sabahi M, et al. Extendable non-isolated high gain DC-DC converter based on active-passive inductor cells. IEEE Trans Ind Electron. Dec.2018;65(12):9478–9487. doi:10.1109/TIE.2018.2807367
[14] Saadat P, Abbaszadeh K. A single switch high step-up DC-DC converter based on quadratic boost. IEEE Trans Ind Electron. 2016 Dec;63(12):7733–7742. doi:10.1109/TIE.2016.2590991
[15] Bryant B, Kazimierczuk MK. Voltage-loop power-stage transfer functions with MOSFET delay for boost PWM converter operating in CCM. IEEE Trans Ind Electron. 2007 Feb;54(1):347–353. doi:10.1109/TIE.2006.885136
[16] Wu X, Zhang J, Ye X, et al. Analysis and derivation for a family ZVS converter based on a new active clamp ZVS cell. IEEE Trans Ind Electron. 2008 Feb;55(2):773–781. doi:10.1109/TIE.2007.907675
[17] Ajami A, Ardi H, Farakhor A. A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. IEEE Trans Power Electron. 2013 May;30:4255–4263.
[18] Chen S-M, Lao M-L, Hsieh Y-H, et al. A novel switched-coupled-inductor DC-DC step-up converter and its derivatives. IEEE Trans Ind Appl. 2015 Feb;51(1):309–312. doi:10.1109/TIA.2014.2332642
[19] Haripriya T, Parimi AM, Rao UM. Performance Evaluation of high voltage gain boost converters for DC grid integration. International conference on circuit, power and computing technologies; 2016.
[20] Sahoo M, Kumar KS. High gain step-up DC-DC converter for DC micro-grid application. IEEE; 2014 Jun.