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Automatika

Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: (Print) (Online) Journal homepage: www.tandfonline.com/journals/taut20

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To cite this article: Tomislav Ivaniš, Marinko Kovačić, Martin Makar & Željko Jakopović (2024) Advanced gate driving concepts and switching optimization for SiC semiconductors, Automatika, 65:3, 1300-1314, DOI: 10.1080/00051144.2024.2362525

To link to this article: https://doi.org/10.1080/00051144.2024.2362525

AUTOMATIKA
2024, VOL. 65, NO. 3, 1300–1314
https://doi.org/10.1080/00051144.2024.2362525

RESEARCH ARTICLE

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Advanced gate driving concepts and switching optimization for SiC semiconductors

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ABSTRACT

Silicon carbide (SiC) MOSFETS are increasingly favoured in power electronics for their improved properties compared to silicon-based counterparts, such as IGBTs. Their ability to operate at higher switching frequencies and execute faster switching transients is notable. However, these features also raise significant concerns with electromagnetic interference (EMI). To exploit the full capabilities of SiC-based technology, meticulous design strategies encompassing the power stage, commutation loop, and gate drive are essential. This paper conducts a comprehensive review of existing gate drive techniques aimed at enhancing the performance of SiC devices. Moreover, this study introduces an innovative approach for optimizing switching processes through the use of active gate drivers (AGD). By pre-mapping the gate-source voltage profiles for different conditions (such as load current, temperature, and DC-link voltage), it is possible to achieve a significantly improved switching trajectory. This optimization process can be applied on a cycle-by-cycle basis in practical scenarios. Herein, pre-mapping and optimization have been experimentally confirmed in a half-bridge configuration. Through simulation, it is demonstrated that optimizing the switching trajectory can lead to a balanced compromise between EMI and switching losses, showcasing the potential for significant performance enhancements in SiC device operation.

ARTICLE HISTORY
Received 14 February 2024
Accepted 26 May 2024

KEYWORDS
Active gate driver; EMI control; dv/dt limiting; switching optimization; hard-switching model

1. Introduction

Elevating the performance and efficiency of power electronics, silicon carbide (SiC) power transistors have emerged as pivotal elements in the field's development. Their impact is pronounced, with SiC semiconductors being integrally used in industries such as automotive, energy, and manufacturing. The advantages of SiC technology, including fast switching speeds and reduced channel resistance, contribute to enhanced efficiency, reduced heatsink requirements, superior dynamic performance, and the facilitation of innovative applications.

Performance improvements from Silicon devices stem from enhanced material properties. However, regardless of the topology used, fast switching which characterizes SiC power transistors causes multiple challenges in the application, namely the need for improved filtering of electromagnetic interference (EMI), careful commutation loop design, and improved gate drive.

Adjusting the gate resistance or applying the appropriate voltage waveform to the MOSFET gate can mitigate EMI and switching losses [1]. Recent studies have also explored passive techniques for optimizing these parameters [2]. The design of the gate drive stage is crucial in power electronics, particularly with active gate drives, due to its significant impact on system performance.

This paper is an extension of [3], and is organized as follows: Section 2 covers an overview of a switching model for a hard-switched SiC half-bridge. Next, Section 3 covers a basic overview of switching influence on EMI, with a focus on conducted emissions of a half-bridge. In Section 4 a comparative analysis of advanced gate drivers is shown. Section 5 covers the switching optimization, direct and inverted maps for an active gate driver. Section 6 showcases experimental verification of the concept, while Section 7 simulates the optimized active switching strategy for a three-phase inverter. Finally, a conclusion and result summary is given in Section 8.

2. SiC MOSFET hard-switching model

The most used building block of modern power electronics converters is a two-quadrant half-bridge. Its model is depicted in Figure 1, showing well documented parasitic elements, which will be discussed further on. To design an appropriate gate drive for the SiC MOSFET, it is required to study the basic model of the SiC MOSFET switching in a half-bridge configuration.

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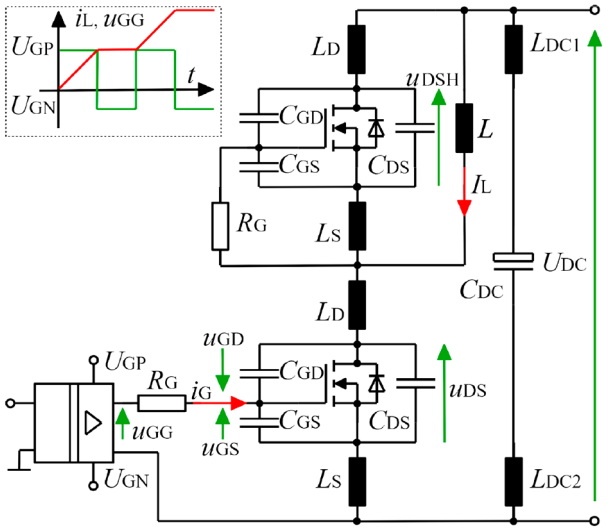

Figure 1. Half-bridge with parasitic elements in the commutation loop.

2.1. Half-bridge parasitic elements and switching process

The basic building elements of a half-bridge are a transistor pair and a DC-link capacitor. However, additional parasitic elements appear due to the layout of individual connecting elements, printed circuit board (PCB) or module segments, and component internals.

Identifying parasitic elements in the switching loop necessitates analysing inductances from filter capacitors, connecting buses, and transistor terminals. The total parasitic inductance, L_Σ, is the sum of all inductances in the commutation loop (single transistor + DC-link). The inductance of the source is especially important as it reduces switching speed and affects voltage overshoots. Lower voltage overshoots enable the transistors to operate at higher voltages, improving the utilization of SiC MOSFETs and power densities of converters [4, 5]. In addition to the commutation loop inductance, the parasitic capacitance to the heatsink and the internal parasitic capacitances of the MOSFET need to be considered. The parasitic capacitances of MOSFETs are highly non-linear and greatly affect the switching. They are labelled as $C_{ISS} = C_{GD} + C_{GS}$ and $C_{OSS} = C_{GD} + C_{DS}$. The gate voltage at which the channel current is just barely supported is defined as:

$$U_{PL} = U_{TH} + \frac{I_{CH}}{g_{fs}} \approx U_{TH} + \frac{I_L}{g_{fs}} \tag{1}$$

Here U_{PL} and U_{TH} are plateau and threshold voltages respectively. The plateau voltage is channel current dependent and for a given load current (I_L), U_{PL} is lower for turn-off and higher for turn-on due to displacement currents flowing through MOSFET parasitic capacitances [6]. Because of this, the plateau voltage is often numerically solved. However, most studies often use an approximation and use the load current (I_L) as the channel current. Transconductance (g_{fs}), is defined as the slope of the MOSFET transfer characteristics in an ohmic region at a specific operating point: $g_{fs} = \partial i_D / \partial u_{GS}$. The resonant circuit formed by parasitic capacitances and inductances often leads to ringing at the switching transition's conclusion [4]. For symmetrical high-side and low-side transistors, the ringing frequency is determined by the RLC circuit of the switching loop and one transistor's parasitic capacitance, given by:

$$f_r = \frac{1}{2\pi\sqrt{L_\Sigma C_{OSS}}} \tag{2}$$

Lowering parasitic inductance reduces the energy in parasitics, thereby diminishing EMI. Yet, it's shown that the majority of converter noise stems from the switch's current and voltage changes.

Table 1. System equations for half bridge in Figure 1.

$u_{GG}(t) = R_G i_G(t) + u_{GS}(t) + L_S \frac{d(i_D(t)+i_G(t))}{dt}$	(3)
$u_{GS}(t) = u_{GD}(t) + u_{DS}(t)$	(4)
$U_{DC} = u_{DS}(t) + L_\Sigma \frac{di_D(t)}{dt} + L_S \frac{di_G(t)}{dt} + u_{DSH}(t)$	(5)
$i_G(t) = C_{GS} \frac{du_{GS}(t)}{dt} + C_{GD} \frac{du_{GD}(t)}{dt}$	(6)
$i_D(t) = i_{CH}(t) + C_{DS} \frac{du_{DS}(t)}{dt} - C_{GD} \frac{du_{GD}(t)}{dt}$	(7)

2.2. Switching model

The model, applicable to many topologies, describes the low-side MOSFET during turn-on and turn-off in a typical double-pulse test setup where an inductive load is connected across the high-side MOSFET [7]. It is assumed that the high-side transistor has been just turned off and its body diode continues to conduct the load current. In addition, it is assumed that the load current (I_L) is constant during the complete low-side impulse duration, i.e. turn-on and turn-off period. The mathematical model which defines the current-voltage relations of the MOSFET in the switching process is shown in Figure 1, with governing equations in Table 1.

Here R_G is the total (external and internal) resistance of the gate. For simplicity, most of the non-dominant inductive parasitic elements are omitted from the model. The parasitic inductance of the source (L_S) causes most of the oscillations and overshoots, while the parasitic inductance on the gate (L_G) for a conventional gate driver (CGD) typically does not cause voltage oscillations if designed properly.

Turn-on and turn-off both have distinct subintervals, i.e. stages $S_n = (1), (2) \ldots (8)$, as also depicted in Figure 2(a,b), respectively. The following is a model for MOSFET switching with asymmetric gate supply. Turn-on starts with a rising edge of a gate drive $u_{GG}(t)$ from U_{GN} to U_{GP}.

2.2.1. Turn-on delay

After the turn-on voltage is asserted, a delay takes place until the voltage rises to the U_{TH} and the MOSFET starts to overtake the current of its counterpart. Since

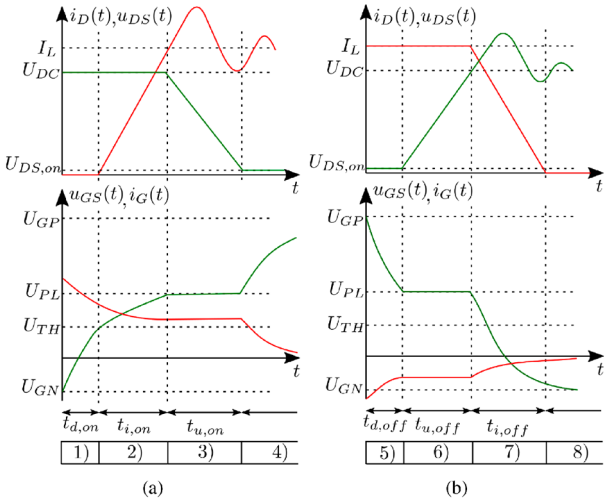

Figure 2. (a) Theoretical turn-on waveforms of with subintervals (1) to (4) and (b) theoretical turn-off waveforms for subintervals (5) to (8) showing drain-source voltage, drain current, gate-source voltage and gate current with corresponding interval durations. Current and voltage overshoots caused by reverse recovery current and parasitic inductances are shown but omitted from the model.

the drain-source voltage u_{DS} does not change, the parasitic capacitance C_{DS} can be viewed as a short circuit. Neglecting all parasitic inductances and the stated conditions, the solutions of the equations are:

$$u_{GS}(t) = (U_{GP} - U_{GN})\left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + U_{GN} \quad (8)$$

$$i_G(t) = \frac{U_{GP} - U_{GN}}{R_G}\,\mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \quad (9)$$

At the same time, $u_{DS}(t) \approx U_{DC}$, and the observed transistor current is still $i_D(t) \approx 0$. For a complex model, in which L_S is included, the gate voltage follows the envelope defined by (9), while any gate-source inductance causes high-frequency oscillations.

2.2.2. Current rise time

This subinterval starts when $u_{GS} \geq U_{TH}$, and ends when $u_{GS} = U_{PL}$ is valid. This coincides with drain current i_D rising to load current I_L. The transistor current takes over the complementary transistor's body diode current. The MOSFET is in the saturation region, and the channel current is determined by the transconductance while $u_{DS} > u_{GS} - U_{TH}$ is valid. If the drain inductance is ignored, the gate voltage continues to rise with the same conditions as before.

$$u_{GS}(t) = (U_{GP} - U_{TH})\left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + U_{TH} \quad (10)$$

$$i_G(t) = \frac{U_{GP} - U_{TH}}{R_G}\,\mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \quad (11)$$

$$i_D(t) \approx i_{CH}(t) = g_{fs}(u_{GS}(t) - U_{TH}) \quad (12)$$

Here $u_{DS}(t) \approx U_{DC}$ holds. Equation (12), i.e. channel current expression, follows from (7) if source parasitic inductance is ignored. The remaining loop inductances cause the drain-source voltage drop ($\Delta u_{DS} = L_\Sigma \cdot \mathrm{d}i_D/\mathrm{d}t$) if present or not ignored. The C_{GD} displacement current is zero if its voltage is unchanged (when $L_\Sigma \approx 0$). Due to the symmetry of the components, the current gradient ($\mathrm{d}i_D/\mathrm{d}t$) is equal to the current gradient of the opposing intrinsic diode [8]. A drain current overshoot due to reverse recovery is observed during this time if applicable.

2.2.3. Voltage fall time

Voltage fall starts when i_D becomes equal to the load current, and when $u_{GS} = U_{PL}$. It ends when u_{DS} falls to the ohmic voltage drop in conduction ($u_{DS} = R_{DS,on} \cdot I_L$). In this sub-interval, parasitic capacitances determine the voltage gradients. Due to the Miller effect, C_{GD} for this subinterval appears to be very large, so both the gate-source voltage $u_{GS} = U_{PL}$ and the gate current i_G are constant. The gate current drains the charge from the Miller capacitance C_{GD}. From the Equation (4) and previous considerations:

$$i_G(t) = \frac{U_{GP} - U_{PL}}{R_G} = I_G = const. \quad (13)$$

$$u_{DS}(t) = U_{DC} - \frac{U_{GP} - U_{PL}}{R_G C_{GD}} \cdot t \quad (14)$$

Because of high $\mathrm{d}u/\mathrm{d}t$ sensitivity to C_{GD}, this capacitor's value must be approximated as the mean of voltage-dependent capacitance $C_{GD}(u)$, as in [9].

$$C_{GDq} = \frac{\int_0^{U_{DC}} C_{GD}(u)\,\mathrm{d}u}{U_{DC}} \quad (15)$$

The effects of displacement currents flowing through both opposite C_{GD} and C_{DS} and observed transistor C_{DS} can be included in the model by utilizing (7), however, often $C_{GD}R_G \gg (2C_{DS} + C_{GD})/g_{fs}$ holds, so the influence of this effect can be neglected for turn-on transition.

Due to the symmetry of low and high-side transistors, their drain-source voltage gradients are equal but of opposite signs.

$$\left.\frac{\mathrm{d}u}{\mathrm{d}t}\right|_{on} = \frac{U_{GP} - U_{PL}}{R_G C_{GDq}} \quad (16)$$

Here it should be also noted that for CGD turn-on $\mathrm{d}u/\mathrm{d}t$ decreases linearly with increasing load current I_L due to Miller plateau voltage shifting up.

2.2.4. Gate voltage rise time

The gate voltage must rise to the terminal voltage U_{GP}, so the voltage and current curves continue from their previous values. The Miller capacitance C_{DS} is charged to the gate voltage, and no longer appears very large from driver side. The voltage u_{DS} is stabilized at the value $R_{DS,on} \cdot I_L$, while the current is stabilized at the value of the load current I_L.

$$u_{GS}(t) = (U_{GP} - U_{PL})\left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + U_{PL} \quad (17)$$

$$i_G(t) = \frac{U_{GP} - U_{PL}}{R_G} \, \mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \tag{18}$$

MOSFET turn-off can be viewed as the four previously mentioned time intervals in reverse order. The current-voltage relationships shown in (3)–(7) can still be applied.

2.2.5. Turn-off delay

Starts with the turn-off voltage (U_{GN}) appearing at the output stage of the gate drive, and lasts until the gate-source voltage drops to the plateau voltage (U_{PL}):

$$u_{GS}(t) = (U_{GN} - U_{GP}) \left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + U_{GP} \tag{19}$$

$$i_G(t) = \frac{U_{GN} - U_{GP}}{R_G} \, \mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \tag{20}$$

During this subinterval, $u_{DS}(t) \approx R_{DS,on} \cdot I_L$ holds true, and the observed transistor current is still $i_D(t) \approx I_L$.

2.2.6. Voltage rise time

In this subinterval, the voltages of the commutation loop change with the Miller effect. Analogous to the voltage fall time interval, for a large enough current, the following applies:

$$i_G(t) = \frac{U_{GN} - U_{PL}}{R_G} = I_G = const. \tag{21}$$

$$u_{DS}(t) = -\frac{U_{GN} - U_{PL}}{R_G C_{GD}} \cdot t \tag{22}$$

However, this voltage gradient model is valid for load currents above a transistor-specific kink current I_k [2], where voltage rise time becomes less dependent on load current. On the contrary, for currents lower than I_k, the sum of currents in (7) are such that $i_{CH} = 0$, and all of the load current I_L distributes to charge all of the parasitic capacitances. This type of switching is essentially lossless and typically called ZVS in literature [2, 9].

$$\left.\frac{\mathrm{d}u}{\mathrm{d}t}\right|_{off} = \begin{cases} \dfrac{U_{PL} - U_{GN}}{C_{GDq} R_G} \cdot \dfrac{I_L}{I_k} & \text{if } I_L < I_k \\ \dfrac{U_{PL} - U_{GN}}{C_{GDq} R_G} & \text{if } I_L \geq I_k \end{cases} \tag{23}$$

For load currents larger than I_k during turn-off, the portion of load current is flowing to the channel as well, instead of only charging both C_{OSS} capacitances. Therefore, using (7), boundary condition is when $I_L = 2C_{OSS} \cdot \mathrm{d}u/\mathrm{d}t$, and I_k can be found as:

$$I_k = 2C_{OSSq} \left.\frac{\mathrm{d}u}{\mathrm{d}t}\right|_{I_L=0} \tag{24}$$

It should also be noted that, analogous to C_{GDq}, a charge-equivalent capacitance using (15) needs to be calculated for C_{OSS}.

2.2.7. Current fall time

Starts when $u_{GS} < U_{PL}$ and is valid until $u_{GS} = U_{TH}$, that is, until the drain current i_D drops to 0 A. The MOSFET is in the saturation region.

$$u_{GS}(t) = (U_{GN} - U_{PL}) \left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + U_{PL} \tag{25}$$

$$i_G(t) = \frac{U_{GN} - U_{PL}}{R_G} \, \mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \tag{26}$$

$$i_D(t) \approx i_{CH}(t) = g_{fs}(u_{GS}(t) - U_{TH}) \tag{27}$$

If stray inductances are not ignored, an overshoot is seen on drain-source voltage u_{DS}.

2.2.8. Gate voltage fall time

The gate voltage must drop to the terminal voltage U_{GN}, continuing with the current-voltage relations of the previous interval, with the current $i_D(t) = 0$.

$$u_{GS}(t) = (U_{GN} - U_{TH}) \left(1 - \mathrm{e}^{\frac{-t}{R_G C_{ISS}}}\right) + (U_{TH}) \tag{28}$$

$$i_G(t) = \frac{U_{GN} - U_{TH}}{R_G} \, \mathrm{e}^{\frac{-t}{R_G C_{ISS}}} \tag{29}$$

Therefore it is possible to calculate the approximate current and voltage rise and fall times during turn-on and turn-off (according to [10]) and from this follows the Table 2 in which $\tau = R_G C_{ISS}$. From these results, it is possible to estimate the losses and EMI of the converter.

3. Fundamental EMI analysis for a half-bridge

According to the considerations from the previous chapter, it is possible to achieve switching gradients of up to 100 V/ns. However, the high switching speed increases EMI. From a practical standpoint, EMI generated by power converters is divided into conducted emissions, transmitted by a conductor leads and radiated emissions, transmitted to the surrounding space.

Conducted EMI can be further divided into differential mode (DM) and common mode (CM) interference [11].

- DM noise pair appears on both of the bus lines of the DC-link in counter-phase (U_{DC+} and U_{DC-}). It is caused by the current through the commutation loop, i.e. path from the DC-link capacitor through one of the semiconductor switches to the load and back to the DC-link and are caused by current gradients.
- CM noise appears in-phase in both bus lines (U_{DC+} and U_{DC-}). It is created by the dielectric displacement current ($C\mathrm{d}u/\mathrm{d}t$) through the parasitic capacitances, for example, from transistor to heatsink i.e. towards the earthing or device housing.

Because power electronics converters are inherently pulsed devices, certain parts of the commutation loop

Table 2. Approximate duration of SiC MOSFET switching subintervals.

S_n	Condition	Duration	
(1)	$U_{GN} \leq u_{GS} < U_{TH}$	$t_{d,on} = \tau ln(\frac{U_{GP}-U_{GN}}{U_{GP}-U_{TH}})$	(30)
(2)	$U_{TH} \leq u_{GS} < U_{PL}$	$t_{i,on} = \tau ln(\frac{g_{fs}(U_{GP}-U_{TH})}{g_{fs}(U_{GP}-U_{TH})-I_L})$	(31)
(3)	$u_{GS} = U_{PL}$	$t_{u,on} = \frac{U_{DC}C_{GDq}R_G}{U_{GP}-U_{PL}}$	(32)
(4)	$U_{PL} < u_{GS} \leq U_{GP}$	$t \to \infty$	
(5)	$U_{PL} < u_{GS} \leq U_{GP}$	$t_{d,off} = \tau ln(\frac{U_{GN}-U_{GP}}{U_{GN}-U_{PL}})$	(33)
(6)	$u_{GS} = U_{PL}, I_L \geq I_k$	$t_{u,off} = \frac{U_{DC}C_{GDq}R_G}{U_{PL}-U_{GN}}$	(34)
(6)′	$u_{GS} = U_{PL}, I_L < I_k$	$t'_{u,off} = \frac{U_{DC}C_{GDq}R_G}{U_{PL}-U_{GN}} \cdot \frac{I_k}{I_L}$	(35)
(7)	$U_{TH} \leq u_{GS} < U_{PL}$	$t_{i,off} = \tau ln\left(\frac{g_{fs}(U_{GN}-U_{TH})-I_L}{g_{fs}(U_{GN}-U_{TH})}\right)$	(36)
(8)	$U_{GN} \leq u_{GS} < U_{TH}$	$t \to \infty$	

(mainly the switch node) have pulsed currents and voltages with finite rise and fall times. Therefore, it is important to analyse the spectrum resulting from the trapezoidal waveform. Using Fourier transform of a trapezoidal waveform with amplitude A, rise time τ_r and duty cycle τ_d, magnitude and phase of nth harmonic are obtained (37), with switching frequency, f_s, being the fundamental harmonic [12]:

$$c_n = A\tau_d f_s \frac{\sin(n\pi\,\tau_d f_s)}{n\pi\,\tau_d f_s} \frac{\sin(n\pi\,\tau_r f_s)}{n\pi\,\tau_r f_s} e^{jn\pi f_s(\tau_d+\tau_r)} \quad (37)$$

It is assumed that the voltage rise time is equal to the fall time. By taking the envelope of the spectrum, i.e. taking the absolute value, converting to decibels and using the limiting value of $\sin(x)/x$, it can be seen that the cutoff frequencies above which -20 dB/dec term is active are:

$$f_{c1} = nf_s = \frac{1}{\tau_d \pi} \quad (38)$$

$$f_{c2} = nf_s = \frac{1}{\tau_r \pi} \quad (39)$$

By shortening the rise time, the term with τ_r shifts the second cutoff frequency higher, resulting in an increase of 20 dB/dec for a band above f_{c2}, as observed in Figure 3.

According to the above consideration, the linear dependence of the noise bandwidth on rise and fall times is visible. Furthermore, this implies a possible trade-off between switching losses and the permissible EMI by the relevant standards [1].

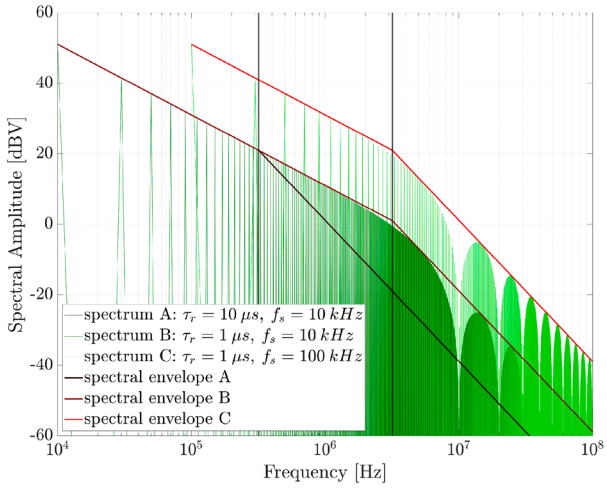

Figure 3. Spectrum of a trapezoidal voltage with τ_r and f_s as parameters, and signal amplitude $A = 560$ V with cutoff frequencies f_{c1} and f_{c2} highlighted.

4. Comparative analysis of advanced gate drivers

4.1. Gate drivers for SiC MOSFETs

Gate drivers for SiC MOSFETs mostly use an isolated DC/DC converter as an asymmetric voltage source and are driven with CMOS or bipolar push-pull outputs to which the gate resistor is connected. Many of the methods shown in Figure 4 point out that switching can be further optimized. As mentioned before, by controlling the gate voltage u_{GS} and the current i_G, it is possible to control du/dt and di/dt, and thus the switching losses, and EMI.

4.1.1. Conventional gate drive (CGD) for SiC MOSFETs

Conventional methods that use a fixed driver stage can be divided into those with symmetric and asymmetric external gate resistance. In SiC MOSFETs, switching with symmetrical (i.e. single resistor for turn-on and turn-off) is rarely used due to poor performance. Different gate resistors allow for greater adaptability of the gate drive. Typically, it takes longer to reach the first turn-off subinterval than the first turn-on subinterval because of the asymmetric power supply. For this reason, and to prevent erroneous turn-on caused by the Miller effect, the turn-off resistance is typically smaller than the turn-on resistance. Different resistance can be achieved utilizing a diode connected to the gate or by split push-pull output [13].

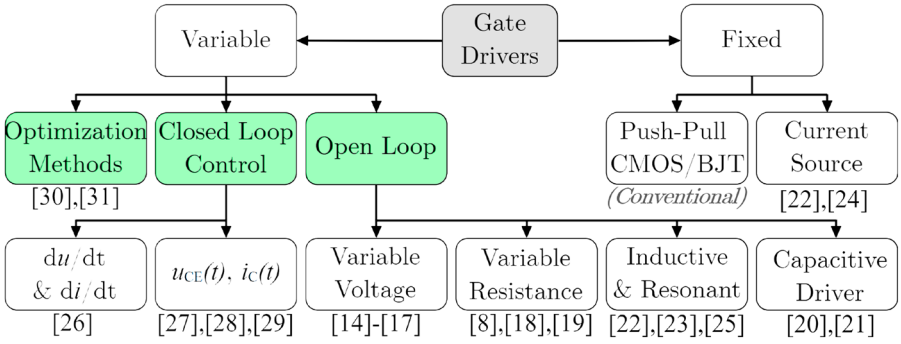

Figure 4. Classification of previously demonstrated gate drives for SiC MOSFET and IGBT with main AGD groups highlighted.

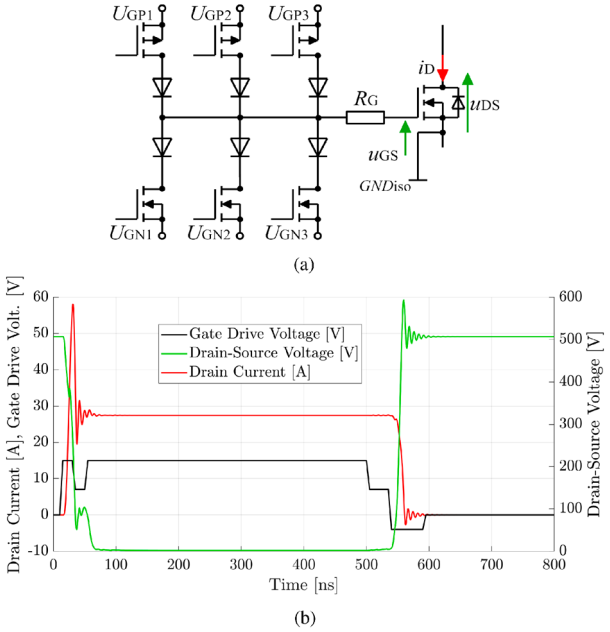

Figure 5. (a) Generalized voltage-fed AGD and (b) simulated characteristic waveforms for turn-on and turn-off. Middle voltage $U_{mid} = 7\,\text{V}$ lasting for 15 ns during turn-on and 35 ns during turn-off. Resulting rising and falling voltage gradients shown are 10 V/ns and 17 V/ns respectively for 25 A inductive clamped load. Simulation is performed in LTSpice using Wolfspeed C3M0065100K MOSFET.

4.1.2. Voltage-fed AGD

In this category, a predefined voltage profile is applied to the gate of a MOSFET. Waveforms for these methods are generalized in Figure 5(b), with a schematic in Figure 5(a).

In [14], a gate drive using four voltage levels was proposed. An ASIC is used to drive the logic of an H-bridge connected to the gate and source. The gate voltage is set to the absolute maximum during turn-on, then reduced to the recommended voltage after 400 ns. During turn-off, the voltage returns to 0 V after the complementary transistor turns on, resulting in a faster turn-on. The method reduces losses by 10%, but increases $\mathrm{d}u/\mathrm{d}t$.

In [15], a similar method is presented that uses an auxiliary circuit triggered by power stage conditions to reduce voltage and current gradients during turn-on and turn-off. The gate voltage is reduced to minimize losses and shorten the turn-on delay time. A comparator is triggered by the parasitic inductance of the source to reduce the output voltage, and after a defined delay time, the output voltage returns to the standard value. This process is reversed during turn-off, reducing overshoot and EMI. Compared to CGD, current overshoot is reduced twofold and voltage overshoot by 68% for the same turn-on losses.

In [16], a described method uses multiple voltage levels only during turnoff. A positive intermediate voltage is used, which can temporarily put the transistor in the saturation region, depending on the set level. The operating principles are similar, with predefined instances of setting the medium voltage level and returning to the allowed negative voltage. However, the method requires additional care due to the effect of threshold voltage reduction with increasing temperature.

The method described in [17] uses voltage-fed AGD to characterize and extract the SiC MOSFET switching parameters. It uses multiple gate drives between multiple voltage rails. The control logic is on the primary side, while the level-shifting is executed through signal isolators. The results are arranged in maps as it will be done in this paper, however, different variables are evaluated, such as overshoot voltage, and no optimization nor other influences is used to determine the optimum mid-level voltage time.

4.1.3. Variable resistance gate driver

Similar to the aforementioned, all resistive methods aim to reduce voltage and current gradients and accelerate transients in the remaining subintervals of the switching, and as such can be seen in Figure 6(b), with schematic in Figure 6(a).

A broadly applicable method described in [18] changes the gate resistance in four stages and reduces current overshoot from 50% to 20%, with lower switching losses by 18%. In turn-on and turn-off, it utilizes initial and final values of $R_G < 5\,\Omega$ and $R_G > 20\,\Omega$ during switching transients. Using the drain-source voltage divider and the shunt in the source, the current and voltage are measured and used to trigger resistance

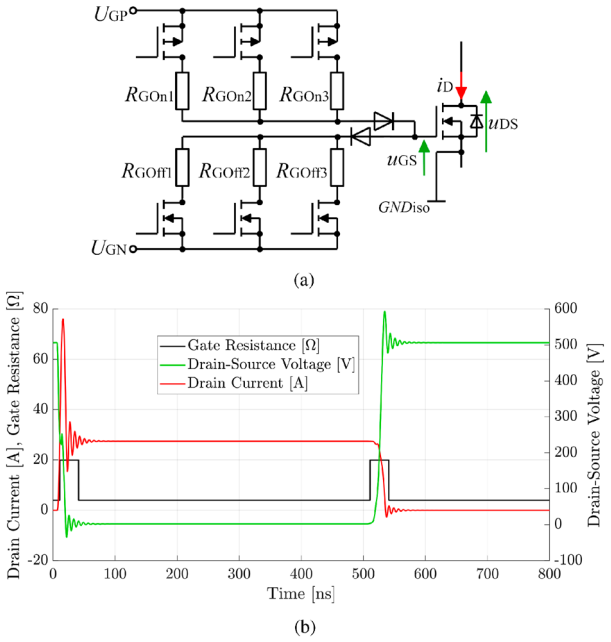

Figure 6. (a) Generalized variable resistance gate driver and (b) simulated response for turn-on and turn-off, $R_G = 4\,\Omega$ and $R_G = 20\,\Omega$, with increased resistance lasting 30 ns during rise and fall times. Resulting rising and falling voltage gradients shown are 10 V/ns and 12 V/ns respectively for 25 A inductive clamped load. Simulation is performed in LTSpice using Wolfspeed C3M0065100K MOSFET.

switchover, with triggering reference values also being adjustable with a DA converter.

The method described in [19] uses two resistance levels for turn-on and turn-off and is measuring u_{GS}, using it as feedback to adjust the switching trajectory using comparators. In right conditions, the method reduces $\mathrm{d}i/\mathrm{d}t$ from 53.2 A/µs to 12.3 A/µs and $\mathrm{d}u/\mathrm{d}t$ from 4.8 kV/µs to 3.2 kV/µs , while simultaneously increasing losses by approximately 12%. This method can be improved by dynamically changing the comparator thresholds as favourable operating conditions occur for a narrow operating point range.

The method [8] has current feedback using a shunt connected to the source. The method uses main and two auxiliary resistors, where one of the auxiliary resistors assists during turn-on, and the other during turn-off during current and voltage rise times. The time intervals in which the additional resistors will be turned on are defined with thresholds that, depending on the current, are changed by the DA converter. The method successfully reduces the voltage overshoot from 50% to 21% with an increase in turn-off losses from 8 mJ to 10 mJ.

4.1.4. Capacitor-assisted active gate drivers

Krishna and Hatua [20] describe a method for turning on and off a SiC MOSFET using three p-channel and three n-channel MOSFETs to indirectly control the charge injected into the gate. There are three complementary stages during turn-on and turn-off. The first transistor is used as a current source, the second as a capacitive impulse charge, and the third transistor completes the turn-on. The method prolongs $\mathrm{d}u/\mathrm{d}t$ by 60% and reduces overshoot peak from 600 V to 500 V.

In [21] method for faster turn-off using an auxiliary capacitor to decrease the time spent in Miller's plateau is proposed. The MOSFET is first turned on through a single gate resistor, after which the second one is added in parallel. In turn-off, the gate is discharged with a current spike through a capacitor after which a Miller clamp is turned on. The method reduces turn-on losses by 12%, but may not be efficient beyond the design operating point.

4.1.5. Resonant SiC MOSFET gate drives

Resonant drivers contain inductors connected to the gate which are current-biased and improve the speed of gate charging.

One of the proposed resonant methods evaluates the temperature dependence of MOSFET parameters [22]. The method uses the peak gate current $i_g(t)$ as temperature detection. The resonant gate drive is composed of an H-bridge with an air-core inductor. The circuit precharges the coil by connecting it between supply rails. Then low-side transistor is turned off with an inductor discharging through the gate in on-state, another high-side transistor pulls the gate to the positive rail. The inductor is then negatively pre-charged (mirror-symmetrical to turn-on) for turn-off and later clamped to negative rail. The method has been validated only on low DC link voltage.

Method described in [23] uses a p and n-channel pair with a diode-inductor connection between them. One end of the inductor is also connected to the gate of the SiC MOSFET. In turn-on, the p-channel driver turns on, while the n-channel driver delays its turn-off, pre-charging the inductor. After a predetermined delay, the n-channel MOSFET turns off and the inductor discharges to the gate. By natural commutation, the current of the inductor drops to zero. The turn-off clamps the gate and source with an n-channel transistor. The method was tested on a boost converter with output voltages 600 V and 800 V. The switching losses were reduced by 20%, while the current rise time was shortened from 15 ns to 7.5 ns. A common disadvantage of resonant gate drive is the inherent lengthening of the dead time, which introduces a delay in the control loop.

4.1.6. Current source gate drivers

Second method introduced in [22] and method [24] use controlled but unadjustable current mirrors during turn-on. A pair of p-channel MOSFETs or PNP BJTs are connected to the positive rail and used as current sources. The disadvantage of the method is the difficulty of achieving symmetrical switching of the SiC MOSFET, as a current sink is also required for this.

Thus, only a turn-on is often realized, while the turn-off uses a single pulldown to a negative voltage or 0 V. However, Pilli et al. [24] show improvements in terms of shorter turn-on delay times, which expands the bandwidth of a main control loop. For increased turn-off losses of 40% and increased turn-on losses of 28% there is a decrease in du/dt in turn-off by 65% and di/dt in turn-on of 45%.

Additionally, the variable current source method described in [25] uses inductive components in an H-bridge-like topology with an auxiliary leg to pre-charge and release the gate current while limiting the oscillatory behaviour of the gate loop. The method is able to produce two gate current pulses, which aims to decouple du/dt from di/dt control. The method reduced the switching losses, but it increased di/dt. The main application are dead-time sensitive topologies like dual-active bridge, as it reduces turn-on and turn-off delay times.

4.2. Advanced and closed loop IGBT gate drivers

Since the IGBT is a mature semiconductor technology, the most advanced active switching methods are more developed than for SiC MOSFETs. An additional advantage is lower switching speed, which makes it significantly easier for IGBTs to achieve closed-loop control. Below is an overview of methods that have been developed exclusively for IGBTs.

4.2.1. Gate drives for IGBT with closed loop du/dt and di/dt control

The most advanced methods control the du/dt and di/dt in a closed loop, with step-functions as the references of gradients. The [26] method uses mostly analogue control and it assumes that di/dt is zero during voltage rise and fall times. This enables a common control loop for current and voltage gradients with an analogue PI controller. The method was validated on IGBT modules and when compared to a CGD a reduction of turn-on losses by 2.15 times and turn-off losses by 2.11 times were seen, with du/dt increasing 4 times.

4.2.2. Drivers with real-time trajectory management

Due to parameter variability (temperature, load current, etc.), method [27] uses adaptive real-time switching control on an FPGA, where a parametric lookup table (LUT) for the gate voltage sequence is used. Individual switching stages are detected by a comparator circuit. A DA converter sets the current source reference. Adaptive control uses a signum algorithm optimization.

The [28] method uses voltage drive as in Figure 5(a), but with 64 possible voltage levels in 60 time slots. This switching sequence is then prepared in the FPGA every second. An external device measures and evaluates the output currents and voltages of the IGBT and determines the next switching sequence with the optimization algorithm adaptable to parameter changes. The method reduces switching losses up to 42%, using voltage overshoot as a constraint variable.

A method similar to the previous, but utilizing 64 current sources is likewise applied to IGBT and uses in-the-loop optimization with a particle-swarm algorithm, however, it requires high performance hardware such as PC to run optimization during converter operation [29].

4.3. Optimization methods for SiC MOSFET switching

The methods which feature variously applied optimization techniques in different scenarios are the current state-of-the-art. The basic method described in [30] uses the four-level active gate drive with continuously adjustable gate voltages. It extracts datasheet parameters to optimize for du/dt, di/dt and switching losses. However, it does not utilize the variability of mid-level time, but rather mid-level voltage only, which limits its controllability range. Also, the method does not vary its parameters regarding load current or DC-link voltage and would greatly benefit from the improved model by using real test values, as neither parasitic elements nor device-to-device variations are accounted for in the datasheet. As the method is not compared to the results of conventional gate drive, it is difficult to evaluate its effectiveness.

Today's most advanced method has been presented in [31]. It uses artificial neural networks (ANN) with variable gate resistances to optimize the active gate drive. A neural network is trained offline with a recorded dataset, and the ANN outputs a mid-level resistance duration depending on external circuit parameters. The method yields 25% lower average du/dt for the same switching losses but requires a large dataset for training and the control in the low current range is very limited.

5. Switching optimization with an AGD

The most prevalent active gate driving methods use either variable voltage or variable resistance. The reason is the similarity to the conventional gate drive, as the logical progression to adding complexity is typically adding one more level of either voltage or gate resistance during turn-on or turn-off. As seen in the previous chapter, gate drivers are commonly voltage sources with external gate resistances for turn-on and turn-off, models of which are well-known and have been studied thoroughly. For the selected gate drive topology, voltage-fed AGD with separate U_{mid} levels for turn-on and turn-off is selected to be further examined. This is because current source drivers typically introduce a delay or have drive strength or bandwidth issues [32],

while other topologies require a deeper understanding of their influence on the switching process in all modes of converter operation, including failures. Due to the relatively simple output stage and more straightforward component selection, which do not feature energy storage, it is uncomplicated to envisage voltage-fed AGD usage in power converters both at discrete and IC levels.

Considering the findings in the previous chapters, a gate voltage profile can be optimized for every switching event. This means that the part of the EMI spectrum on which the gate drive has influence is kept constant under every switching condition regardless of load current (I_L), semiconductor temperature, etc. It will later be shown that since E_{on} and E_{off} are monotonically increasing functions, the optimum switching will be achieved for the shortest possible mid-level time (t_{mid}). To generalize this problem, it is possible to map out all of the possible switching sequences for a certain active gate drive. If the half-bridge observed is symmetrical, i.e. uses the same transistor for the high and low sides, then also mapping a single direction of current is sufficient to find all of the possible switching states. For the reverse current direction, the diagonally opposite diode and transistor pair commutate, however, the switching events remain the same.

5.1. Methodology of gate drive mapping

As Section 2 has shown, for a given transistor, its $\mathrm{d}u/\mathrm{d}t$ is dependent on the half-bridge load current, gate resistance, and the injected gate voltage. Furthermore, gate voltage shaping has yielded favourable results in previous works [28]. For the context of this paper, gate voltage threshold temperature dependency will be ignored, however, this additional parameter can be included in a physical setup. If a "pre-mapping" of a switching device exists, then an optimum voltage sequence can be generated at the gate given the power stage conditions i.e. load current and required $\mathrm{d}u/\mathrm{d}t$.

To confirm the validity of this concept, a simulation framework that generates maps of the $\mathrm{d}u/\mathrm{d}t$ versus load current I_L and various gate voltage sequences during turn-on and turn-off was implemented. The mapping is achieved through a MATLAB script which executes LTSpice as a simulation tool with an appropriate gate drive voltage sequence. For each load current condition i.e. from 0 to rated and for each voltage level and each voltage-level duration, a piece-wise linear (PWL) file is generated and Spice simulation is started by a command prompt batch file. The simulation performs a single pulse test with a current source as a load. After the Spice simulation converges, the output file is read back to MATLAB where $\mathrm{d}u/\mathrm{d}t$ during both turn-on and turn-off is read as rise time. The turn-on or turn-off switching energy are calculated from the results of the same simulation as (40) and (41):

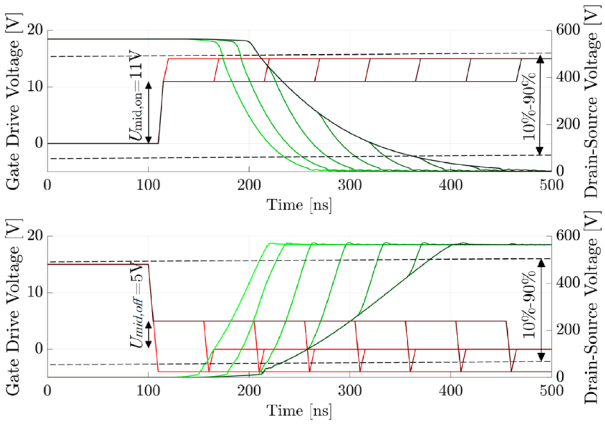

Figure 7. Gate voltage sequences: u_{GG} and u_{DS} for turn on and turn-off. Displays simulated signal shaping and t_{mid} duration influence on $\mathrm{d}u/\mathrm{d}t$ for IMZ120R045M1. The mid-level gate drive voltages are $U_{mid,on} = 11\,\mathrm{V}$ and $U_{mid,off} = 5\,\mathrm{V}$. The selected duration t_{mid} ranges from 0 to 350 ns in 50 ns increments. Simulation is performed with $R_G = 33\,\Omega$, and with load current of 14 A.

$$E_{on} = \int_0^{t_{on}} i_D(t) \cdot u_{DS}(t)\,\mathrm{d}t \tag{40}$$

$$E_{off} = \int_0^{t_{off}} i_D(t) \cdot u_{DS}(t)\,\mathrm{d}t \tag{41}$$

Since the sampling time of the Spice tool is variable, the points are linearly interpolated to a sample time of 1 ns. The $\mathrm{d}u/\mathrm{d}t$ values are taken as average on a time interval from 10% to 90% of DC-link voltage. After the calculation, the results are saved to a map and a new simulation is started with the next circuit parameters and a new gate voltage profile PWL file. The resulting map is a discrete function of two variables $\mathrm{d}u/\mathrm{d}t = f(I_L, t_{mid})$ with gate resistance R_G, mid-level gate voltage U_{mid} and voltage sequence type as a parameter. In this paper, two sequences were examined, namely "pullback-like" (as in Figure 5(b)), and "staircase-like" sequences (as in Figure 7). In each examined case, the DC-link voltage was set to 560 V. To enhance global convergence, the simulation circuit excludes external parasitic elements, such as commutation loop inductances, because they do not affect $\mathrm{d}u/\mathrm{d}t$, but rather influence $\mathrm{d}i/\mathrm{d}t$, justifying their omission. As Figure 7 suggests, the drain-source voltage of a transistor, and therefore half-bridge AC node, is broken in two distinct sections, i.e. section during t_{mid} with low $\mathrm{d}u/\mathrm{d}t$, and section after t_{mid} with high $\mathrm{d}u/\mathrm{d}t$, for both turn-on and turn-off.

5.2. Direct maps

To optimize the switching, both turn-on and turn-off $\mathrm{d}u/\mathrm{d}t = f(I_L, t_{mid})$ maps need to be examined. Since the plateau voltage varies with current, is temperature-dependent and varies for turn-on and turn-off [6].

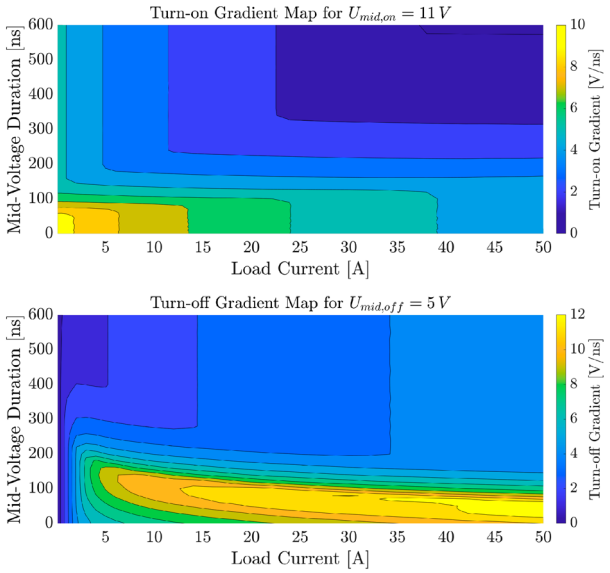

Figure 8. A contour plot of direct $du/dt = f(I_L, t_{mid})$ maps for turn-on and turn off of Infineon IMZ120R045M1 SiC MOSFET in half-bridge. DC-link voltage used is 560 V. External $R_G = 33\,\Omega$ is used to provide a balance of controllability and achievable time resolution. Gate time constant is $\tau = 70$ ns. A high-sensitivity area can be observed for a range of $t_{mid} = 100$ ns to 200 ns. Voltages of $U_{mid,on} = 11$ V and $U_{mid,off} = 5$ V are selected from a set of maps to optimize between controllability and losses. Similar results were obtained for Cree C3M0065100K SiC MOSFET.

Turn-on and turn-off events were mapped with different U_{mid} voltages in the appropriate range for possible Miller plateau levels (this is transistor-dependent). The reasoning behind R_g and U_{mid} selection will be explained in the upcoming subsection. The resulting maps are shown in Figure 8. Examining the two different sequences (i.e. "pullback" and "staircase"), the "staircase" sequence was selected because of its straightforward hardware realization, safety (no re-turn off is possible after the current commutation) and a lack of additional timing parameters (peak-gate voltage duration before "pullback").

5.3. Map inversions and optimum switching time

Optimum switching requires knowing the exact mid-voltage (U_{mid}) pulse duration (t_{mid}) and its value given the current condition and required du/dt. The goal is to minimize switching energy for turn-on and turn-off while keeping du/dt as constant as possible. To obtain the inverted map, i.e. $t_{mid} = f(I_L, du/dt)$ the direct maps need to be restricted to their monotonic intervals. This is because an inverse of a function exists if and only if each input point corresponds to a single unique output point (bijective function).

For both turn-on and turn-off, the area for which the function is defined (i.e. domain) is bounded by two curves. This is also the area where du/dt can be controlled, and has to be taken into consideration. This is the controllability area and is the domain of the inverted function $\mathcal{D}(f(I_L, du/dt))$ and can be bounded by four lines for turn-off, and two for turn-on.

5.3.1. Turn-on area of controllability

The area in which turn-on gradient can be controlled is bounded by two curves. The upper bound is defined by the expression (42), and corresponds to du/dt when t_{mid} is too short to influence the switching. For this case, mid-level voltage is shorter than turn-on delay, i.e. $t_{mid} < t_{d,on}$ holds.

$$\left.\frac{du}{dt}\right|_{on,AGD1} = \frac{U_{GP} - U_{PL}}{R_G C_{GDq}} \tag{42}$$

The lower bound is defined by the relation (43). In this case t_{mid} lasts longer than Miller plateau time, and $t_{mid} > t_{u,on}$ holds.

$$\left.\frac{du}{dt}\right|_{on,AGD2} = \begin{cases} \dfrac{U_{mid,on} - U_{PL}}{C_{GDq} R_G} & \text{if } U_{PL} < U_{mid,on} \\ 0 & \text{if } U_{PL} \geq U_{mid,on} \end{cases} \tag{43}$$

5.3.2. Turn-off area of controllability

For turn-off, non-linear curves are approximated as piecewise linear lines, as in (23). The upper bound of the area of controllability is defined by (44) and corresponds to the du/dt curve when t_{mid} is too short to influence the switching. Here $t_{mid} < t_{d,off}$ holds.

$$\left.\frac{du}{dt}\right|_{off,AGD1} = \begin{cases} \dfrac{U_{PL} - U_{GN}}{C_{GDq} R_G} \cdot \dfrac{I_L}{I_{k1}} & \text{if } I_L < I_{k1} \\ \dfrac{U_{PL} - U_{GN}}{C_{GDq} R_G} & \text{if } I_L \geq I_{k1} \end{cases} \tag{44}$$

Conversely, the lower bound of the area of controllability is defined by the curve (45). In this case, t_{mid} lasts longer than Miller plateau time, and AGD can no longer influence du/dt in switching. Here $t_{mid} > t_{u,off}$ holds.

$$\left.\frac{du}{dt}\right|_{off,AGD2} = \begin{cases} \dfrac{U_{PL} - U_{mid,off}}{C_{GDq} R_G} \cdot \dfrac{I_L}{I_{k2}} & \text{if } I_L < I_{k2} \\ \dfrac{U_{PL} - U_{mid,off}}{C_{GDq} R_G} & \text{if } I_L \geq I_{k2} \end{cases} \tag{45}$$

For both cases, currents I_{k1} and I_{k2} can be calculated as:

$$I_{k1} = 2 \cdot \frac{U_{th} - U_{GN}}{C_{GDq} R_G} C_{OSSq} \tag{46}$$

$$I_{k2} = 2 \cdot \frac{U_{th} - U_{mid,off}}{C_{GDq} R_G} C_{OSSq} \tag{47}$$

Inverted maps in Figures 9 and 10 were obtained using a search algorithm. Before, upper and lower boundaries were set to limit the search to a controllable area. In practice, a 2D cross-section of the direct map was found first and the longest monotonic sequence was extracted from it to obtain the search boundaries. Then, an optimum point for which

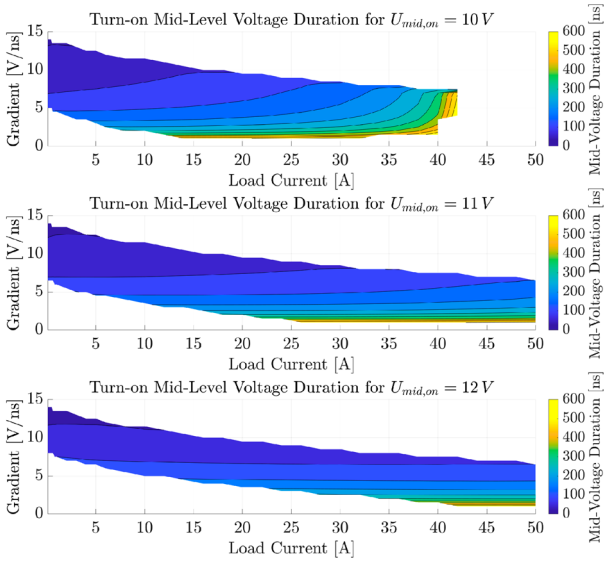

Figure 9. A contour plot of inverted $t_{mid} = f(I_L, \mathrm{d}u/\mathrm{d}t)$ maps for turn-on with $U_{mid} = 10, 11$ and 12 V, and for $R_G = 33\,\Omega$. The controllability area is maximized for $U_{mid} = 11$ V. A tradeoff exists between the area of controllability and total losses. The highest difference is seen for large drain currents.

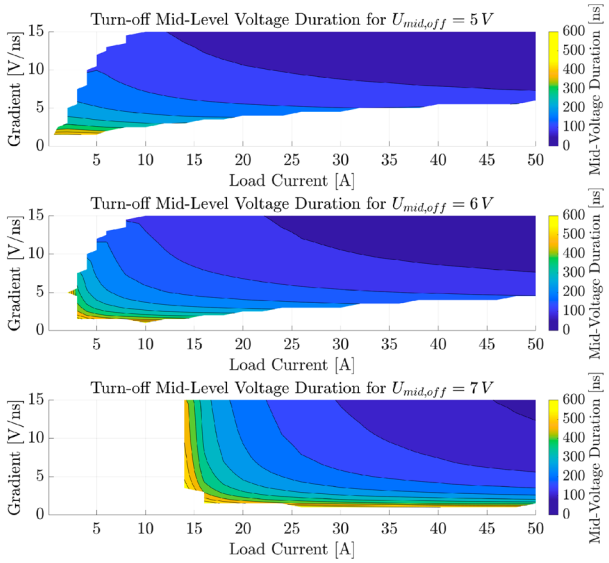

Figure 10. A contour plot of inverted $t_{mid} = f(I_L, \mathrm{d}u/\mathrm{d}t)$ maps for turn-off $U_{mid} = 5, 6$ and 7 V and for $R_G = 33\,\Omega$. The area of controllability is maximized for $U_{mid} = 6$ V, however, lower losses are achieved for $U_{mid} = 5$ V. Controllability is severely limited for $U_{mid} \geq 7$ V.

$min\{(\mathrm{d}u/\mathrm{d}t)^2 - (\mathrm{d}u/\mathrm{d}t)^2_{new}\}$ is satisfied is found with sequential quadratic programming method, which yields a single inverted map point. The algorithm is repeated for all $(\mathrm{d}u/\mathrm{d}t)_{new}$ and I_L vector points.

5.4. Gate resistor and mid-voltage selection

From Equations (42)–(45) it can be seen that R_G greatly influences the area of controllability. In general, gate resistance for AGD must be selected low enough so that it does not limit the upper bounds of controllability and can achieve fast enough $\mathrm{d}u/\mathrm{d}t$ for shortest t_{mid} times, Also, gate resistance needs to be high enough to allow for achievable t_{mid} time resolutions to influence switching in a physical setup using FPGA (for example in around nanosecond range), though for SiC devices, typical C_{ISS} is in the range of 1 nF up to 100 nF for large modules, which yields controllable gate time constants.

Additionally, to improve the overall EMI performance of AGD further, the R_G for AGD needs to be empirically in the range of 30% to 60% of the CGD R_G needed for the required $\mathrm{d}u/\mathrm{d}t$ to minimize the slope of individual $\mathrm{d}u/\mathrm{d}t$ pieces (Figure 7).

To minimize losses, U_{mid} has to be selected so that it is as low as possible for turn-off and as high as possible for turn-on, while $\mathrm{d}u/\mathrm{d}t$ is still controllable for the required current range.

5.5. Switching losses

For CGD, losses can be estimated according to [33]:

$$E_{on} = \frac{1}{2}\left(t_{u,on}\left(I_L + \frac{2C_{OSSq}U_{DC}}{t_{u,on}}\right)U_{DC} + t_{i,on}U_{DC}I_L\right) + E_{rr} \tag{48}$$

$$E_{off} = \frac{1}{2}\left(t_{u,off}\left(I_L - 2\frac{C_{OSSq}U_{DC}}{t_{u,off}}\right) + t_{i,off}U_{DC}I_L\right) \tag{49}$$

Where E_{rr} are losses due to reverse recovery. Relationship between $t_{u,on}$ and t_{mid} is non-linear, however since it is monotonic for observed mid-level times, the optimum switching strategy is to select the lowest possible t_{mid} which yields selected $\mathrm{d}u/\mathrm{d}t$, for example 5 V/ns. This way losses are minimized in every switching cycle. As switching energy is also calculated alongside $\mathrm{d}u/\mathrm{d}t$ values, it is arranged for turn-on and turn-off in a map as depicted in Figure 11 as well. The figure also highlights the optimum switching trajectory for constant 5 V/ns gradient.

6. Experimental verification

To verify the findings from the previous chapter, a special test setup has to be designed. Since no commercial gate driver allows for slope shaping by dynamically changing t_{mid} and U_{mid} in both turn-on and turn-off events, Infineon 1ED3890 was selected as an appropriate IC for turn-off gradient control only. The device settings are reconfigurable through I2C, where turn-off t_{mid} can be reconfigured in 250 ns steps analogous to waveforms in Figure 7. In addition, the test fixture was developed in a half-bridge configuration with the possibility of interchanging the gate drive PCBs for further research. The current measurement was performed with PEM CWT1 Rogowski coil, and the voltage measurement was made using two Tektronix

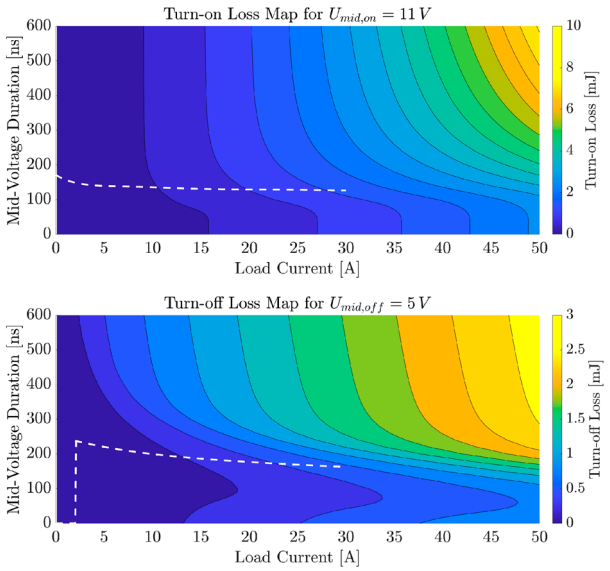

Figure 11. Switching loss map $E = f(I_L, t_{mid})$ of IMZ120R045M1 with optimum switching path for currents up to 30 A highlighted. For turn-off, AGD affects switching above 2.5 A for any combination of R_G and $U_{mid,off}$.

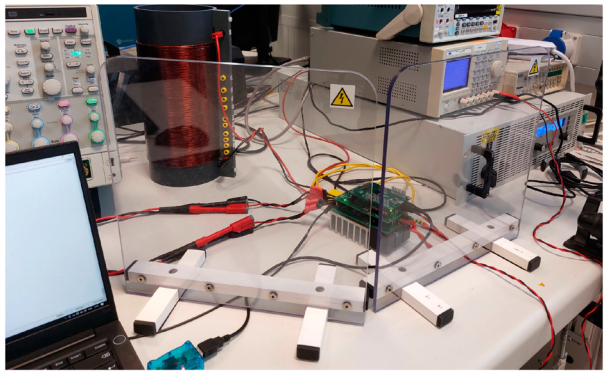

Figure 12. Test setup for experimental verification of direct maps, consisting of HVDC source, 700 µH inductor and PC with UART communication to main MCU for test parametrization.

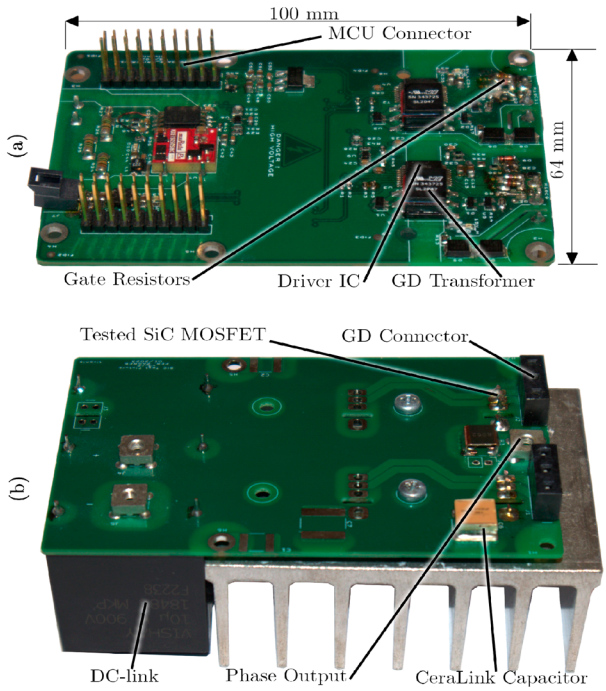

Figure 13. Test hardware PCB stack depicting the (a) gate drive (GD) and (b) half-bridge with 30 µF bulk capacitance and 250 nF Cera-Link capacitor. Additional high and low-side transistor footprint slots are added for potential usage in parallel testing.

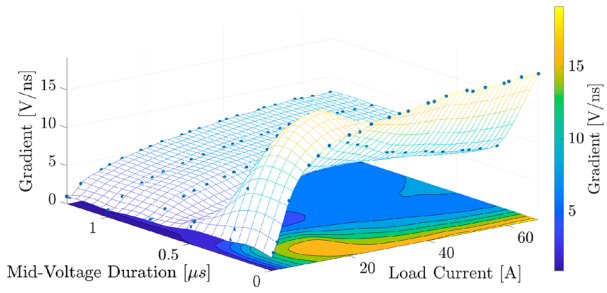

Figure 14. Scatter plot of measured points in an experimental verification of direct maps on a half-bridge setup for IMZ120R045M1. The DC-link voltage used is 550 V with gate resistance of AGD 22 Ω, and with U_{mid} of 5 V.

THDP0200 differential probes with short voltage clips to reduce couplings as is depicted in Figure 12.

The setup is automated and the pulse sequence is controlled through a microcontroller (MCU) stacked on top of the gate drive board which is depicted alongside the half-bridge test fixture in Figure 13. The MCU controls the duration of a single pulse, i.e. the PWM pin of the low-side SiC device, and reconfigures pulse duration (i.e. load current), mid-voltage duration t_{mid} and mid-voltage level U_{mid} with a 3-second pause in between. The oscilloscope is set to store every shot captured in normal mode. The current is controlled with pulse duration in 0 A to 65 A range, while t_{mid} is controlled in 0 ns to 1500 ns range and U_{mid} from 5 V to 12 V in 1 V steps. In total, 1056 shots for transistor current, drain-source voltage and gate-source voltage were captured, their value later extracted and fitted to a map depicted in Figure 14 for $U_{mid} = 5$ V.

Although the direct comparison of maps is not possible due to differences between setup and simulation, i.e. differences in gate resistance, the existence of parasitics in the commutation loop and production tolerances, maps can be qualitatively compared. The performance measurements show that du/dt during turn-off events can be controlled by applying different durations of mid-voltage levels similarly as was predicted by the simulations. Moreover, the measurements show that the shape of the map from Figure 8 qualitatively follows Figure 14, therefore justifying the usage of the proposed method.

Furthermore, by interpolating measured points to a finer grid, an inverted map with visible controllability area can be obtained as in Figure 15. An inverted map was obtained using the method described in the previous chapter. Having the current dependant inverted

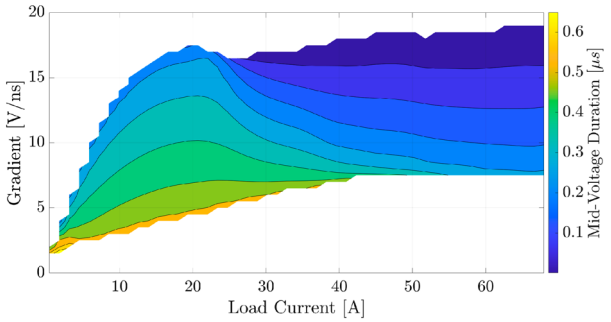

Figure 15. A contour plot of an experimental inverted map for 550 V DC-link voltage and $U_{mid} = 5$ V with $R_G = 22\,\Omega$. Areas of controllability have been following a similar domain shape as with inverted simulated maps.

map datasets pre-loaded in an MCU or FPGA enables a cycle-by-cycle du/dt control on an improved hardware setup that is currently under construction. Although the proposed method could be applied to many topologies which use a half-bridge as a building block, the automotive three-phase inverters are seen as the best candidate due to their beneficial influence on common mode and high demand in the future.

7. Simulated validation of optimized switching strategy

To compare the optimum switching strategy to the conventional gate drive, a simulated application of the three-phase inverter was employed. The three-phase inverter model consisted of six IMZ120R045M1 SiC MOSFETs. Six PWL files containing optimized injected gate voltages as well as load current signals were generated using MATLAB script. This way cycle-by-cycle du/dt control is employed and any operating point for the inverter could be tested.

In general, du/dt can be kept constant to limit the insulation strain and minimize peak EMI noise. For standard industrial drives, a typical limit of 5 V/ns to 10 V/ns is employed [34]. Mid-level time duration t_{mid} for input I_L and required du/dt is extracted from the inverted map and fitted to a polynomial. Moreover, for the uncontrollable parts of the switching cycle, i.e. when $I_L < 2.5$ A, duration $t_{mid} = 0$ ns is set.

Parasitics were omitted from the main simulation circuit to take the worst possible case of du/dt into the account, since additional parasitic slow down the switching further. To evaluate the active gate drive performance, the simulation uses worst-case modulation index for CM noise ($m_a = 0$ or $\tau_d f_s = 50\%$). This is because all of the three phases of the inverter then switch simultaneously and therefore generate a square wave-like CM voltage of triple the fundamental frequency instead of a stepped sine wave, like for high modulation indexes. The simulated time-domain common-mode signal was then fed to a virtual EMI receiver [35] for 9 kHz RBW, sweeping from 150 kHz

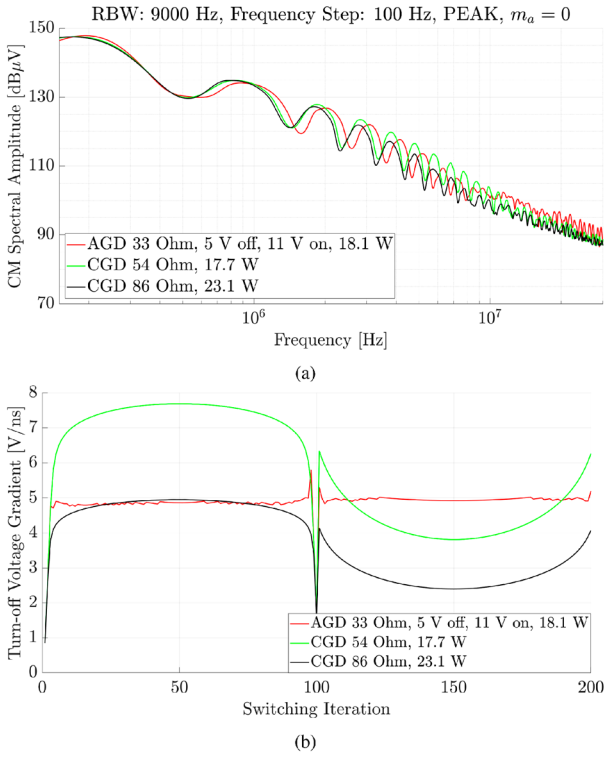

Figure 16. (a) Spectral response of peak CM noise of a three-phase inverter for 9 kHz RBW in 100 Hz steps and from 150 kHz to 30 MHz, and (b) du/dt in turn-off for every switching cycle for a sinusoidal current. Turn-on du/dt is symmetric along zero-crossing. Switching frequency used is 20 kHz with a fundamental output frequency of 100 Hz, while load current sine wave peak is 25 A. AGD exploits the unused area close to 5 V/ns as much as possible.

to 30 MHz. The resulting spectral response is depicted in Figure 16(a).

The comparison between the optimized AGD, equivalent losses CGD and equivalent maximum du/dt CGD has been shown in Table 3. While Peak CM emissions remain in the same range, Figure 16 shows that the time-dependent du/d$t(t)$ curve using AGD is fixed to 5 V/ns. CGD reaches set du/dt level in just one operating point, significantly increasing the losses.

For practical application, inverted maps can be pre-loaded into a DSP, so that close to optimal t_{mid} time can be found cycle-by-cycle. Small corrections to t_{mid} for temperature and DC-link voltage dependency with predictive methods could be employed to compensate for modelling inaccuracies.

8. Conclusion

SiC MOSFETs can now be used as easily as Si MOSFETs or IGBTs, with improved performance and potential for widespread use. The higher cost of SiC-based converters and potential EMI issues are the main obstacles to their adoption. Broader use is expected to bring costs down, while EMI issues could be reduced by passive filters or with appropriate conventional gate driving.

Table 3. Optimized AGD and CGD inverter parameters and comparison.

	Optimized AGD	Equation losses CGD	Equation du/dt CGD
Gate Resistance	Active 33 Ω	54 Ω	86 Ω
Total Losses	18.1 W	17.7 W	23.2 W
Max du/dt	5 V/ns	7.7 V/ns	5 V/ns
Peak noise @ 1 MHz	133 dBμV	133 dBμV	133 dBμV
Peak noise @ 6 MHz	109 dBμV	113 dBμV	109 dBμV
Peak noise @ 30 MHz	92 dBμV	89 dBμV	88 dBμV

In this paper, an overview of various active and advanced gate driving techniques were studied with several design practices for conventional SiC-based converters. Existing advanced solutions adjust the gate voltage or resistance to dynamically change the du/dt and/or di/dt. Typically, the advanced methods shorten the remaining transient phenomena after the transitions.

This paper gives the simplified switching model, which can be applied to both CGD and AGD. More importantly, an advanced and optimized active gate driving strategy with an explanation of underlying phenomena was introduced.

Within this, a strategy for cycle-by-cycle optimization of SiC MOSFETs switching is proposed to enable trade-off between switching losses and du/dt by keeping du/dt as close to constant as possible. The method yielded 28% lower total losses for the same maximum du/dt, with peak EMI within the same range. Employing the proposed method has shown that there is still room for improvement in active gate driving strategies.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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