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Journal for Control, Measurement, Electronics, Computing and Communications

ISSN: (Print) (Online) Journal homepage: www.tandfonline.com/journals/taut20

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**To cite this article:** Marek Pastor, Daniel Gordan, Tomáš Basarik & Chiemeka L. Maxwell (2024) Inverter optimization of soft-switching DC-DC converter*, Automatika, 65:4, 1391-1401, DOI: 10.1080/00051144.2024.2388442

**To link to this article:** https://doi.org/10.1080/00051144.2024.2388442



Published online: 07 Aug 2024.

AUTOMATIKA
2024, VOL. 65, NO. 4, 1391–1401
https://doi.org/10.1080/00051144.2024.2388442



# Inverter optimization of soft-switching DC-DC converter*

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**ABSTRACT**
The paper describes the influence of the magnetizing inductance of the transformer on zero-voltage switching of the primary transistors in a soft-switching full-bridge dc-dc converter with a controlled rectifier and turn-off snubber. The optimized version of the transformer allows for achieving a full zero-voltage and zero-current turn-on of the primary transistors in a full-bridge soft-switching DC-DC converter. The analysis is verified by measurements on a laboratory model of the converter. The influence of undischarged output capacitances on the efficiency is measured as well. Also, the impact of the GaN transistors on the zero-voltage switching is discussed.

**ARTICLE HISTORY**
Received 21 February 2024
Accepted 29 July 2024

**KEYWORDS**
DC-DC converter; transformer; zero-voltage switching

## 1. Introduction

The efficiency and power density of power converters are one of the most critical aspects in design for electric mobility [2] and renewable energy applications [3]. The preferred topology for medium and higher power levels is a full bridge converter with a high-frequency transformer [4]. Either unidirectional or bidirectional topology is selected based on the requirement for power flow. The typical topology for bidirectional power flow is a dual-active bridge (DAB) converter [5,6] which enables modern requirements such as vehicle-to-grid (V2G) interface [7]. On the other hand, the converter with a unidirectional power flow is a phase-shifted pulse-width modulated (PS-PWM) full-bridge converter. Both abovementioned topologies can incorporate soft-switching techniques to decrease the switching losses usually in the form of zero-voltage switching (ZVS) which enables to increase in the switching frequency [8–10].

The competitor for PSFB converter is a resonant converter, e.g. LCL, LLC or other types. In the real world, it's often a choice of trade-offs, the details of a given application. The disadvantage of the LLC converter is that it requires a more complex design, the frequency is variable from the load, causing a more complicated EMI filter design, and it requires approximately 7,5 times the output capacitor compared to the PSFB converter. The advantage is that it does not need an output choke. The disadvantage of the PSFB converter is that it is more difficult to achieve ZVS at low load [11], but this paper attempts to eliminate this problem.

The switching frequency is crucial for increasing the power density. Even though there are modern semiconductor devices based on silicon carbide (SiC) or gallium nitride (GaN) semiconductors which enable higher switching frequencies [12–14] for high-power converters, the soft-switching techniques still have their importance.

The range for ZVS in PS-PWM converter is influenced by the load current, especially for the lagging leg. The energy stored in the transformer's leakage inductance may not be sufficient for discharging the output capacitances in the lagging leg during the free-wheeling interval when the voltage on the primary side of the transformer is zero [15]. The switches in the leading leg are discharged by the energy stored in the output smoothing choke and it is usually high enough to ensure the ZVS even under light-load conditions. It would be useful to cancel the dependence of the lagging leg ZVS on the load current. This can be accomplished by incorporating the controlled rectifier which disconnects the secondary side of the converter during the free-wheeling interval [4,16,17]. If the primary side of the converter is designed in such a way that the magnetizing current of the transformer is sufficient for discharging the output capacitances, then the ZVS is independent on the load [17]. The scheme of such a converter is shown in Figure 1.

The zero-voltage zero-current switching (ZVZSC) DC-DC converter shown in Figure 1 was originally presented in [4]. The operating point of the primary transistor is shown in Figure 2. The operating point of the

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*This paper is an extended version of our paper [1] published in 2023 International Conference on Electrical Drives and Power Electronics (EDPE), The High Tatras, Slovakia, 25–27 September 2023, pp. 1–5. doi:10.1109/EDPE58625.2023.10274020.

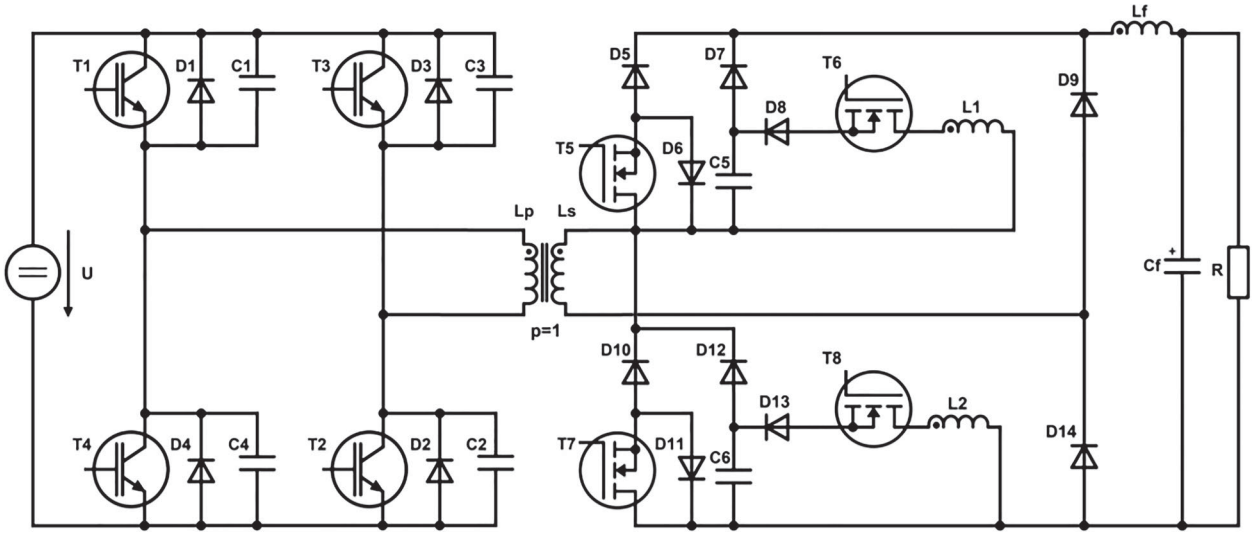



**Figure 1.** Converter of a ZVS full-bridge converter with controlled rectifier and energy recovery snubber.

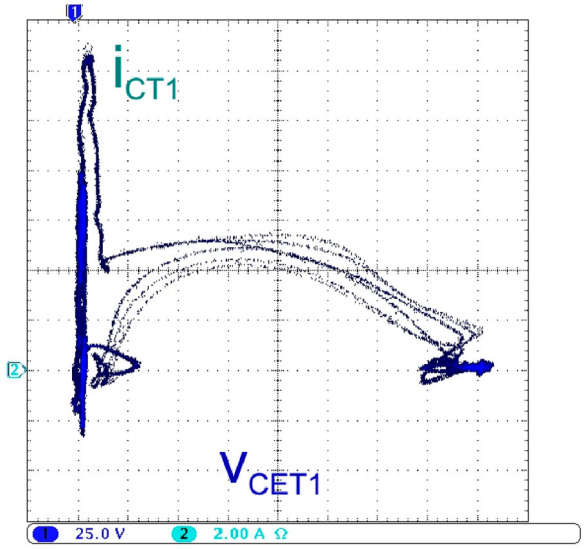



**Figure 2.** The operating point of the primary IGBT transistor for the original DC-DC converter [4].

transistor T1 stays in the area of high switching losses due to the poor design of the high-frequency transformer. The magnetizing current of the transformer is not sufficient for discharging the output capacitances of the IGBT transistors during dead-time intervals. The output capacitances are thus discharged during turn-on which causes higher turn-on losses.

This paper presents the optimization of transformer design and its impact on the ZVS of the primary transistors. The paper is organized as follows. Section 2 describes the topology and operational principle of the converter. Section 3 describes the design of the new transformer and its impact on the ZVS. Section 4 presents verification of the designed transformer operation by measurements on the soft-switching DC-DC converter. Section 5 concludes the paper.

## 2. ZVS converter topology and operational principle

### 2.1. Converter topology

The scheme of the described soft-switching DC-DC converter is shown in Figure 1. The converter consists of a primary side inverter with IGBTs $T_1$ – $T_4$ with antiparallel diodes $D_1$ – $D_4$. Output capacitances of transistors are illustrated by capacitors $C_1$ – $C_4$ to emphasize their importance for ZVS of primary transistors. The inverter is coupled with a controlled rectifier through the high-frequency transformer. The controlled rectifier consists of two MOSFET transistors $T_5$ and $T_7$ and rectifier diodes $D_5$, $D_{10}$, $D_9$ and $D_{14}$. The output voltage is filtered by inductor $L_f$ and capacitor $C_f$. A snubber network is designed to ensure zero-voltage turn-on of the rectifier transistors. The snubber for transistor $T_5$ consists of snubber transistor $C_5$, diode $D_7$, diode $D_8$, transistor $T_5$ and inductor $L_1$. The purpose of a snubber is to decrease the rate of change of voltage for the drain voltage during turn-off of the rectifier transistors, to absorb the energy of leakage inductance of the transformer and to return the absorbed energy to the load.

### 2.2. Operational principle

The operation of the converter can be divided into four time intervals within one half-period (Figure 4) based on the switching diagram of primary and secondary transistors shown in Figure 3. The resulting time series waveforms of the converter are shown in Figure 5. The primary transistors have modified switching when compared to classical PS-PWM switching. Primary transistor pairs switch with a fixed 50% duty cycle and fixed zero-degree phase shift. There is a short dead-time interval inserted between switching of the upper and the lower transistor within one leg. The

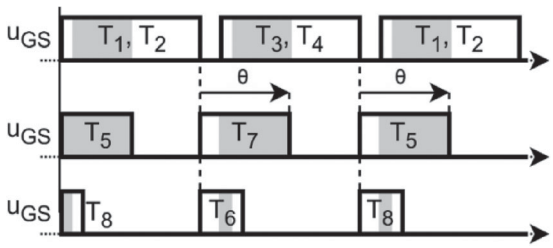



**Figure 3.** Switching diagram of transistors.

dead-time is used for safety reasons to prevent the short circuit within a leg and to ensure the discharge of output capacitances for the ZVS of primary transistors. The dead-time interval is thus usually longer than is required to prevent a short-circuit and the control circuit should have the possibility to set its duration. Also, there is no possibility for the control of the power flow at the primary side of the transformer. The power flow is controlled by the duty cycle of the secondary transistors $T_5$ and $T_7$ which are synchronized to the primary side. The snubber transistors $T_6$ and $T_8$ are turned on only for a fixed short time interval to discharge the snubber capacitors $C_5$ and $C_6$.

(a) Interval $t_0 - t_1$

Transistors $T_1$ and $T_2$ on the primary side are turned on together with the secondary transistor $T_5$ and the snubber transistor $T_8$. The snubber capacitor $C_6$ is discharged through the inductor $L_2$ and diode $D_{12}$. Part of the inductor current flows to the load. The primary current is decreased by the value of this discharging current. The rate of change of current for the primary current is limited by the leakage inductance of the transformer which ensures the zero-current turn-on of the transistors on the transformer primary side. Their output capacitances were discharged in the previous cycle which ensures their ZVS turn-on. At the end of this interval, the snubber capacitor $C_6$ is completely discharged and prepared for the next turn-off of the transistor $T_7$.

(b) Interval $t_1 - t_2$

After the snubber capacitor $C_6$ is discharged, the load current commutes to transistor $T_5$. The transformer primary and secondary currents are identical and differ only by the transformer ratio. This is the main power transfer interval and its duration controls the power flow to the load.

(c) Interval $t_2 - t_3$

The transistor $T_5$ is turned off at $t_2$. Its drain current commutes through the diode $D_7$ to the snubber capacitor $C_5$, which is discharged from the previous cycle. The capacitor $C_5$ limits the rate of change of voltage for the $T_5$ drain voltage which ensures its zero-voltage (ZV) turn-off. The primary current is decreasing to the value of the magnetizing current till the capacitor $C_5$ is completely charged.

(d) Interval $t_3 - t_4$

The primary transistors $T_1$ and $T_2$ are turned off at $t_3$. The load current flows through rectifier diodes $D_9$ and $D_{14}$ which now act as free-wheeling diodes. On the primary side, the transformer magnetizing current flows through output capacitances of IGBT transistors in a direction which charges capacitors $C_1$ and $C_2$ and discharges capacitors $C_3$ and $C_4$. The time variation in decreasing the collector voltage of primary transistors $T_3$ and $T_4$, $v_{T3}$ and $v_{T4}$ is described by:

$$v_{T3} = v_{T4} \approx \frac{1}{2}V\left(1+\cos\left(\sqrt{\frac{1}{C_{OES}+L_\sigma}}(t-t_3)\right)\right) - \frac{1}{2}I_\mu\sqrt{\frac{L_\sigma}{C_{OES}}}\sin\left(\sqrt{\frac{1}{C_{OES}L_\sigma}}(t-t_3)\right) \quad (1)$$

where: $L_\sigma$ – leakage inductance on the primary side, $C_{OES}$ – output capacitance of IGBT transistors, $I_\mu$ – magnetizing current, $V$ – converter supply voltage.

The minimum dead-time $t_d$ required for output capacitances to completely discharge is:

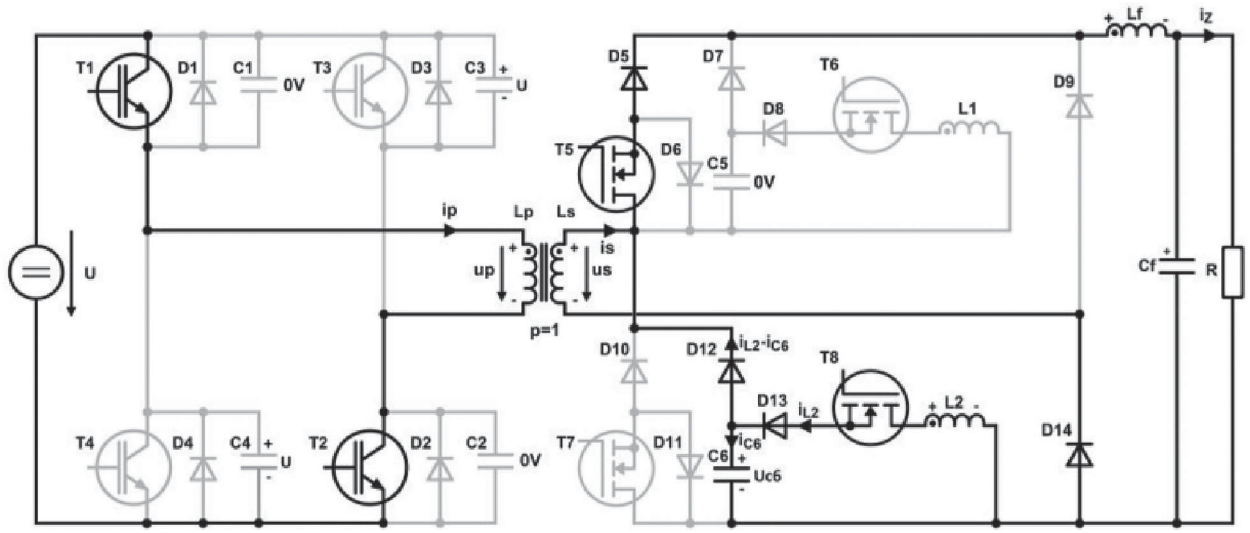
$$t_d \geq \frac{\pi + arctg\left(\frac{2I_\mu\sqrt{\frac{L_\sigma}{C_{OSS}}}VC_{OES}}{I_\mu^2L_\sigma - V^2C_{OES}}\right)}{\sqrt{\frac{1}{C_{OES}L_\sigma}}} \quad (2)$$

After the output capacitances are completely charged/discharged, the primary current starts to flow through the antiparallel diodes $D_1 - D_4$ and ZV turn-on of primary transistors is possible. Also, the snubber transistor $T_6$ is turned on which starts the resonance in $L_1$, $C_5$ circuit limited by diode $D_8$.

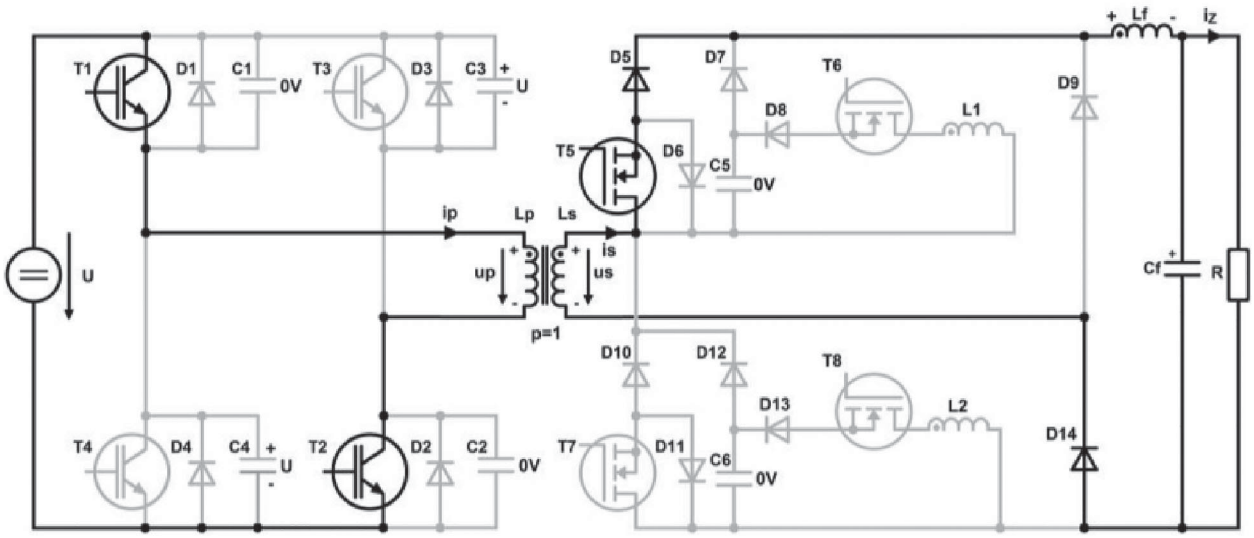
(e) Interval $t_4 - t_5$

This interval is similar to the interval $t_0$-$t_1$ except the polarity of the transformer voltages is reversed and the power is transferred through the other half of the converter. Due to the circuit symmetry, the description of these two intervals is similar. The rest of the operation of the converter in the next half-period is not shown as it can be easily derived from the presented operation in the first half-period.

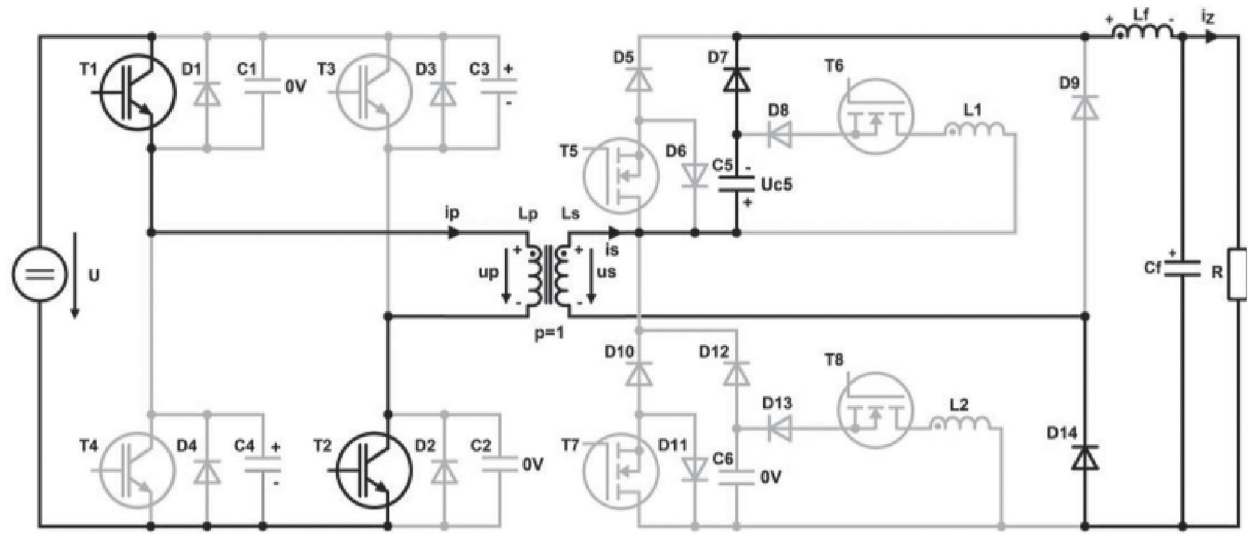
Based on (1) it is important to have a sufficient magnetizing current $I_\mu$ to discharge the output capacitances $C_{OES}$ within time interval $t_3 - t_4$ and to maintain the ZVS of the primary side IGBT transistors. Also, the dead-time period needs to be sufficiently long as defined by (2).




*a) interval $t_0$-$t_1$*

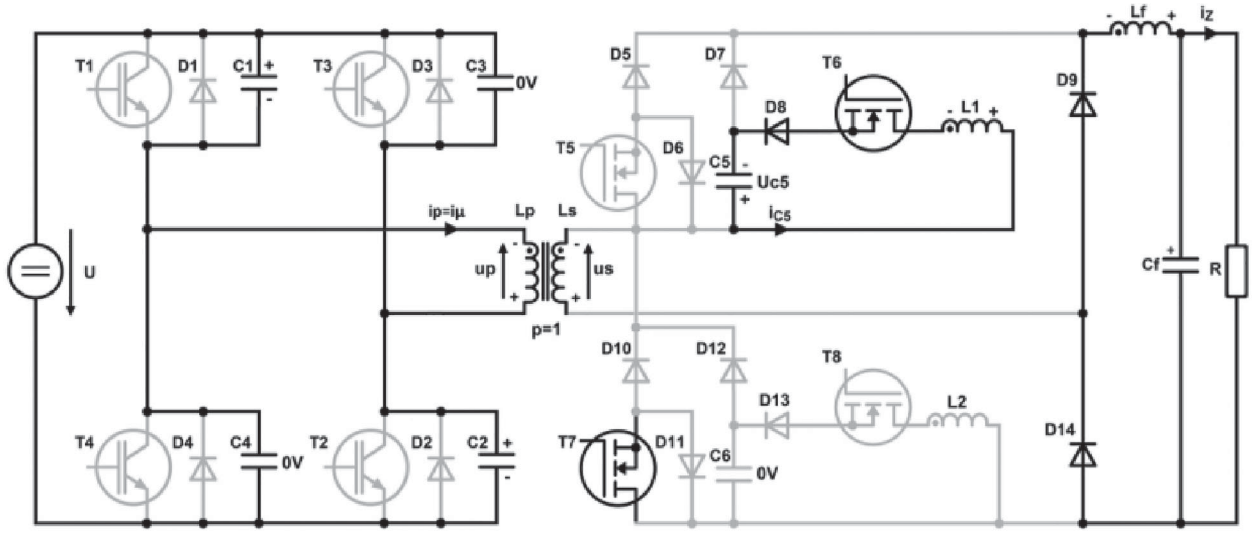



*b) interval $t_1$-$t_2$*

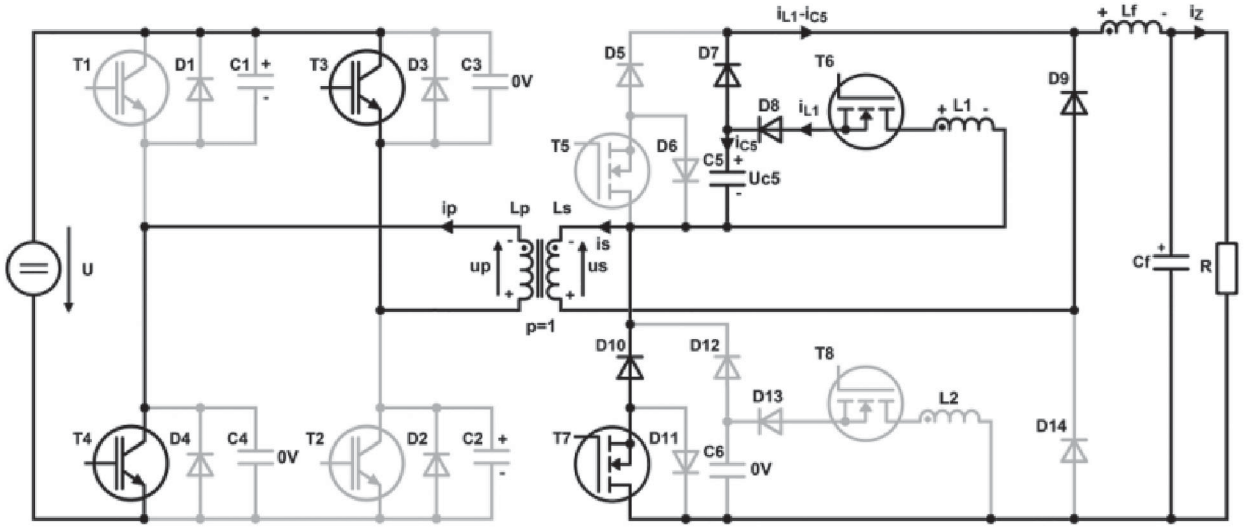



*c) interval $t_2$-$t_3$*

**Figure 4.** Operational principle of the DC-DC converter.




*d) interval $t_3$-$t_4$*




*e) interval $t_4$-$t_5$*

**Figure 4.** Continued.

## 3. Transformer optimization

The advantage of using the controlled rectifier is the independence of ZVS on the primary side from the load current. On the other hand, this approach increases the requirement for the design of the high-frequency transformer. The design of transformers is usually not based on the value of the magnetizing current and the manufacturer tries to keep this current low.

The leakage inductance $L_\sigma$ with the output capacitances $C_{OES}$ of IGBTs creates a resonant circuit. For the coarse value of required dead-time a formula based on the resonant frequency of an LC circuit can be used:

$$t_d \geq \sqrt{L_\sigma C_{OES}} \tag{3}$$

The magnetizing current will decrease the required minimum dead-time based on (2) for a given output capacitance of the IGBTs. The minimum required dead-time will be shortened with the help of the magnetizing current as is shown in Figure 6.

The parameter $L_\sigma$ in Figure 5 is the leakage inductance of the transformer. The leakage inductance usually causes problems in DC-DC converters. However, it has a positive influence on the proposed converter. The leakage inductance will slow down the commutation of the current from the secondary to the primary side of the converter after the primary transistors are turned on in interval $t_4 - t_5$. This will help to achieve zero-current (ZC) turn-on of the IGBT transistors. The energy of the leakage inductance is absorbed by the snubber capacitor in the interval $t_2 - t_3$ and returned to the load in the interval $t_4 - t_5$. The value of the leakage inductance is thus not crucial for the safe operation of the converter and its value influences minimum dead-time and

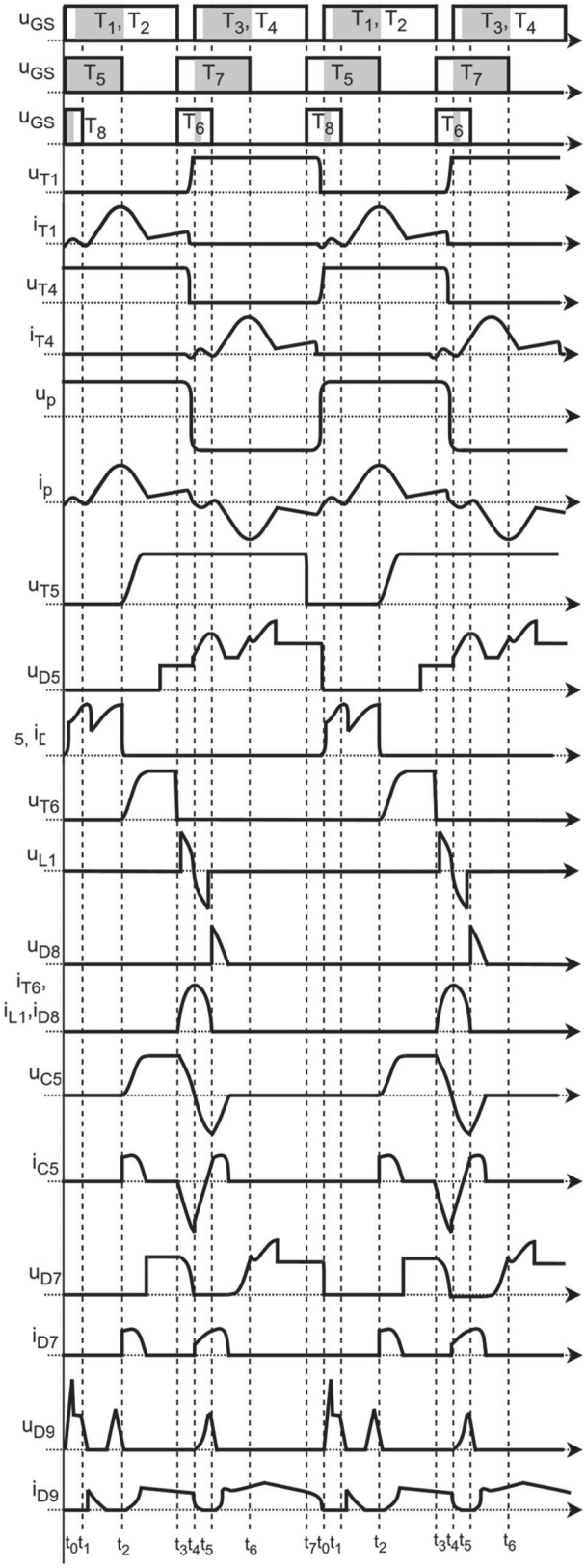



**Figure 5.** Time waveforms of the DC-DC converter.

the size of the snubber capacitor as it has to absorb its energy.

The main values of the original transformer are shown in Table 1. Its magnetizing inductance is 2.8 mH. The amplitude of the resulting magnetizing current can

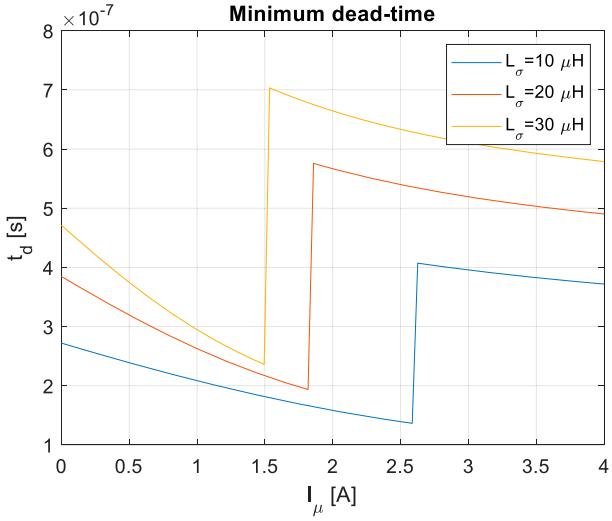



**Figure 6.** Minimum dead-time as a function of the magnetizing current for various transformer leakage inductances [1].

**Table 1.** Original transformer parameters.

| Parameter | Value |
|---|---|
| Power $P$ | 5 kVA |
| Magnetising inductance $L\mu$ | 2.8 mH |
| Leakage inductance $L\sigma$ | 2.5 μH |
| Operating frequency $f$ | 50 kHz |
| Transformer ratio $p$ | 1:1 |

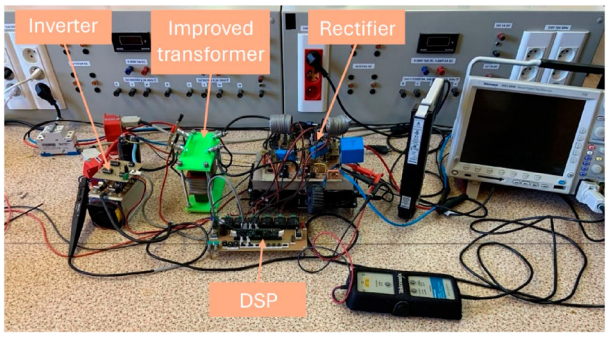



**Figure 7.** ZVZCS converter with newly designed high frequency transformer with increased magnetising current.

be calculated:

$$I_\mu = \frac{V}{4 f_S L_\mu} \tag{4}$$

For the supply voltage of $V = 400$ V, frequency of $f_S = 50$ kHz and magnetizing inductance of $L_\mu = 2.8$ mH, the resulting amplitude of the magnetizing current is $I_\mu = 0.71$ A.

The parameters of the newly designed transformer (Figure 7) are shown in Table 2. Its magnetizing inductance is reduced to 1.17 mH, which results in the amplitude of the magnetizing current being 1.71 A. Also, its leakage inductance was increased to 20.2 μH.

## 4. Converter measurements

The nominal parameters of the DC-DC converter are shown in Table 3 and its main components are shown

**Table 2.** Optimized transformer parameters.

| Parameter | Value |
|---|---|
| Power $P$ | 5 kVA |
| Magnetising inductance $L\mu$ | 1.17 mH |
| Leakage inductance $L\sigma$ | 20.2 µH |
| Operating frequency $f$ | 50 kHz |
| Transformer ratio $p$ | 1:1 |

**Table 3.** DC-DC converter parameters.

| Parameter | Value | Unit |
|---|---|---|
| Nominal power $P_N$ | 4 | kW |
| Nominal input voltage $V_I$ | 400 | V |
| Nominal output voltage $V_O$ | 300 | V |
| Switching frequency $f_{SW}$ | 50 | kHz |

**Table 4.** DC-DC converter components.

| Component | Value |
|---|---|
| T1, T2, T3, T4 | IRG4PSC71UD |
| T5, T6, T7, T8 | C2M0025120D |
| D8, D9, D13, D14 | HFA30PB120 |
| D5, D7, D10, D12 | C2D20120 |
| L1, L2 | 8.6 µH |
| C5, C6 | 27 nF |
| $L_O$ | 130 µH |
| $C_O$ | 1 µF |

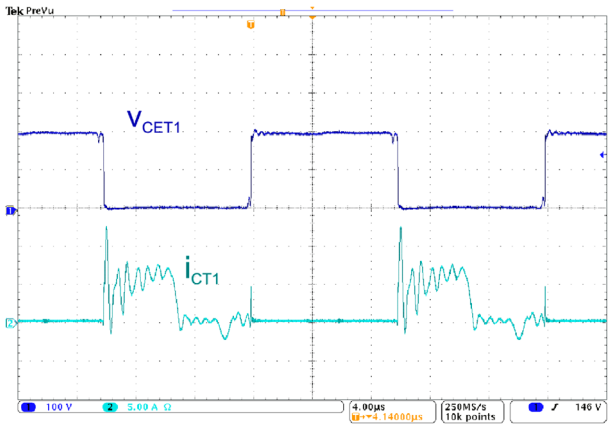



**Figure 8.** The switching of the primary transistor with the original transformer [1].

in Table 4. The converter was measured with the supply voltage $V_I = 200$ V and the output current $I_o = 5$ A. The switching frequency $f_S$ on the primary and secondary side was 50 kHz.

The previous version of the ZVZCS DC-DC converter [2] had poor ZVS performance on the primary side. Figure 8 shows the collector voltage $v_{CE}$ and collector current $i_C$ of transistor $T_1$. Its operating point is shown in Figure 1. The magnetizing current was insufficient to completely discharge the transistor output capacitance.

The control algorithm of the converter is shown in Figure 9. The theoretical minimum required deadtime interval for IGBT transistors IRG4PSC71UD with $C_{OES} = 720$ pF is $t_d = 0.38$ µs. The converter operated with a $t_d = 1$ µs.

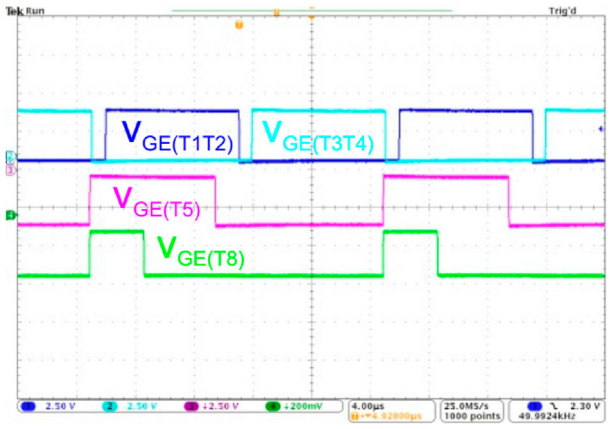



**Figure 9.** The generated control voltages for primary transistors and cooperating secondary transistors.

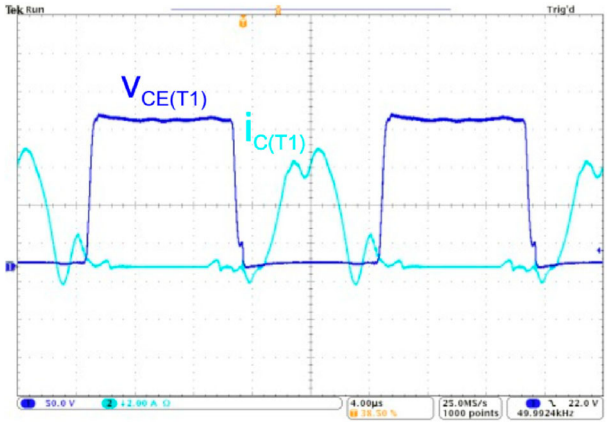



**Figure 10.** The switching of the primary transistor $T_1$ with the optimized transformer.

The waveforms of the collector voltage and collector current of transistor $T_1$ are shown in Figure 9. The output capacitance of the transistor is discharged ensuring ZV turn-on. Also, the increased leakage inductance of the transfer limits the rate of rise of collector current. The reason why the waveforms are shown only for transistor T1 is the location of the current probe, adding additional measurement points adds parasitic elements to the inverter circuit.

Moreover, the antiparallel diode conducts prior to transistor turn-on ensuring ZV and ZC turn-on process. The switching of the primary transistor T1 is shown in Figure 10 and its operating point of the transistor is shown in Figure 11, which also illustrates the improvement of the switching trajectory when compared to the one shown in Figure 1. The primary transistor has ideal ZV and ZC switching conditions.

The ideal switching trajectory reflects ZV and ZC switching, which results in lower inverter switching losses.

The discharge of the output capacitance of the primary IGBT transistor for a supply voltage $V_I = 200$ V is illustrated in Figure 12. The magnetizing current of the original transformer was not able to completely

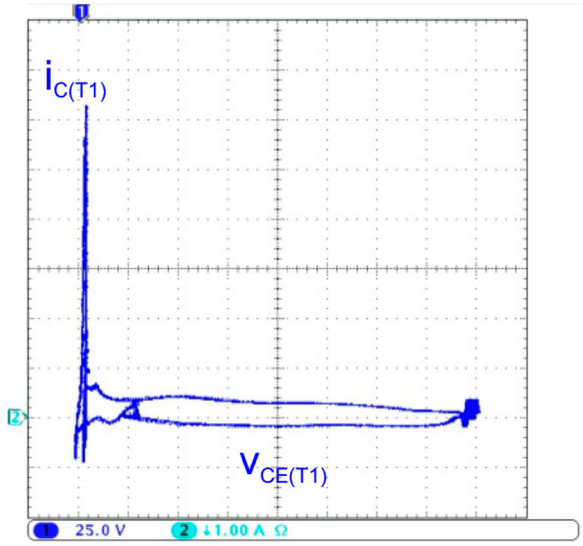



**Figure 11.** The switching trajectory of the primary transistor $T_1$ with the optimized transformer.

**Table 5.** Inverter efficiency at $V_I = 100$ V.

| $I_Z$ (A) | Eff. with original transformer (%) | Eff. with improved transformer (%) |
|---|---|---|
| 1 | 94,97 | 95,19 |
| 1,5 | 93,36 | 94,83 |
| 2 | 93,74 | 94,56 |
| 2,5 | 94,17 | 95,38 |
| 3 | 94,59 | 96,11 |
| 3,5 | 95,08 | 96,71 |
| 4 | 95,36 | 97,14 |
| 4,5 | 95,58 | 97,57 |
| 5 | 95,79 | 97,82 |

discharge the output capacitance of the IGBT transistor due to the low magnetizing current with the amplitude of 250 mA. The partially charged output capacitance was abruptly discharged after the gate voltage was applied which resulted in current oscillation (Figure 12(a)). On the other hand, the improved transformer had an amplitude of the magnetizing current 580 mA which was sufficient for output capacitance discharge and there was no current oscillation after the turn-on as can be seen in Figure 12(b). The converter was not loaded and the only load for the inverter was the transformer.

The inverter efficiency was measured at reduced voltages of $V_I = 100$ V, Table 5 and 200 V, shown in Table 6, with a converter load current in the range of 1 A to 5 A. The lower input voltage was not able to create a sufficient magnitude of the magnetizing current to discharge the output capacitances.

Based on the data in Tables 5 and 6, the diagrams shown in Figures 13 and 14 depict the influence of the load current on the efficiency of the inverter for both transformers.

The efficiency was measured by a power analyser ZES ZIMMER LMG500. The efficiency of the inverter should be inversely proportional to the load current due to the conduction losses. However, the efficiency

**Table 6.** Inverter efficiency at $V_I = 200$ V.

| $I_Z$ (A) | Eff. with original transformer (%) | Eff. with improved transformer (%) |
|---|---|---|
| 1 | 95,10 | 95,16 |
| 1,5 | 96,76 | 96,38 |
| 2 | 96,90 | 97,82 |
| 2,5 | 94,48 | 97,73 |
| 3 | 94,16 | 97,26 |
| 3,5 | 94,24 | 96,96 |
| 4 | 94,42 | 96,90 |
| 4,5 | 94,73 | 96,90 |
| 5 | 95,09 | 96,97 |

**Table 7.** Comparison of converters.

| | ZVZCS – original transformer | ZVZCS – improved transformer | PSFB converter |
|---|---|---|---|
| ZVS | Only partially, low magnetizing current, Figure 7 | Yes, independent of the load, Figure 9 | Yes, typically starting from 50%[a] of the load No[b] |
| ZCS | Only partially, fast current rise, Figure 7 | Yes, leakage inductance decreased the current rise, Figure 9 | |
| Efficiency | Limited by inverter partial hard switching losses and by losses in the secondary snubber and controlled rectifier | Limited by losses in the secondary snubber and controlled rectifier | Limited by circulating current[b] |
| Complexity | Necessary additional circuits on the secondary side | Necessary additional circuits on the secondary side | Relatively few components |

[a]Typical value in PSFB converter design, depends on the additional inductance and output capacitance of transistors.
[b]Typical PSFB converter is not able to turn off the circulating current from the output filtering inductance.

also depends on the quality of the turn-on and turn-off process which is influenced by parasitic inductances mainly in the secondary side of the dc/dc converter. Even though the magnetizing current of the transformer is not influenced by the load current, the load current influences the transients which has a positive impact on the quality of the turn-on process.

A clear comparison of the converter with the improved transformer, with the original transformer and the classic PSFB converter is shown in Table 7.

## 5. Discussion

The paper demonstrates the improvement of transistor switching in an inverter by increasing the magnetizing current. A higher magnetizing current will cause a faster voltage drop across the output capacitance Coss. In equation (2), there was a change in the magnetizing inductance, a smaller value resulting in a larger magnetizing current.

Inspecting equation (2), it is evident that the required output capacity Coss is a function of the minimum dead time. By using transistors with smaller

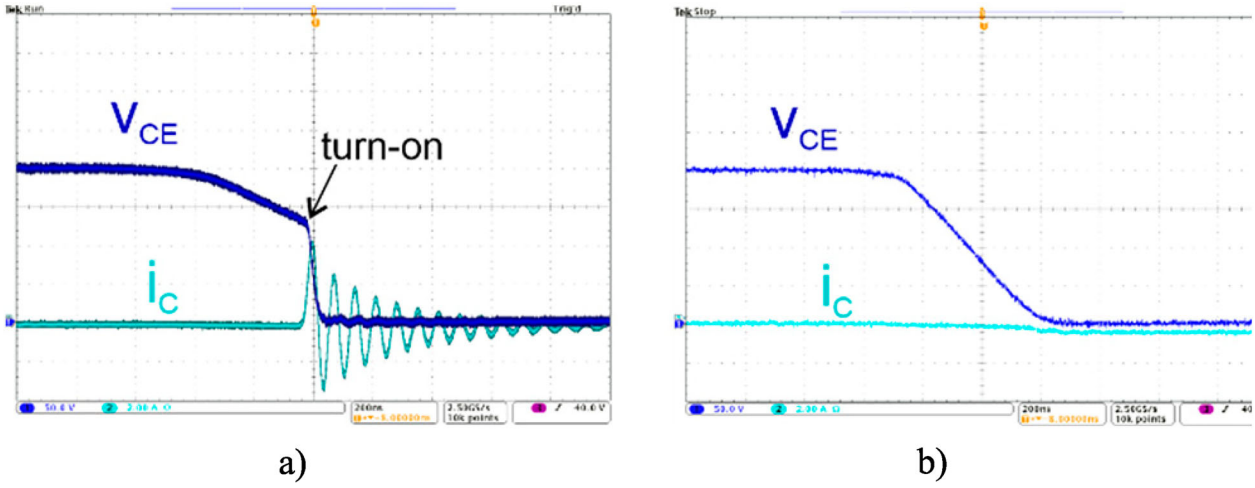



**Figure 12.** Output capacitance discharge of transistor T1 prior to its turn-on for $V_I = 200$ V. (a) original transformer ($I\mu = 250$ mA), (b) improved transformer ($I\mu = 580$ mA).

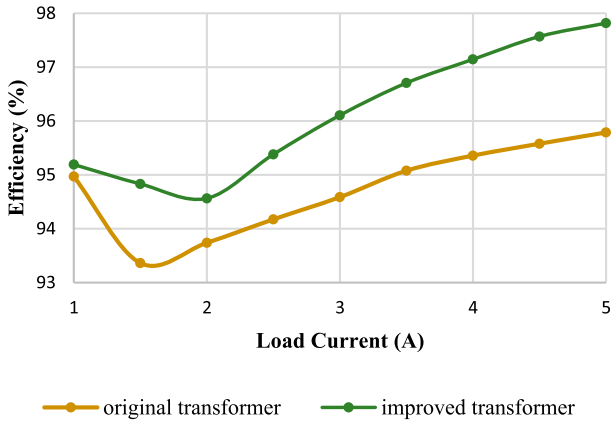



**Figure 13.** Comparison of inverter efficiency at $V_I = 100$ V.

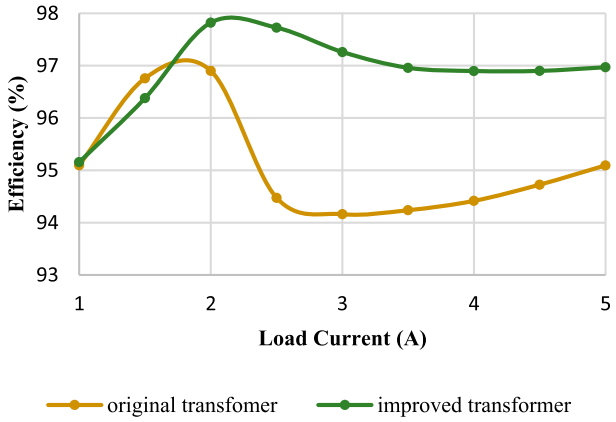



**Figure 14.** Comparison of inverter efficiency at $V_I = 200$ V.

output capacitance, the same effect could be achieved with the original transformer. The advantages of GaN transistors on dead time for a similar converter with PS control are given in [18] and [19] and for PFC converter in [20]. In addition to the change in dead time, different semiconductor technology also has an impact on switching losses, which is described in [21]. The Table 8 shows the minimum dead time for IGBT with improved transformer and GaN with original transformer.

**Table 8.** Comparison of IGBT with improved transformer and Gan with original transformer.

| | GaN GS0650302L | IGBT IRG4PSC71UD |
|---|---|---|
| $C_{oss}$ | 60 pF | 720 pF |
| $I_\mu$ | 1.71 A | 0.71 A |
| $t_{d\,(min)}$ | 0.163 us | 0.229 us |

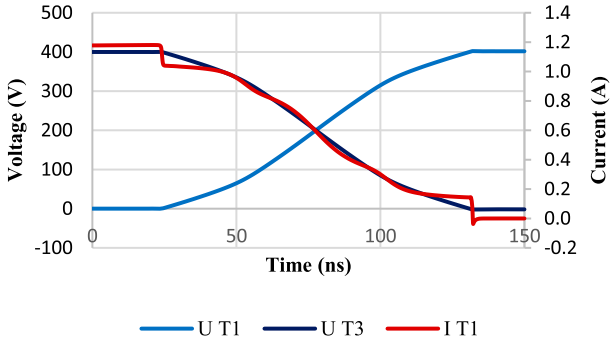



**Figure 15.** Voltage drop at GaN transistor with original transformer.

By changing the transistor type to a one with smaller output capacitance $C_{OSS}$ we can achieve similar results as by changing the transformer. Keeping the amplitude of the magnetization current lower, will result in lower losses in the transformer, which has a positive effect on the overall converter losses.

The calculation was validated by a simulation for three conditions. For IGBT with the original transformer, with an improved transformer and for GaN with the original transformer. The voltage drop time of $U_{T1}$ from 400 V to 0 V was measured. An example waveform for GaN with the original transformer is shown in Figure 15. The complete results of the simulation measurement are shown in Table 9.

Simulation results show that we can achieve a smaller minimum required dead time with the GaN transistors and the original transformer than with the IGBT transistors and the improved transformer.

**Table 9.** Voltage drop time for different conditions.

| | Time (ns) |
|---|---|
| IGBT original transformer | 696 |
| IGBT improved transformer | 384 |
| Gan original transformer | 108 |

## 6. Conclusion

The paper presents optimization of the switching trajectory of primary transistors in the soft-switching full-bridge DC-DC converter with a controlled rectifier. The controlled rectifier enables decoupling of the load current from influencing the ZVS of the primary transistors. The soft switching on the primary side depends on the parameters of the high-frequency transformer, mainly its magnetizing current. The proper design of the transformer can ensure the ZV turn-on of the primary transistors by discharging their output capacitances within the dead-time period. Its influence on ZV turn-on needs to be considered as well. Measurements on the laboratory model of the converter show significant improvement on the primary side switching after high-frequency transformer optimization. This improvement enables to increase the efficiency of the inverter. Further research will be conducted on the implementation of GaN transistors on the primary side of the dc/dc converter. This approach promises a further increase of the converter efficiency by decreasing not only the losses in the inverter but also in the high-frequency transformer.

## Disclosure statement

No potential conflict of interest was reported by the author(s).

## Funding

This work was supported by the Scientific Grant Agency of the Ministry of Education of the Slovak Republic under the project VEGA 1/0584/24.

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