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Enhanced Low Power FinFET-Based Flash ADC Design for High-Speed Electronics Applications

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Abstract: In electronics applications, signals are often of very low amplitude and frequency, making them susceptible to distortion and noise, which are unavoidable issues. Over the last few decades, Complementary Metal Oxide Semiconductor (CMOS) technology has been the most widely used process technology for mobile communication devices, biomedical systems, and image processing. However, conventional CMOS comparators suffer from stacking and driving current limitations, and face significant second-order effects below the 45 nm process node. In this paper, we present the circuits of Flash analog-to-digital converters (ADCs) specifically designed for mobile and biomedical applications. Flash ADCs are ideal for high-speed and wide-bandwidth applications, where comparators and encoders are crucial components of the ADC architecture. The main objective of this work is to design low-power, enhanced current-driving circuits for Flash ADCs. This is achieved by designing a FinFET-based comparator, encoder, and supporting circuits for ADCs in a 32 nm process. Our investigation shows that performance degrades at higher speeds below 32 nm, but our modified double-tail comparator and encoder unit effectively reduce power consumption while improving current-driving capabilities. This work builds upon previous research conducted at the 180 nm CMOS process level. For implementation, we investigated Taiwan Semiconductor models for CMOS and FinFET at 45 nm, 32 nm, and 14 nm using Synopsys HSPICE.

Keywords: comparator design; flash ADC; FinFET technology; high-speed circuits; low power design

1 INTRODUCTION

In Very Large-Scale Integrated circuits (VLSI), the device density is improving day by day through new technology but the power problem is one of the most serious limitations in high performance applications. In biomedical applications, the signals used are of very low amplitude and frequency. A small distortion or noise problem is unavoidable. In last decades, Complementary Metal Oxide Semiconductor (CMOS) is the most utilized process technology for mobile communication devices, biomedical system and image processing. Due to the rapid advancement in fabrication high density chips were manufactured for various applications using the digital circuit technologies. Especially in mobile communication, there were high data rate and speed. On the other hand, for image processing and signal processing the amount of data used were high. The system needs a very high processing speed and data handling capability. The memory requirements were also increased. So to process these information digital systems with analog acquisition circuits with higher operating speed is needed. Several Analog to digital converters (ADC) were used in literature which is effective [1]. There are still challenges with CMOS circuits when the size of the transistor is reduced. Over the years, circuits have evolved to analyze signals in the continuous time domain and convert them to the digital domain. Comparators based on voltage levels are key components of these systems. The design should sense the signal below 1mV, due to the voltage range in the medical system [2]. In addition to that, the operational amplifier used in the analog acquisition unit should have better offset cancellation [3], operating speed and high common mode rejection ratio (CMRR). In conventional circuit the compensation methods for charge pumping are required for the large voltage swing [4]. But in low power application the driving current should be sufficient enough to stabilize the logic levels of the subsequent stages of the circuit [5]. The other problems are the device stacking in the comparator. The input range of low power applications is in milli volts which is amplified using the voltage gain circuit. Offset is another issue due to device mismatch and the load capacitor [6].

In literature, ADCs used both lower and higher sampling rate based on the application. The parallel architecture of flash ADC makes it a faster circuit and simple to implement. These can become part of processor core input port which acquires the analog input [7]. Vedic architectures were used in processing of information in several works. But the power consumption of high-speed devices increases if the input and sampling frequency is higher. The flash ADC resolution is increased to a limited level only due to the components count [8]. Several ADCs were designed for successive approximation method which uses delay shift technique and loop unrolling [9, 10]. In flash ADC to enhance the buffering, latching interpolated architecture was designed in 65 nm CMOS technology [11]. A similar type of interpolation was performed with offset calibration [12]. Other designs followed the linearity, asynchronous and residual transfer in ADC [13-15]. The other challenges are on the clock distribution for the ADC circuits especially for microprocessor board [16]. Time based ADC with non-interleaved architecture is presented in literature which was implemented in 65nm CMOS. The performance for various frequencies is presented [17]. Delta sigma design is preferred for application which needs moderate bandwidth and power requirements [18]. CMOS based delta sigma ADC design is performed in 65 nm technology [19]. The analysis of various ADC and digital to analog converters was reviewed by Smith et al [20]. The frequency response was investigated. The comparators and processing elements like multipliers were used in several applications [21-24]. The FinFET based design provides low power and minimum area when designed for ADC [25, 26]. Boot strapping was included in certain design for the performance improvement in high speed device[27]. In this paper the design of various ADC circuits was presented. The problems of CMOS based Flash ADCs were high power dissipation because of the large number of high-speed comparators and leakage current.

The power optimization has been achieved, and the current driving capability of the designed circuits increases due to the elimination of leakage current during static

operation. The speed is also improved, reaching ranges of several hundred MHz. In ASICs, new devices can be fabricated for implementation. Various technologies, such as 65 nm, 45 nm, 32 nm, and 14 nm, can be utilized for fabrication. ASICs allow for mixed-device fabrication, enabling the integration of CMOS and FinFET technologies within the same device. In FPGA, the device is fixed while the programming can be used for changing the application. The reconfigurable nature allows modifying the internal elements of the system whenever required.

Research Gap: Power optimization has been addressed as an important aspect of VLSI technology. In current CMOS technology, power and current management are critical issues. Since CMOS circuits face limitations in these areas, improvements in driving current and power reduction have been achieved by using multigate devices. The challenges in CMOS circuits are addressed by employing dual-gate MOS devices. Below the 32 nm node, conventional systems exhibit poor performance at higher speeds.

2 LITERATURE REVIEW

Various components of ADC are to be designed to match the compatibility between the blocks and its performance. The various components of ADC are shown in Fig. 1. The number of channels is 8. In biomedical and wireless network the number of channels varies. The analog multiplexer (MUX) selects the sensor input. The main unit of the ADC is the encoder and the comparator. The resolution of the ADC is maintained by the comparator. The step size is the important factor considered for the ADC designed. The selected input is compared with the reference signal. Based on the feedback of the comparison, the encoder generates the digital value. In the 8bit ADC, Q [7] the MSB is encoded once the analog input A_IN is analyzed in the comparator. Thermometer code T [127:1] is used for the generation of the other bits. The Comparator block output is processed in the Thermo-to-Gray-to-Binary Encoder.

The schematic diagram for the analog multiplexer used in the ADC is shown in Fig. 2, with its corresponding truth table provided in Tab. 1. The selection lines are indicated, and based on the selection, the sensor input is chosen. The schematic is connected to various channels or sensor units. Typically, the ADC is connected to a DSP or microprocessor unit. The three selection lines are connected to the ports of the microcontroller, which selects the channel or analog input for conversion to digital form.

In recent decades, microcontrollers have integrated internal ADCs. In this work, the designed ADC components are suitable for on-chip design, as the implementation follows the Application Specific Integrated Circuit (ASIC) system. The sampling frequency can be controlled programmatically. The CMOS-based comparator, operating with a 1 V Vdd, converts the input to a logic level, which is then converted to binary in the encoder block.. The truth table of the MUX is shown in Tab. 1. Based on the select lines S2, S1 and S0 the inputs are selected. The select lines logic 1 correspond to 1 V and logic 0 to 0 V.

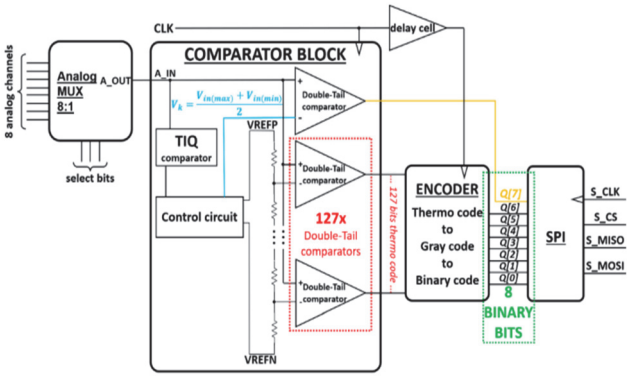

Figure 1 Block diagram of flash ADC with thermos code to gray code to binary code

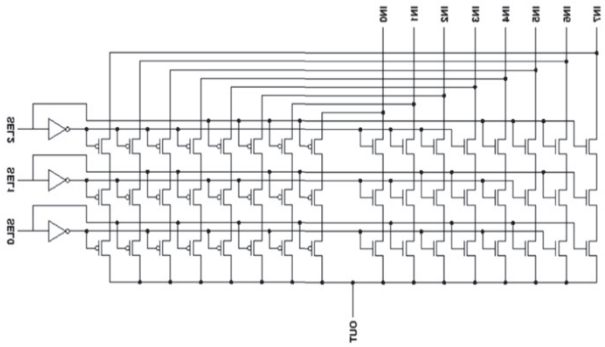

Figure 2 Schematic diagram for analog MUX used in ADC

Table 1 The truth table of eight by one MUX

S2	S1	S0	OUT
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	0	0	IN4
1	0	1	IN5
1	1	0	IN6
1	1	1	IN7

2.1 Comparator Block

The dynamic latch comparator circuit, in certain applications, functions as a sense amplifier using CMOS devices. These circuits enhance driving current and minimize offset variations, which can be effectively eliminated. Mismatches in transistors are common in VLSI fabrication; however, due to their minimal magnitude, these offsets can be corrected. Linear amplifiers can mitigate offsets, thereby avoiding resolution issues. Offset noise adversely affects the system, and if unnoticed or unresolved, it impacts subsequent stages. Amplified noise can distort the information present in the input signal. To address this, the acquisition unit is designed with filters that remove noise at the input stage, ensuring the signal fed to the ADC is free from mismatch and offset noise. Additionally, a differential input stage can further eliminate offset noise issues. In flash ADCs, power consumption is higher in clocked regenerative comparators. Static power consumption can be eliminated, and parasitic capacitance can be reduced by using larger transistors. Dynamic comparators were designed to nullify the static power consumption. This also avoids the stacked transistors and need for high supply voltage.

2.2 Encoder Block

In the proposed ADC, the encoder circuit converts a thermometer code into binary code, with a gray code as an intermediate step. The grouped encoder unit ensures the conversion of invalid logic into valid logic without errors, achieved through signal latching. In biomedical systems, the sensor output may sometimes be low, below a single step size, which can lead to logic instability. The design addresses this by allowing a one-bit increase or decrease to stabilize the logic.

The schematic diagram of the encoder block is shown in Fig. 3. This parallel architecture converts thermometer code to binary using a combination of NOT, AND, OR, and XOR gates. The comparator generates the thermometer code, and the final output is the binary code. The digital accuracy is high, as each thermometer bit impacts only one gray code bit, ensuring reliable conversion.

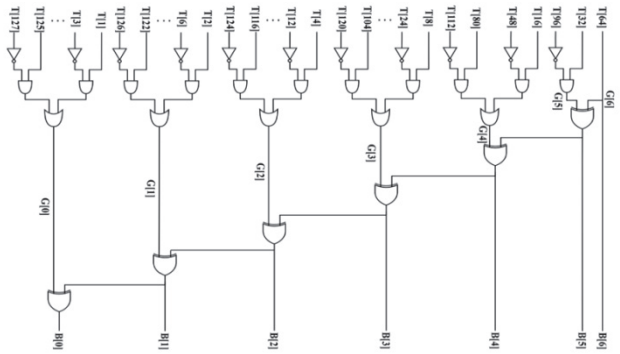

Figure 3 Schematic diagram of the encoder block

2.3 Control Circuit

The purpose of the Control circuit is to generate the reference voltage to the resistor network or ladder. Since the ladder network has increasing voltage levels, the levels are designed by the control circuit as per the comparator controlling input signal-VCTRL. The input levels are VDD and GND while VK is the mid voltage level.

If comparator output > VK, PMOS is ON, VREF = 1 V

If comparator output < VK, NMOS is ON, VREF = 0.5 V

The transistors M11 and M12 enhance the signal improvement since the resistor network loads the outputs and the expected output is not attained. There is variation in the output voltage against the expected value.

2.4 Limitations of the Existing Architectures

Today, as artificial intelligence plays a significant role in biomedical signal and image processing, efficient processing elements and circuits are essential for data acquisition, processing, and decision-making. Although general-purpose computers have been used for these applications, application-specific integrated circuits (ASICs) are increasingly employed. ASICs require Very Large-Scale Integration (VLSI) technology for their implementation, enabling low-power and high-density circuit designs. However, existing technologies often fail to meet the requirements for low-power design.

For example, the comparators designed use dynamic structures which face the mismatch in transistors. This led to offset and amplification of it in further stages. Differential Stages or Linear amplifier may be used with the comparators to avoid the offset due to device mismatches. The stacking reduces the driving current at the output stage. The voltage should be high enough to provide the bias voltage. The input range of low power applications was in milli volts which should be amplified using the voltage gain circuit. Stacking affects this process.The regeneration in clock can increase the impedence at the input and rail-to-rail voltage; the comparator can be designed with clocked regeneration. The other requirements are strong positive feedback and reduced input-referred offset. ADCs are faster so comparator and other circuit speed should be higher, which is lagging in the existing methods.

3 PROPOSED DESIGN

The proposed flash ADC architecture is shown in Fig. 4. The design uses two comparators, the threshold interleaved comparator and a proposed double tail comparator. The control circuit is used for the reference voltage generation.The circuit for ADC can be used in other applications like audio applications and sensor technology. The sensor technology with IoT is used in agriculture and wireless sensor networks for traffic management.

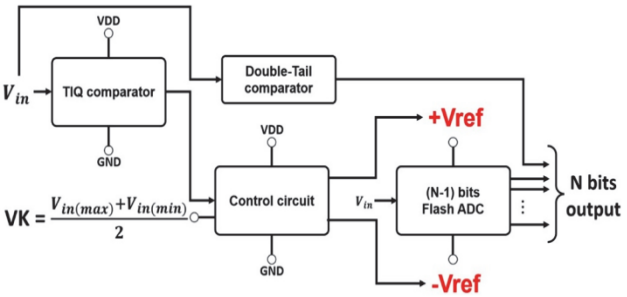

Figure 4 The proposed architecture of N-bit flash ADC

The FinFET based proposed design for comparator is shown in Fig. 5. The signal from the electrode or sensor is compared and if the voltage is below or above the comparator threshold voltage the output will be between the VDD and GND. The comparator operation is guided by the two clock signals. The speed of operation is decided by the comparator clock circuit. The speed is very high due to the clock frequency between 800 MHz to 1.5 GHz. Digital stream input of frequency 1 KHz was used.After 1.5 GHz the finfet performance on speed is low. But it reduces the leakage current in a better way. The supply voltage is also low due to power consumption reduction. The offset is also minimum. The offset is improved through subsequent amplifier circuit. To adjust the time sequence, clocks of different frequency can be used. Fig. 6 shows the CMOS and FinFET design of the double tail comparator.The design is based on real-time application inputs and can handle any sampling frequency. It adheres to fabrication standards. To validate the design, Taiwan Semiconductor MC and Stanford model files were used for implementing FinFETs and other devices. The 32 nm DGNMOS and

DGPMOS model files, commonly used in the real-time fabrication of integrated circuits, were utilized in this work.

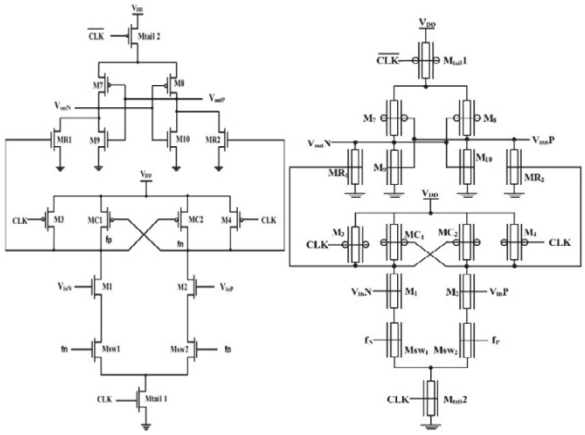

Figure 5 Modified double tail comparator using (a) CMOS (b) FinFET technology

In comparator circuit, the kick back noise is reduced using large transistor sizes. But it adds large parasitic capacitances. In the proposed circuit, the stage 1 uses buffering and bias current control. The double tail structure eliminates the stacking problem. A built-in threshold is included in stage 2 to reduce the power consumption. This reduces the addition power requirement for threshold generation. Capacitive loads increase the robustness of the circuit. The drains of the input transistors have capacitive loads. These capacitances of transistors provide overlap capacitance values on their drain nodes. So, the capacitive load improves the robustness with capacitance values in femto farad.

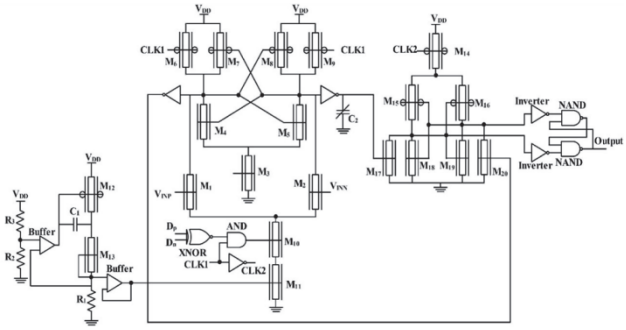

Figure 6 Proposed high speed low power comparator using FinFET technology

The kick back noise is reduced through the large area transistors which can be avoided by the multigate devices. The main problems in this design is the area and the large power requirements. The capacitance also increases as the area increases. The calibration is the challenging task and the reduction may not avoid the leakage current or fast switching current happening in the CMOS circuits. In double tail comparator, the current is well controlled. The temperature and process spread affects the current. The stability and reduction in skew are important features in the ADC design which is guaranteed using the multigate devices. The time factor is reduced. The increase in area may create additional delay which is avoided in this design. The frequency response is wide so suitable for biomedical and communication systems. Fig. 6 is the FinFET based design.

4 PROPOSED DESIGN USING FINFET

The FinFET based proposed design is in the shorted gate configuration. In the independent Gate method, the different gate is given unique voltage levels which are kept for future work and out of scope of this work.

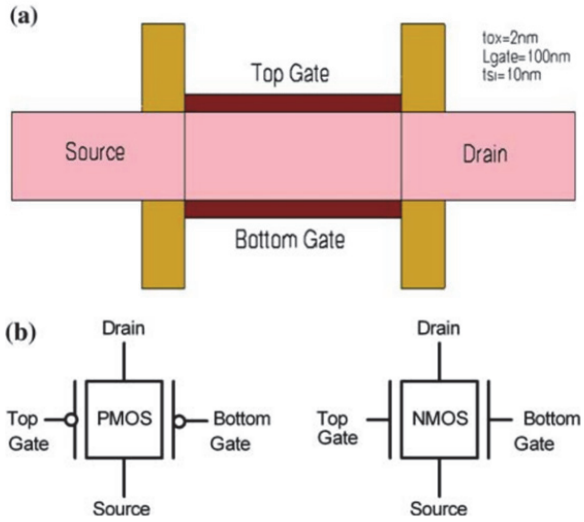

Figure 7 (a) Structure of the DGMOS device (b) DGPMOS and DGNMOS circuit symbols

Fig. 7 shows the structure and symbols of the DGMOS devices. The structure overcomes the short channel effects. The structure shows the drain, source, double gates and the body. If the gates are tied up it corresponds to the short-gated configuration. The other component in the structure is the fin or Silicon On Insulator (SOI) finger. The fin is protected by silicon fin nitride depositions.

5 RESULTS AND DISCUSSION

The implementation was done for the various blocks like the encoder, comparator, mux and control circuit of the ADC system. The resistor network with voltage references with respect to ground represents the threshold values of the bits.

The schematic of the encoder block is shown in Fig. 9. It converts the thermometer code into binary code with a gray code intermediate. The design using the FinFET provides current and logic for conversion. There is a one bit increase or decrease in the value while the quantization error is not considered. The digital accuracy is higher since each thermometer bit affects only one gray code bit. The offset errors are eliminated while the skew and jitter in the clock circuits will be corrected by the clock distribution unit. Latching of the signal is done to avoid the gain errors occurring at the output logic. Amplitude information was properly maintained as the biomedical system sensor output is less, below one step size. The NOT, AND, OR and XOR gates were implemented using CMOS and FinFET. The comparator further generates thermometer code and the final output is the binary code. The resolution of the ADC is maintained so as to avoid the quantization error.

The 8 bits, ranging from 1 to 8, have eight reference levels. The outputs from the comparator are fed into an encoder, which converts the voltage levels into binary

code. These binary equivalents are passed to the next stage, ultimately forming the digital output of the ADC. Several configurations and circuits were used for the comparator, as shown in Fig. 8.

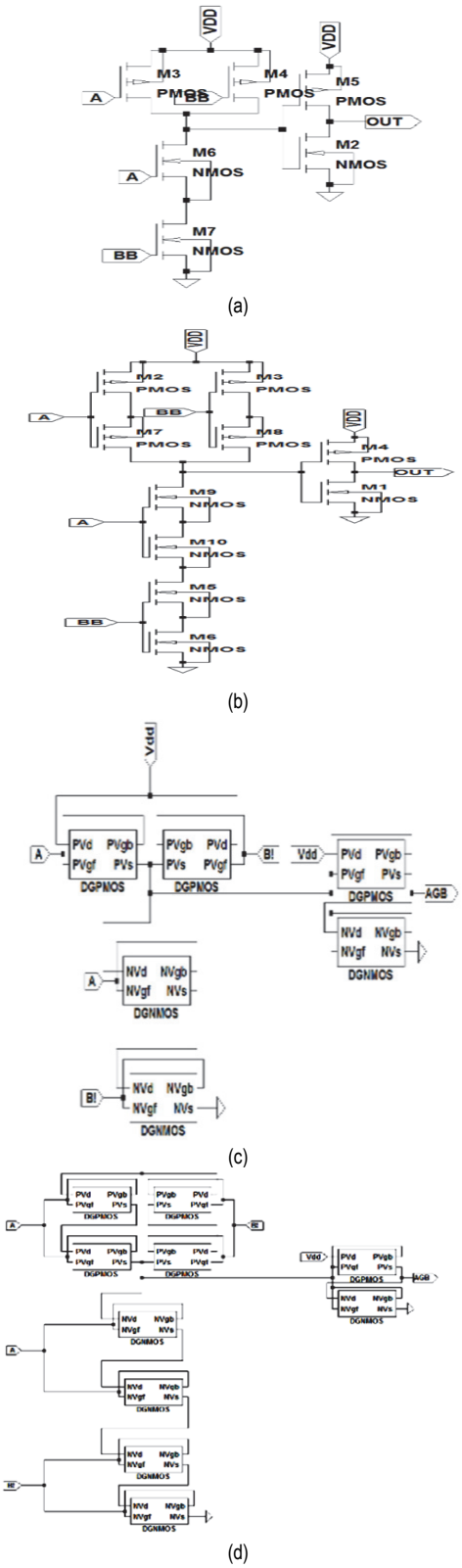

Figure 8 Comparator using (a) stacking technique, (b) without stacking, (c) using FinFET without and with and (d) stacking

During the testing of the circuits, both analog and digital voltages were used. For the comparator, the voltage levels ranged from 0 to 1 V. In the digital blocks, logic levels of 0 and 1 were determined by voltage levels below and above the threshold voltage (Vth). The Vth value was 0.6 V. Parameters such as power, current, and energy were measured. The frequency range used extended up to 2 GHz. The performance of the comparator, shown in Fig. 10, was evaluated both with and without the stacking technique.

Tab. 2 shows the performance of the dynamic comparator for CMOS and FinFET considering the stacking configuration. For this dynamic comparator the FinFET performance was found effective. The FinFET is saving power when compared with the CMOS counterpart. The temperature drift and supply voltage variations were not recorded and left for the future directions. The mismatch in the components can be addressed when the circuits were fabricated as integrated circuit. The component tolerances impacts the gain so do the reference voltage inaccuracies. In this simulation all reference voltages, supply voltages and other parameters were kept ideal values. But during fabrication the supply becomes external inputs which may have errors and fluctuations.

Table 2 Output of dynamic comparator

Circuit name	Configuration	Average power / nW	Peak power / nW
CMOS	without stacking	310	318
	with stacking	126	132
FinFET	without stacking	47	47
	with stacking	25	27

The proposed double tail structure enables fast latching due to large current in the latching stage. The comparator functions are not affected by the input common mode voltage. Kickback noise is shielded by the intermediate stage. The few disadvantages are the increased delay due to the additional transistors which can be eliminated. The results show that in VLSI technology the parameters on voltage supply, frequency of operation and area cannot be optimized at the same time. In the Tabs. 3 and 4 it can be seen that the performance of the circuits varies with different devices. The current driving capability also varies between the same circuits implemented with different devices. The power supply is 1 V for the circuits under investigation. The input signal frequency is kept at the range of 300 MHz to 3 GHz for higher speeds, FinFETs consume more power compared to CMOS circuits. However, for frequency ranges around 1 GHz, FinFETs demonstrate better performance. The various blocks of the ADC were implemented and tested.

Table 3 CMOS and FinFET based comparator performance comparison

Circuit name	Type	Average Current / µA	Average Power / nW	Average Energy / fJ
Double tail Comparator	CMOS	23	654	312
	FinFET	12	122	87
Proposed Low noise, Power Comparator	CMOS	485	224	98
	FinFET	324	112	86

The MUX and control circuit schematic is shown in Fig. 8 and Fig. 9. The control circuit is responsible for the overall operation of the ADC. The ADC operation consists of the control signals like SOC-Start of conversion, End of Conversion EOC, clock signal and RD -read for reading

the digital data. The embedded unit will send the signals for the proper functioning of the ADC system. The control signal is initiated and terminated by the program of the embedded system. The circuit developed provides sufficient current to take care of the handshaking signals of the ADC and the microcontroller or any other processor.

Table 4 Parameter comparison of various blocks of ADC in existing and proposed circuit

Name of circuit	Device	Average Current	Average Power	Average Energy
4 bit t2g encoder	CMOS	7.46u	8.66u	744f
	FinFET	2u	1.85u	2.3p
Control circuit	CMOS	647u	1.17m	93.96p
	FinFET	781u	1.04m	122.9p
Mux 8_1	CMOS	104m	22u	5.31n
	FinFET	1.97p	39f	$138e^{-21}$

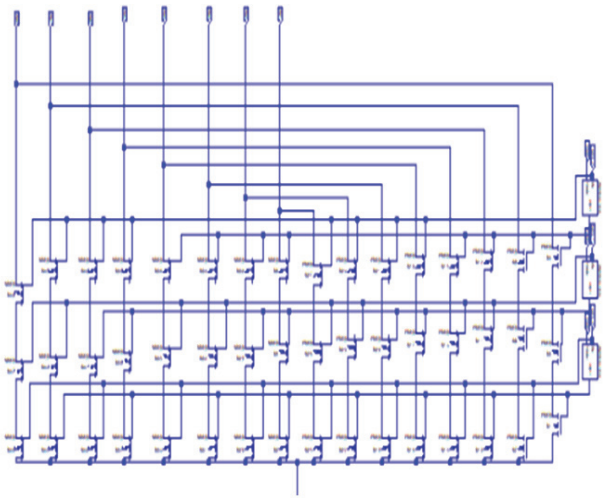

Figure 9 Schematic of the MUX circuit

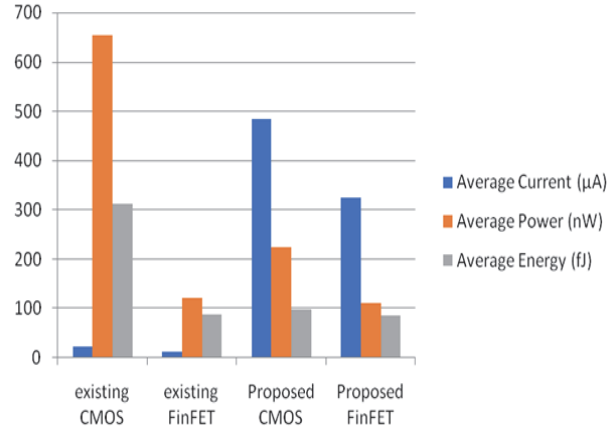

Figure 10 Comparison of the various comparators for current, power and energy - existing double tail comparator and proposed low noise comparator

Figs. 10 and 11 compare the ADC circuit for the proposed comparator with various existing circuits. From observations and investigations, it has been found that the proposed circuit consumes less power and has higher current-driving capability compared to existing methods. CMOS circuits consume more power due to leakage. Power analysis indicates that the developed circuits are suitable for all kinds of battery-operated applications. The current-driving capability increases in the designed circuits due to the elimination of leakage current during static operation. The speed is also improved, operating in the range of a few hundred MHz. For audio applications, since the switching factor is low, the circuits are expected to perform better; this aspect is left for future investigation.

Table 5 Parameter comparison of various circuits ADC in existing and proposed circuit

Circuit name	Average power / uW	Peak power / uW
CMOS (Babayan-Mashhadi et al.)	420	467
FinFET	67	68
CMOS (Varshney et al.)	334	336
FinFET	127	129
CMOS (Abumurad i et al.)	333	365
FinFET	177	182
CMOS (Abumurad et al.)	433	456
FinFET	174	179
CMOS (Ohhata et al.)	322	342
FinFET	122	176
CMOS (proposed)	126	132
FinFET (proposed)	54	59

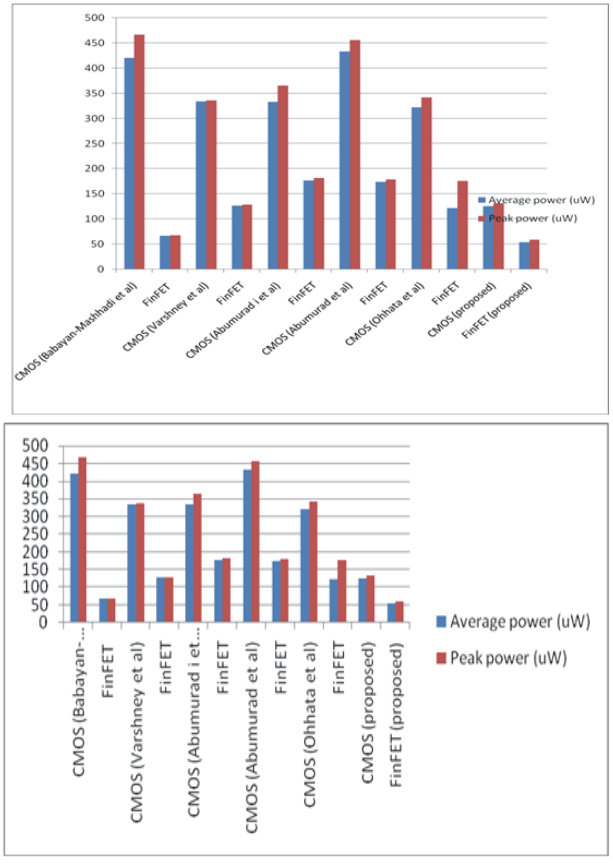

Figure 11 Comparison of the ADC unit for power existing and proposed designs

As the work is based on biomedical applications, where the frequency of operation is very low (in the range of a few Hz), the battery life is expected to be significantly extended. The ADC circuit can also be used in other applications, such as audio processing and sensor technology. In sensor technology integrated with IoT, applications include agriculture and wireless sensor networks for traffic management. VANET is another domain that requires a large number of sensors, where the proposed system can be effectively utilized. The circuit operates in a non-sequential manner and is triggered only by the start-of-conversion signal. The sampling frequency

is controlled programmatically. For example, an ADC used in heart-based systems typically operates at a sampling frequency of 360-500 Hz. For testing purposes, an 8-bit resolution was used. In biomedical applications, as the number of samples is lower due to the input frequency components ranging between 1 Hz and 1,000 Hz, the data rate can remain below a few MHz. However, the experiments were also tested at higher frequency ranges, up to a few hundred MHz.

6 CONCLUSION

In this paper, an improvement in driving current and power reduction using multigate devices was proposed. The circuits for the ADC were designed using CMOS and FinFET technology. The issues in CMOS circuits were addressed by employing dual-gate MOS devices. Low-power and improved current-driving circuits, including the encoder, multiplexer, control circuit, and comparator for flash ADC, were designed. The objective was achieved by designing a FinFET-based comparator, encoder, and supporting circuits for the ADC in a 32 nm process. Below the 32nm node, investigations show poor performance at higher speeds. The modified double-tail comparator and encoder unit reduce power consumption and enhance current-driving capability. In previous work, a 180 nm CMOS process was used. For the implementation, Taiwan Semiconductor models for CMOS and FinFET at 45 nm, 32 nm, and 14 nm were investigated using Synopsis HSPICE.

The circuits are planned for implementation in a 24-bit ADC with a transmission speed of 16 mega-samples per second in the future. The System-on-Chip (SoC) architecture will be built using the proposed ADC circuits. Further analysis, including temperature drift and supply voltage variation, will be conducted during fabrication.

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